# Features

- **Conforms to Intel LPC Interface Specification 1.0**
- **8M Bits of Flash Memory for Platform Code/Data Storage**
  - **Automated Byte-program and Sector-erase Operations**
- **Two Configurable Interfaces**
  - **Low Pin Count (LPC) Interface for In-System Operation**
  - **Address/Address Multiplexed (A/A Mux) Interface for Programming during Manufacturing**
- **Low Pin Count Hardware Interface Mode**
  - **5-signal Communication Interface Supporting x8 Reads and Writes**
  - **Read and Write Protection for Each Sector Using Software-controlled Registers**
  - **Two Hardware Write-protect Pins: One for the Top Boot Sector, One for All Other Sectors**
  - **Five General-purpose Inputs, GPIs, for Platform Design Flexibility**
  - **Operates with 33 MHz PCI Clock and 3.3V I/O**
- **Address/Address Multiplexed (A/A Mux) Interface**
  - **11-pin Multiplexed Address and 8-pin Data Interface**
  - **Supports Fast On-board or Out-of-system Programming**
- **Power Supply Specifications**
  - **$V_{CC}$: 3.3V ± 0.3V**
  - **$V_{PP}$: 3.3V and 12V for Fast Programming**
- **Industry-standard Package**
  - **40-lead TSOP or 32-lead PLCC**

# Description

The AT49LL080 is a Flash memory device designed to interface with the LPC bus for PC Applications. A feature of the AT49LL080 is the nonvolatile memory core. The high-performance memory is arranged in sixteen sectors (see page 11).

The AT49LL080 supports two hardware interfaces: Low Pin Count (LPC) for in-system operation and Address/Address Multiplexed (A/A Mux) for programming during manufacturing. The IC (Interface Configuration) pin of the device provides the control between the interfaces. The interface mode needs to be selected prior to power-up or before return from reset ($\overline{RST}$ or $\overline{INIT}$ low to high transition).

# Pin Configuration
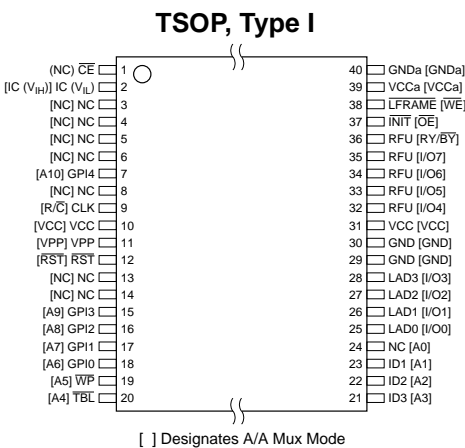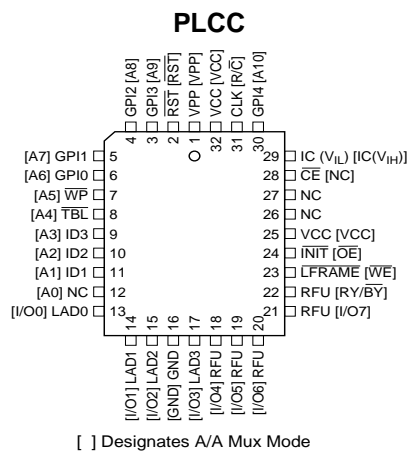
**8-megabit Low-pin Count Flash Memory**

**AT49LL080**

## PLCC



[ ] Designates A/A Mux Mode

## TSOP, Type I



[ ] Designates A/A Mux Mode

An internal Command User Interface (CUI) serves as the control center between the two device interfaces (LPC and A/A Mux) and internal operation of the nonvolatile memory. A valid command sequence written to the CUI initiates device automation.

Specifically designed for 3V systems, the AT49LL080 supports read operations at 3.3V and sector erase and program operations at 3.3V and 12V $V_{PP}$. The 12V $V_{PP}$ option renders the fastest program performance which will increase factory throughput, but is not recommended for standard in-system LPC operation in the platform. Internal $V_{PP}$ detection circuitry automatically configures the device for sector erase and program operations. Note that, while current for 12V programming will be drawn from $V_{PP}$, 3.3V programming board solutions should design such that $V_{PP}$ draws from the same supply as $V_{CC}$, and should assume that full programming current may be drawn from either pin.

## Low Pin Count Interface

The Low Pin Count (LPC) interface is designed to work with the I/O Controller Hub (ICH) during platform operation.

The LPC interface consists primarily of a five-signal communication interface used to control the operation of the device in a system environment. The buffers for this interface are PCI compliant. To ensure the effective delivery of security and manageability features, the LPC interface is the only way to get access to the full feature set of the device. The LPC interface is equipped to operate at 33 MHz, synchronous with the PCI bus.

## Address/Address Multiplexed Interface

The A/A Mux interface is designed as a programming interface for OEMs to use during motherboard manufacturing or component pre-programming.

The A/A Mux refers to the multiplexed row and column addresses in this interface. This approach is required so that the device can be tested and programmed quickly with automated test equipment (ATE) and PROM programmers in the OEM's manufacturing flow. This interface also allows the device to have an efficient programming interface with potentially large future densities, while still fitting into a 32-pin package. Only basic reads, programming, and erase of the nonvolatile memory sectors can be performed through the A/A Mux interface. In this mode LPC features, security features and registers are unavailable. A row/column (R/$\overline{\text{C}}$) pin determines which set of addresses "rows or columns" are latched.

## Block Diagram

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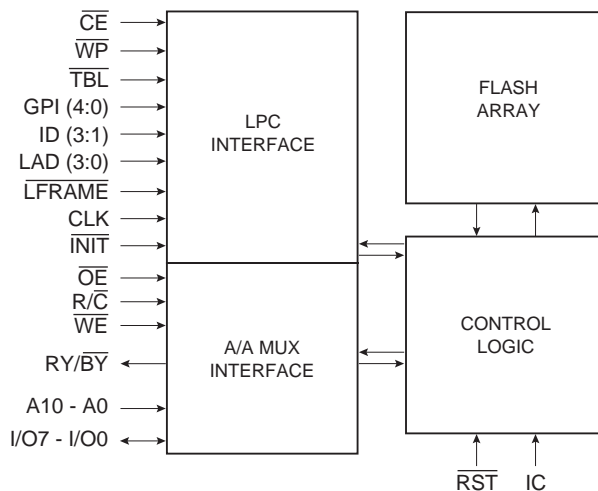
## Pin Description

Table 1 details the usage of each of the device pins. Most of the pins have dual function-ality, with functions in both the Firmware Hub and A/A Mux interfaces. A/A Mux functionality for pins is shown in **bold** in the description box for that pin. All pins are designed to be compliant with voltage of $V_{CC}$ + 0.3V max, unless otherwise noted.

**Table 1.** Pin Description

| Symbol | Type | Interface | | Name and Function |
| --- | --- | --- | --- | --- |
| | | LPC | A/A Mux | |
| IC | INPUT | X | X | **INTERFACE CONFIGURATION PIN:** This pin determines which interface is operational. This pin is held high to enable the A/A Mux interface. This pin is held low to enable the LPC interface. This pin must be set at power-up or before return from reset and not changed during device operation. This pin is pulled down with an internal resistor, with values between 20 and 100 kΩ With IC high (A/A Mux mode), this pin will exhibit a leakage current of approximately 200 µA. This pin may be floated, which will select LPC mode. |
| $\overline{RST}$ | INPUT | X | X | **INTERFACE RESET:** Valid for both A/A Mux and LPC interface operations. When driven low, $\overline{RST}$ inhibits write operations to provide data protection during power transitions, resets internal automation, and tri-states pins LAD[3:0] (in LPC interface mode). $\overline{RST}$ high enables normal operation. When exiting from reset, the device defaults to read array mode. |
| $\overline{INIT}$ | INPUT | X | | **PROCESSOR RESET:** This is a second reset pin for in-system use. This pin is internally combined with the $\overline{RST}$ pin. If this pin or $\overline{RST}$ is driven low, identical operation is exhibited. This signal is designed to be connected to the chipset INIT signal (Max voltage depends on the processor. Do not use 3.3V.) **A/A Mux = $\overline{OE}$** |
| CLK | INPUT | X | | **33 MHz CLOCK for LPC INTERFACE:** This input is the same as the PCI clock and adheres to the PCI specification. **A/A Mux = R/$\overline{C}$** |
| LAD[3:0] | I/O | X | | **ADDRESS AND DATA:** These pins provide LPC control signals, as well as addresses and command Inputs/Outputs Data. **A/A Mux = I/O[3:0]** |
| $\overline{LFRAME}$ | INPUT | X | | **FRAME:** This pin indicates the start of a data transfer operation; also used to abort an LPC cycle in progress. **A/A Mux = $\overline{WE}$** |
| ID[3:1] | INPUT | X | | **IDENTIFICATION INPUTS:** These three pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:1] = 000, and it is recommended that all subsequent devices should use a sequential up-count strapping (i.e., 001, 010, 011, etc.). These pins are pulled down with internal resistors, with values between 20 and 100 kΩ when in LPC mode. Any ID pins that are pulled high will exhibit a leakage current of approximately 200 µA. Any pins intended to be low may be left to float. In a single LPC system, all may be left floating. **A/A Mux = A[3:0]** |
| $\overline{CE}$ | INPUT | X | | When $\overline{CE}$ is low, the device is enabled. This pin is pulled down with an internal resistor and can exhibit a leakage current of approximately 10 µA. Since this pin is internally pulled down and thus can be left unconnected, the AT49LL080 is compatible with systems that do not use a $\overline{CE}$ signal. To reduce power, the device is placed in a low-power standby mode when $\overline{CE}$ is high. |

Table 1. Pin Description (Continued)

| Symbol | Type | Interface | | Name and Function |
|---|---|---|---|---|
| | | LPC | A/A Mux | |
| GPI[4:0] | INPUT | X | | **GENERAL PURPOSE INPUTS:** These individual inputs can be used for additional board flexibility. The state of these pins can be read through LPC registers. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain at the same level until the end of the read cycle. They may *only* be used for **3.3V** signals. Unused GPI pins must **not** be floated.<br>**A/A Mux = A[10:6]** |
| $\overline{TBL}$ | INPUT | X | | **TOP SECTOR LOCK:** When low, prevents programming or sector erase to the highest addressable sector (15), regardless of the state of the lock registers $\overline{TBL}$ high disables hardware write protection for the top sector, though register-based protection still applies. The status of $\overline{TBL}$ does not affect the status of sector-locking registers.<br>**A/A Mux = A4** |
| $\overline{WP}$ | INPUT | X | | **WRITE-PROTECT:** When low, prevents programming or sector erase to all but the highest addressable sectors (0 - 14), regardless of the state of the corresponding lock registers. $\overline{WP}$-high disables hardware write protection for these sectors, though register-based protection still applies. The status of $\overline{TBL}$ does not affect the status of sector-locking registers.<br>**A/A Mux = A5** |
| A0 - A10 | INPUT | | X | **LOW-ORDER ADDRESS INPUTS:** Inputs for low-order addresses during read and write operations. Addresses are internally latched during a write cycle. For the A/A Mux interface these addresses are latched by $R/\overline{C}$ and share the same pins as the high-order address inputs. |
| I/O0 - I/O7 | I/O | | X | **DATA INPUT/OUTPUTS:** These pins receive data and commands during write cycles and transmit data during memory array and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. |
| $\overline{OE}$ | INPUT | | X | **OUTPUT ENABLE:** Gates the device's outputs during a read cycle. |
| $R/\overline{C}$ | INPUT | | X | **ROW-COLUMN ADDRESS SELECT:** For the A/A Mux interface, this pin determines whether the address pins are pointing to the row addresses, A0 - A10, or to the column addresses, A11 - A19. |
| $\overline{WE}$ | INPUT | | X | **WRITE ENABLE:** Controls writes to the array sectors. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse. |
| $V_{PP}$ | SUPPLY | X | X | **SECTOR ERASE/PROGRAM POWER SUPPLY:** For erasing array sectors or programming data $0V \leq V_{PP} \leq 3.6V$ or 12V for faster erase and programming operations. The VPP pin can be left unconnected. Sector erase or program with an invalid $V_{PP}$ (see DC Characteristics) produces spurious results and should not be attempted. $V_{PP}$ may only be held at 12V for 80 hours over the lifetime of the device. |
| $V_{CC}$ | SUPPLY | X | X | **DEVICE POWER SUPPLY:** Internal detection automatically configures the device for optimized read performance. Do no float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid $V_{CC}$ voltages (see DC Characteristics) produce spurious results and should not be attempted. |
| GND | SUPPLY | X | X | **GROUND:** Do not float any ground pins. |
| $V_{CCa}$ | SUPPLY | X | X | **ANALOG POWER SUPPLY:** This supply should share the same system supply as $V_{CC}$. |

**Table 1.** Pin Description (Continued)

| Symbol | Type | Interface | | Name and Function |
|--------|------|-----------|---|-------------------|
| | | **LPC** | **A/A Mux** | |
| GNDa | SUPPLY | X | X | **ANALOG GROUND:** Should be tied to same plane as GND. |
| RFU | | X | | **RESERVED FOR FUTURE USE:** These pins are reserved for future generations of this product and should be connected accordingly. These pins may be left disconnected or driven. If they are driven, the voltage levels should meet $V_{IH}$ and $V_{IL}$ requirements.<br>**A/A Mux = I/O[7:4]** |
| NC | | X | X | **NO CONNECT:** Pin may be driven or floated. If it is driven, the voltage levels should meet $V_{IH}$ and $V_{IL}$. |
| RY/$\overline{BY}$ | OUTPUT | | X | **READY/BUSY:** Valid only in A/A Mux Mode. This output pin is a reflection of bit 7 in the status register. This pin is used to determine sector erase or program completion. |

## Low Pin Count Interface (LPC)

Table 2 lists the seven required signals used for the LPC interface.

**Table 2.** LPC Required Signal List

| Signal | Direction | | Description |
|--------|-----------|---|-------------|
| | **Peripheral** | **Master** | |
| LAD[3:0] | I/O | I/O | Multiplexed command, address and data |
| $\overline{LFRAME}$ | I | O | Indicates start of a new cycle, termination of broken cycle. |
| $\overline{RST}$ | I | I | Reset: Same as PCI Reset on the master. The master does not need this signal if it already has $\overline{PCIRST}$ on its interface. |
| CLK | I | I | Clock: Same 33 MHz clock as PCI clock on the master. Same clock phase with typical PCI skew. The master does not need this signal if it already has PCICLK on its interface. |

**LAD[3:0]:** The LAD[3:0] signal lines communicate address, control, and data information over the LPC bus between a master and a peripheral. The information communicated are: start, stop (abort a cycle), transfer type (memory, I/O, DMA), transfer direction (read/write), address, data, wait states, DMA channel, and bus master grant.

**LFRAME:** $\overline{LFRAME}$ is used by the master to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used be by peripherals to know when to monitor the bus for a cycle.

The $\overline{LFRAME}$ signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that peripherals must monitor the bus to determine whether the cycle is intended for them. The benefit to peripherals of $\overline{LFRAME}$ is, it allows them to enter lower power states internally.

When peripherals sample $\overline{LFRAME}$ active, they are to immediately stop driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

**RESET:** $\overline{RST}$ or $\overline{INIT}$ at VIL initiates a device reset. In read mode, $\overline{RST}$ or $\overline{INIT}$ low deselects the memory, places output drivers in a high-impedance state, and turns off all

internal circuits. $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ must be held low for time $t_{PLPH}$ (A/A Mux and LPC operation). The LPC resets to read array mode upon return from reset, and all sectors are set to default (locked) status regardless of their locked state prior to reset.

Driving $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ low resets the device, which resets the sector lock registers to their default (write-locked) condition. A reset time ($t_{PHQV}$ A/A Mux) is required from $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ switching high until outputs are valid. Likewise, the device has a wake time ($t_{PHRH}$ A/A Mux) from $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ high until writes to the CUI are recognized. A reset latency will occur if a reset procedure is performed during a programming or erase operation.

During sector erase or program, driving $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ low will abort the operation underway, in addition to causing a reset latency. Memory contents being altered are no longer valid, since the data may be partially erased or programmed.

It is important to assert $\overline{\text{RST}}$ or $\overline{\text{INIT}}$ during system reset. When the system comes out of reset, it will expect to read from the memory array of the device. If a system reset occurs with no LPC reset (this will be hardware dependent), it is possible that proper CPU initialization will not occur (the LPC memory may be providing status information instead of memory array data).

**CYCLE TYPES:** There are two types of cycles that are supported by the AT49LL080: LPC Memory Read and LPC Memory Write.

## Device Operation

**READ:** Read operations consist of START, CYCTYPE + DIR, ADDRESS, TAR, SYNC and data fields as shown in Figure 1 and described in Table 5. The different fields are described below. Commands using the read mode include the following functions: reading memory from the array, reading the identifier codes, reading the lock bit registers and reading the GPI registers. Memory information, identifier codes, or the GPI registers can be read independent of the $V_{PP}$ voltage. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode.

**READ CYCLE, SINGLE BYTE:** For read cycles, after the address is transferred, the master drives a TAR field to give ownership of the bus to the LPC. After the second clock of the TAR phase the LPC assumes the bus and begins driving SYNC values. When it is ready, it drives the low nibble, then the high nibble of data, followed by a TAR field to give control back to the master.

Figure 1 shows a device that requires three SYNC clocks to access data. Since the access time can begin once the address phase has been completed, the two clocks of the TAR phase can be considered as part of the access time of the part. For example, a device with a 120 ns access time could assert "0101b" for clocks 1 and 2 of the SYNC phase and "0000b" for the last clock of the SYNC phase. This would be equivalent to five clocks worth of access time if the device started that access at the conclusion of the preamble phase. Once SYNC is achieved, the device then returns the data in two clocks and gives ownership of the bus back to the master with a TAR phase.

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**START:** This one-clock field indicates the start of a cycle. It is valid on the last clock that $\overline{\text{LFRAME}}$ is sampled low. On the rising edge of CLK with $\overline{\text{LFRAME}}$ low, the contents of LAD3 - LAD0 must be 0000b to indicate the start of a LPC cycle.

**Table 3.** CYCTYPE + DIR Fields

| LAD[3:0] | Indication |
|----------|------------|
| 010xb | LPC Memory Read |
| 011xb | LPC Memory Write |

**CYCTYPES + DIR:** This one-clock field is used to indicate the type of cycle and direction of transfer. Bits 3 - 2 must be "01b" for a memory cycle. Bit 1 indicates the type of transfer: "0" for read operation, "1" for write operation. DIR field indication of transfer: "0" for read, "1" for write. Bit 0 is reserved. "010xb" indicates a memory read cycle; while "011xb" indicates a memory write cycle.

**MADDR (MEMORY ADDRESS):** This is an eight-clock field, which gives a 32-bit memory address. LPC supports the 32-bit address protocol. The address is transferred with the most significant nibble first. For the AT49LL080, address bit 23 directs Reads and Writes to memory locations ($A_{23}$ = 1) or to register access locations ($A_{23}$ = 0). $A_{22}$ - $A_{20}$ are device ID strapping bits, and $A_{19}$ - $A_0$ are decoded as memory addresses.

**TURN-AROUND (TAR):** This field is two clocks wide, and is driven by the master when it is turning control over to the LPC, (for example, to read data), and is driven by the LPC when it is turning control back over to the master. On the first clock of this two-clock-wide field, the master or LPC drives the LAD[3:0] lines to "1111b". On the second clock of this field, the master or peripheral tri-states the LAD[3:0] lines.

**SYNC:** This field is used to add wait states. It can be several clocks in length. On target or DMA cycles, this field is driven by the LPC. If the LPC needs to assert wait states, it does so by driving "0101b" (short SYNC) on LAD[3:0] until it is ready. When ready, it will drive "0000b". Valid values for this field are shown in Table 4.

**Table 4.** Valid SYNC Values

| Bits[3:0] | Indication |
|-----------|------------|
| 0000 | Ready: SYNC achieved with no error. |
| 0101 | Short Wait: Part indicating wait states. |

**Figure 1.** LPC Read Waveforms
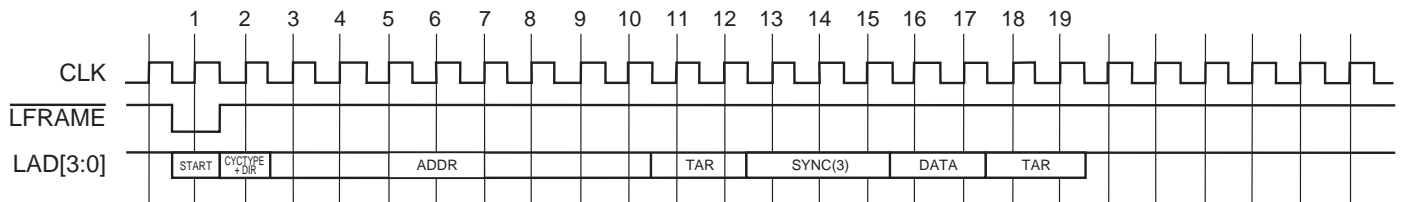


**Table 5.** LPC Read Cycle

| Clock Cycle | Field Name | Field Contents[1] LAD[3:0] | LAD[3:0] Direction | Comments |
|---|---|---|---|---|
| 1 | START | 0000b | IN | $\overline{LFRAME}$ must be active (low) for the part to respond. Only the last start field (before $\overline{LFRAME}$ transitioning high) should be recognized. The START field contents indicate an LPC memory read cycle. |
| 2 | CYCTYPE + DIR | 010xb | IN | Cycle Type: Indicates the type of cycle. Bits 3:2 must be 01 for a memory cycle. DIR: Bit 1 indicates the direction of the transfer (0 for read). Bit 0 is reserved. |
| 3 - 10 | ADDR | YYYY | IN | These eight clock cycles make up the 32-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most significant nibble first. |
| 11 | TAR0 | 1111b | IN then float | In this clock cycle, the master (ICH) has driven the bus to all 1s and then floats the bus, prior to the next clock cycle. This is the first part of the bus "turnaround cycle". |
| 12 | TAR1 | 1111b (float) | Float then OUT | The LPC takes control of the bus during this cycle. During the next clock cycle, it will be driving "sync data". |
| 13 - 14 | WSYNC | 0101b (WAIT) | OUT | The LPC outputs the value 0101, a wait-sync (WSYNC, a.k.a. "short-sync"), for two clock cycles. This value indicates to the master (ICH) that data is not yet available from the part. This number of wait-syncs is a function of the device's access time. |
| 15 | RSYNC | 0000b (READY) | OUT | During this clock cycle, the LPC will generate a "ready-sync" (RSYNC) indicating that the least significant nibble of the least significant byte will be available during the next clock cycle. |
| 16 | DATA | YYYY | OUT | YYYY is the least significant nibble of the least significant data byte. |
| 17 | DATA | YYYY | OUT | YYYY is the most significant nibble of the least significant data byte. |
| 18 | TAR0 | 1111b | OUT then float | The LPC Flash memory drives LAD0 - LAD3 to 1111b to indicate a turnaround cycle. |
| 19 | TAR1 | 1111b (float) | Float then IN | The LPC Flash memory floats its outputs, the master (ICH) takes control of LAD3 - LAD0. |

Note:  1.  Field contents are valid on the rising edge of the present clock cycle.

**WRITE:** Write operations consist of START, CYCTYPE + DIR, ADDRESS, data, TAR and SYNC fields as shown in Figure 2 and described in Table 6.

**WRITE CYCLES:** For write cycles, after the address is transferred, the master writes the low nibble, then the high nibble of data. After that the master drives a TAR field to give ownership of the bus to the LPC. After the second clock of the TAR phase, the target device assumes the bus and begins driving SYNC values. A TAR field to give control back to the master follows this.

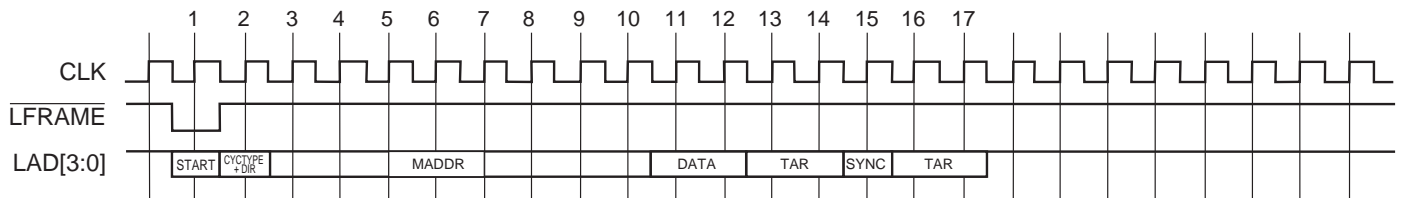**Figure 2.** LPC Single-byte Write Waveforms



**Table 6.** LPC Write Cycle

| Clock Cycle | Field Name | Field Contents[1] LAD[3:0] | LAD[3:0] Direction | Comments |
|---|---|---|---|---|
| 1 | START | 0000b | IN | LFRAME must be active (low) for the part to respond. Only the last start field (before LFRAME transitioning high) should be recognized. The START field contents indicate an LPC memory write cycle. |
| 2 | CYCTYPE + DIR | 011xb | IN | Cycle Type: Indicates the type of cycle. Bits 3:2 must be 01 for a memory cycle. DIR: Bit 1 indicates the direction of the transfer (1 for write). Bit 0 is reserved. |
| 3 - 10 | ADDR | YYYY | IN | These eight clock cycles make up the 32-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most significant nibble first. |
| 11 | DATA | YYYY | IN | This field is the least significant nibble of the data byte. This data is either the data to be programmed into the Flash memory or any valid Flash command. |
| 12 | DATA | YYYY | IN | This field is the most significant nibble of the data byte. |
| 13 | TAR0 | 1111b | IN then float | In this clock cycle, the master (ICH) has driven the bus to all 1s and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle". |
| 14 | TAR1 | 1111b (float) | Float then OUT | The LPC takes control of the bus during this cycle. During the next clock cycle it will be driving the "sync" data. |
| 15 | RSYNC | 0000b | OUT | The LPC outputs the values 0000, indicating that it has received data or a Flash command. |
| 16 | TAR0 | 1111b | OUT then Float | The LPC Flash memory drives LAD0 - LAD3 to 1111b to indicate a turnaround cycle. |
| 17 | TAR1 | 1111b (float) | Float then IN | The LPC Flash memory floats its outputs, the master (ICH) takes control of LAD3 - LAD0. |

Note:  1.  Field contents are valid on the rising edge of the present clock cycle.

**OUTPUT DISABLE:** When the LPC is not selected through a LPC read or write cycle, the LPC interface outputs (LAD[3:0]) are disabled and will be placed in a high-impedance state.

**Bus Abort**

The Bus Abort operation can be used to immediately abort the current bus operation. A Bus Abort occurs when $\overline{\text{LFRAME}}$ is driven Low, $V_{IL}$, during the bus operation; the memory will tri-state the Input/Output Communication pins, LAD3 - LAD0 and the LPC state machine will reset. During a write cycle, there is the possibility that an internal Flash write or erase operation is in progress (or has just been initiated). If the $\overline{\text{LFRAME}}$ is asserted during this time frame, the internal operation will not abort. The software must send an explicit Flash command to terminate or suspend the operation. The internal LPC state machine will not initiate a Flash write or erase operation until it has received the last nibble from the chipset. This means that $\overline{\text{LFRAME}}$ can be asserted as late as cycle 12 (Table 6) and no internal Flash operation will be attempted.

**HARDWARE WRITE-PROTECT PINS $\overline{\text{TBL}}$ AND $\overline{\text{WP}}$:** Two pins are available with the LPC to provide hardware write-protect capabilities.

The Top Sector Lock ($\overline{\text{TBL}}$) pin is a signal, when held low (active), prevents program or sector erase operations in the top sector of the device (sector 15) where critical code can be stored. When $\overline{\text{TBL}}$ is high, hardware write protection of the top sector is disabled. The write-protect ($\overline{\text{WP}}$) pin serves the same function for all the remaining sectors except the top sector. $\overline{\text{WP}}$ operates independently from $\overline{\text{TBL}}$ and does not affect the lock status of the top sector.

The $\overline{\text{TBL}}$ and $\overline{\text{WP}}$ pins must be set to the desired protection state prior to starting a program or erase operation since they are sampled at the beginning of the operation. Changing the state of $\overline{\text{TBL}}$ or $\overline{\text{WP}}$ during a program or erase operation may cause unpredictable results.

If the state of $\overline{\text{TBL}}$ or $\overline{\text{WP}}$ changes during a program suspend or erase suspend state, the changes to the device's locking status do not take place immediately. The suspended operation may be resumed to successfully complete the program or erase operation. The new lock status will take place after the program or erase operation completes.

These pins function in combination with the register-based sector locking (to be explained later). These pins, when active, will write-protect the appropriate sector(s), regardless of the associated sector locking registers. (For example, when $\overline{\text{TBL}}$ is active, writing to the top sector is prevented, regardless of the state of the Write Lock bit for the top sector's locking register. In such a case, clearing the write-protect bit in the register will have no functional effect, even though the register may indicate that the sector is no longer locked. The register may still be set to read-lock the sector, if desired.)

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## Device Memory Map with LPC Hardware Lock Architecture

| Sector | Size (Bytes) | Address Range | Hardware Write-protect Pin |
|---|---|---|---|
| SA15 | 64K | F0000 - FFFFF | $\overline{TBL}$ |
| SA14 | 64K | E0000 - EFFFF | $\overline{WP}$ |
| SA13 | 64K | D0000 - DFFFF | $\overline{WP}$ |
| SA12 | 64K | C0000 - CFFFF | $\overline{WP}$ |
| SA11 | 64K | B0000 - BFFFF | $\overline{WP}$ |
| SA10 | 64K | A0000 - AFFFF | $\overline{WP}$ |
| SA9 | 64K | 90000 - 9FFFF | $\overline{WP}$ |
| SA8 | 64K | 80000 - 8FFFF | $\overline{WP}$ |
| SA7 | 64K | 70000 - 7FFFF | $\overline{WP}$ |
| SA6 | 64K | 60000 - 6FFFF | $\overline{WP}$ |
| SA5 | 64K | 50000 - 5FFFF | $\overline{WP}$ |
| SA4 | 64K | 40000 - 4FFFF | $\overline{WP}$ |
| SA3 | 64K | 30000 - 3FFFF | $\overline{WP}$ |
| SA2 | 64K | 20000 - 2FFFF | $\overline{WP}$ |
| SA1 | 64K | 10000 - 1FFFF | $\overline{WP}$ |
| SA0 | 64K | 00000 - 0FFFF | $\overline{WP}$ |

## Register-based Locking and General-purpose Input Registers

A series of registers are available in the LPC to provide software read and write locking and GPI feedback. These registers are accessible through standard addressable memory space.

**REGISTERS:** The AT49LL080 has two types of registers: sector-locking registers and general-purpose input registers. The two types of registers appear at their respective address locations in the 4 GB system memory map.

**SECTOR-LOCKING REGISTERS:** The AT49LL080 has 16 (LR0 - LR15) sector-locking registers. Each sector-locking register controls the lock protection for a sector of memory as shown in Table 7. The sector-locking registers are accessible through the register memory address shown in the third column of Table 7. The sector-locking registers are read/write as shown in the last column of Table 7. Each sector has three dedicated locking bits as shown in Table 8 and Table 9.

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**Table 7.** Sector-locking Registers for AT49LL080

| Register Name | Sector Size | Register Memory Address (ID [3:0] = 0000) | Default Value | Type |
|---|---|---|---|---|
| LR15 | 64K | FF7F0002H | 01H | R/W |
| LR14 | 64K | FF7E0002H | 01H | R/W |
| LR13 | 64K | FF7D0002H | 01H | R/W |
| LR12 | 64K | FF7C0002H | 01H | R/W |
| LR11 | 64K | FF7B0002H | 01H | R/W |
| LR10 | 64K | FF7A0002H | 01H | R/W |
| LR9 | 64K | FF790002H | 01H | R/W |
| LR8 | 64K | FF780002H | 01H | R/W |
| LR7 | 64K | FF770002H | 01H | R/W |
| LR6 | 64K | FF760002H | 01H | R/W |
| LR5 | 64K | FF750002H | 01H | R/W |
| LR4 | 64K | FF740002H | 01H | R/W |
| LR3 | 64K | FF730002H | 01H | R/W |
| LR2 | 64K | FF720002H | 01H | R/W |
| LR1 | 64K | FF710002H | 01H | R/W |
| LR0 | 64K | FF700002H | 01H | R/W |
| FGPI-REG | | FF7C0100H | N/A | RO |

**Table 8.** Function of Sector-locking Bits

| Bit | Function |
|---|---|
| 7:3 | **Reserved** |
| 2 | **Read Lock**<br>1 = Prevents read operations in the sector where set.<br>0 = Normal operation for reads in the sector where clear. This is the default state. |
| 1 | **Lock-down**<br>1 = Prevents further set or clear operations to the Write Lock and Read Lock bits. Lock-down can only be set, but not cleared. The sector will remain locked-down until reset (with $\overline{RST}$ or $\overline{INIT}$), or until the device is power-cycled.<br>0 = Normal operation for Write Lock and Read Lock bits altering in the sector where clear. This is the default state. |
| 0 | **Write Lock**<br>1 = Prevents program or erase operations in the sector where set. This is the default state.<br>0 = Normal operation for programming and erase in the sector where clear. |

**Table 9.** Register-based Locking Value Definitions

| Data | Reserved Data 7 - 3 | Read Lock, Data 2 | Lock-down, Data 1 | Write Lock, Data 0 | Resulting Sector State[1] |
|---|---|---|---|---|---|
| 00 | 00000 | **0** | **0** | **0** | Full access |
| 01 | 00000 | **0** | **0** | **1** | Write locked – **Default state at power-up** |
| 02 | 00000 | **0** | **1** | **0** | Locked open (full access locked down) |
| 03 | 00000 | **0** | **1** | **1** | Write locked down |
| 04 | 00000 | **1** | **0** | **0** | Read locked |
| 05 | 00000 | **1** | **0** | **1** | Read and write locked |
| 06 | 00000 | **1** | **1** | **0** | Read locked down |
| 07 | 00000 | **1** | **1** | **1** | Read and write locked down |

Note: 1. The Write Lock bit must be set to the desired protection state prior to starting a program or erase operation since it is sampled at the beginning of the operation. Changing the state of the Write Lock bit during a program or erase operation may cause unpredictable results. If the state of the Write Lock bit changes during a program suspend or erase suspend state, the changes to the sector's locking status do not take place immediately. The suspended operation may be resumed successfully. The new lock status will take place after the program or erase operation completes. The individual bit functions are described in the following sections.

**READ LOCK:** The default read status of all sectors upon power-up is read-unlocked. When a sector's read-lock bit is set (1 state), data cannot be read from that sector. An attempted read from a read-locked sector will result in data 00H being read. (Note that failure is not reflected in the status register). The read-lock status can be unlocked by clearing (0 state) the read-lock bit, provided the lock-down bit has not been set. The current read-lock status of a particular sector can be determined by reading the corresponding read-lock bit.

**WRITE LOCK:** The default write status of all sectors upon power-up is write-locked (1 state). Any program or erase operations attempted on a locked sector will return an error in the status register (indicating sector lock). The status of the locked sector can be changed to unlocked (0 state) by clearing the write-lock bit, provided the lock-down bit is not also set. The current write-lock status of a particular sector can be determined by reading the corresponding write-lock bit. Any program or erase operations attempted on a locked sector will return an error in the status register (indicating sector lock). The write-lock functions in conjunction with the hardware write-lock pins, $\overline{TBL}$ and $\overline{WP}$. When active, these pins take precedence over the register-locking function and write-lock the top sector or remaining sectors, respectively. Reading this register will not read the state of the $\overline{TBL}$ or $\overline{WP}$ pins.

**LOCK-DOWN:** When in the LPC interface mode, the default lock-down status of all sectors upon power-up is not-locked-down (0 state). The lock-down bit for any sector may be set (1 state), but only once, as future attempted changes to that sector locking register will be ignored. The lock-down bit is only cleared upon a device reset with $\overline{RST}$ or $\overline{INIT}$. The current lock-down status of a particular sector can be determined by reading the corresponding lock-down bit. Once a sector's lock-down bit is set, the read- and write-lock bits for that sector can no longer be modified and the sector is locked down in its current state of read and write accessibility.

**GENERAL-PURPOSE INPUTS REGISTER:** This register reads the status of the GPI[4:0] pins on the LPC at power-up. Since this is a pass-through register, there is no default value as shown in Table 7. It is recommended that the GPI pins be in the desired state before $\overline{LFRAME}$ is brought low for the beginning of the next bus cycle, and remain in that state until the end of the cycle.

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**Table 10.** General-purpose Input Registers

| Bit | Function |
|-----|----------|
| 7:5 | **Reserved** |
| 4 | **GPI[4]**<br>Reads status of general-purpose input pin (PLCC-30/TSOP-7) |
| 3 | **GPI[3]**<br>Reads status of general-purpose input pin (PLCC-3/TSOP-15) |
| 2 | **GPI[2]**<br>Reads status of general-purpose input pin (PLCC-4/TSOP-16) |
| 1 | **GPI[1]**<br>Reads status of general-purpose input pin (PLCC-5/TSOP-17) |
| 0 | **GPI[0]**<br>Reads status of general-purpose input pin (PLCC-6/TSOP-18) |

# Command Definitions in (Hex)

| Command Sequence | Bus Cycles | Operation | 1st Bus Cycle Addr | 1st Bus Cycle Data | Operation | 2nd Bus Cycle Addr | 2nd Bus Cycle Data |
|---|---|---|---|---|---|---|---|
| Read Array/Reset | 1 | Write | XXXX | FF | | | |
| Sector Erase[2][3] | 2 | Write | SA | 20 | Write | SA | D0 |
| Byte Program[2][4] | 2 | Write | Addr | 40 or 10 | Write | Addr | $D_{IN}$ |
| Sector Erase Suspend[2] | 1 | Write | XXXX | B0 | | | |
| Program Suspend[2] | | Write | | | | | |
| Sector Erase Resume[2] | 1 | Write | XXXX | D0 | | | |
| Program Resume[2] | | Write | | | | | |
| Product ID Entry[5] | 2 | Write | XXXX | 90 | Read | AID[6] | $D_{OUT}$ |
| Read Status Register | 2 | Write | XXXX | 70 | Read | XXXX | SRD[7] |
| Clear Status Register | 1 | Write | XXXX | 50 | | | |

Notes: 1. X = Any valid address within the device.
2. The sector must not be write locked when attempting sector erase or program operations. Attempts to issue a sector erase or byte program to a write locked sector will fail.
3. SA = Sector address. Any byte address within a sector can be used to designate the sector address (see page 11).
4. Either 40H or 10H is recognized as the program setup.
5. Following the Product ID Entry command, read operations access manufacture and device ID. See Table 11.
6. AID = Address used to read data for manufacture or device ID.
7. SRD = Data Read from status register.

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**READ ARRAY:** Upon initial device power-up and after exit from reset, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal state machine (WSM) has started a block erase or program operation, the device will not recognize the Read Array Command until the operation is completed, unless the operation is suspended via an Erase Suspend or Program Suspend Command. The Read Array command functions independently of the $V_{PP}$ voltage.

**PRODUCT IDENTIFICATION:** The product identification mode identifies the device and manufacturer as Atmel.

Following the Product ID Entry command, read cycles from the addresses shown in Table 11 retrieve the manufacturer and device code. To exit the product identification mode, any valid command can be written to the device. The Product ID Entry command functions independently of the $V_{PP}$ voltage.

**Table 11.** Identifier Codes

| Code | Address (AID) | Data |
|------|---------------|------|
| Manufacturer Code | 00000 | 1FH |
| Device Code | 00001 | EBH |

**SECTOR ERASE:** Before a byte can be programmed, it must be erased. The erased state of the memory bits is a logical "1". Since the AT49LL080 does not offer a complete chip erase, the device is organized into multiple sectors that can be individually erased. The Sector Erase command is a two-bus cycle operation.

Successful sector erase requires that the corresponding sector's Write Lock bit be cleared and the corresponding write-protect pin ($\overline{TBL}$ or $\overline{WP}$) be inactive. If sector erase is attempted when the sector is locked, the sector erase will fail, with the reason for failure in the status register.

Successful sector erase only occurs when $V_{PP} = V_{PPH1}$ or $V_{PPH2}$. If the erase operation is attempted at $V_{PP} \neq V_{PPH1}$ or $V_{PPH2}$ erratic results may occur.

**BYTE PROGRAMMING:** The device is programmed on a byte-by-byte basis. Programming is accomplished via the internal device command register and is a two-bus cycle operation. The programming address and data are latched in the second bus cycle. The device will automatically generate the required internal programming pulses. Please note that a "0" cannot be programmed back to a "1"; only an erase operation can convert "0"s to "1"s.

After the program command is written, the device automatically outputs the status register data when read. When programming is complete, the status register may be checked. If a program error is detected, the status register should be cleared before corrective action is taken by the software. The internal WSM verification Error Checking only detects "1"s that do not successfully program to "0"s.

Reliable programming only occurs when $V_{PP} = V_{PPH1}$ or $V_{PPH2}$. If the program operation is attempted at $V_{PP} \neq V_{PPH1}$ or $V_{PPH2}$ erratic results may occur.

A successful program operation also requires that the corresponding sector's Write Lock bit be cleared, and the corresponding write-protect pin ($\overline{TBL}$ or $\overline{WP}$) be inactive. If a program operation is attempted when the sector is locked, the operation will fail.

**ERASE SUSPEND:** The Erase Suspend command allows sector-erase interruption to read or program data in another sector of memory. Once the sector erase process starts, writing the sector erase suspend command requests that the WSM suspend the

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sector erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the sector erase suspend command is written. Polling the status register can help determine when the sector erase operation was suspended. After a successful suspend, a Read Array command can be written to read data from a sector other than the suspended sector. A program command sequence may also be issued during erase suspend to program data in sectors other than the sector currently in the erase suspend mode.

The other valid commands while sector erase is suspended include Read Status Register and Sector Erase Resume. After a Sector Erase Resume command is written, the WSM will continue the sector erase process. $V_{PP}$ must remain at $V_{PPH1/2}$ (the same $V_{PP}$ level initially used for sector erase) while sector erase is suspended. $\overline{RST}$ or $\overline{INIT}$ must also remain at $V_{IH}$. Sector erase cannot resume until program operations initiated during sector erase suspend have completed.

**PROGRAM SUSPEND:** The Program Suspend command allows program interruption to read data in other memory locations. Once the program process starts, writing the Program Suspend Command requests that the WSM suspend the program sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the program suspend command is written. Polling the status register can help determine when the program operation was suspended. After a successful suspend, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while program is suspended are Read Status Register and Program Resume. $V_{PP}$ must remain at $V_{PPH1/2}$ (the same $V_{PP}$ level used for program) while in program suspend mode. $\overline{RST}$ or $\overline{INIT}$ must also remain at $V_{IH}$.

**READ STATUS REGISTER:** The status register may be read to determine when a sector erase or program completes and whether the operation completed successfully. The status register may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations will return data from the status register until another valid command is written. The Read Status Register command functions independently of the $V_{PP}$ voltage.

**CLEAR STATUS REGISTER:** Error flags in the status register can only be set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions. The Clear Status Register command functions independently of the applied $V_{PP}$ voltage.

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## Status Register Definition

| B7 | Write State Machine Status[1] | 1 | Ready |
|---|---|---|---|
| | | 0 | Busy |
| B6 | Erase Suspend Status | 1 | Sector Erase Suspended |
| | | 0 | Sector Erase in Progress/Completed |
| B5 | Erase Status[2] | 1 | Error in Sector Erasure |
| | | 0 | Successful Sector Erase |
| B4 | Program Status | 1 | Error in Program |
| | | 0 | Successful Program |
| B2 | Program Suspend Status | 1 | Program Suspended |
| | | 0 | Program in Progress/Completed |
| B1 | Device Protect Status[3] | 1 | Write Lock Bit, $\overline{TBL}$ Pin or $\overline{WP}$ Pin Detected, Operation Abort |
| | | 0 | Unlock |
| B0 | Reserved for Future Enhancements[4] | | |

Notes: 1. Check B7 to determine sector erase or program completion. B6 - B0 are invalid while B7 = "0".
2. If both B5 and B4 are "1"s after a sector erase attempt, an improper command sequence was entered.
3. B1 does not provide a continuous indication of Write Lock bit, $\overline{TBL}$ pin or $\overline{WP}$ pin values. The WSM interrogates the Write Lock bit, $\overline{TBL}$ pin or $\overline{WP}$ pin only after a sector erase or program operation. Depending on the attempted operation, it informs the system whether or not the selected sector is locked.
4. B0 is reserved for future use and should be masked out when polling the status register.

## A/A Mux Interface

The following information applies *only* to the AT49LL080 when in A/A Mux Mode. Information on LPC Mode (the standard operating mode) is detailed earlier in this document. Electrical characteristics in A/A Mux Mode are provided on pages starting from page 24.

The AT49LL080 is designed to offer a parallel programming mode for faster factory programming. This mode, called A/A Mux Mode, is selected by having this IC pin high. The IC pin is pulled down internally in the AT49LL080, so a modest current should be expected to be drawn (see Table 1 on page 3 for further information). Four control pins dictate data flow in and out of the component: R/$\overline{C}$, $\overline{OE}$, $\overline{WE}$, and $\overline{RST}$. R/$\overline{C}$ is the A/A Mux control pin used to latch row and column addresses. $\overline{OE}$ is the data output control pin (I/O0 - I/O7), drives the selected memory data onto the I/O bus, when active $\overline{WE}$ and $\overline{RST}$ must be at $V_{IH}$.

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**BUS OPERATION:** All A/A Mux bus cycles can be conformed to operate on most auto-mated test equipment and PROM programmers.

## Bus Operations

| Mode | $\overline{\text{RST}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | Address | $V_{PP}$ | I/O0 - I/O7 |
|------|------|------|------|---------|-----|-------------|
| Read[1][5] | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | X | X | $D_{OUT}$ |
| Output Disable[5] | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | X | High-Z |
| Product ID Entry[5] | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | [2] | X | Note 3 |
| Write[3][4][5] | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | X | X | $D_{IN}$ |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$ for control and address input pins and $V_{PPH1/2}$ for the VPP supply pin. See the "DC Characteristics" for $V_{PPH1/2}$ voltages.
2. See Table 11 on page 15 for Product ID Entry data and addresses.
3. Command writes involving sector erase or program are reliably executed when $V_{PP}$ = $V_{PPH1/2}$ and $V_{CC}$ = $V_{CC}$ ± 0.3V.
4. Refer to "A/A Mux Read-only Operations" for valid $D_{IN}$ during a write operation.
5. $V_{IH}$ and $V_{IL}$ refer to the DC characteristics associated with Flash memory output buffers: $V_{IL}$ min = 0.5V, $V_{IL}$ max = 0.8V, $V_{IH}$ min = 2.0V, $V_{IH}$ max = $V_{CC}$ + 0.5V.

**OUTPUT DISABLE/ENABLE:** With $\overline{\text{OE}}$ at a logic-high level ($V_{IH}$), the device outputs are disabled. Output pins I/O0 - I/O7 are placed in the high-impedance state. With $\overline{\text{OE}}$ at a logic-low level ($V_{IL}$), the device outputs are enabled. Output pins I/O0 - I/O7 are placed in a output-drive state.

**ROW/COLUMN ADDRESSES:** R/$\overline{\text{C}}$ is the A/A Mux control pin used to latch row (A0 - A10) and column addresses (A11 - A19). R/$\overline{\text{C}}$ latches row addresses on the falling edge and column addresses on the rising edge.

**RDY/$\overline{\text{BUSY}}$:** An open drain Ready/$\overline{\text{Busy}}$ output pin provides a hardware method of detecting the end of a program or erase operation. RDY/$\overline{\text{Busy}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle.

# Absolute Maximum Ratings*

Voltage on Any Pin
(except $V_{PP}$) ................................-0.5V to +VCC + 0.5V[1][2][4]

$V_{PP}$ Voltage ......................................... -0.5V to +13.0V[1][2][3]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. All specified voltages are with respect to GND. Minimum DC voltage on the $V_{PP}$ pin is -0.5V. During transitions, this level may undershoot to -2.0V for periods of <20 ns. During transitions, this level may overshoot to $V_{CC}$ + 2.0V for periods <20 ns.
2. Maximum DC voltage on $V_{PP}$ may overshoot to +13.0V for periods <20 ns.
3. Connection to supply of $V_{HH}$ is allowed for a maximum cumulative period of 80 hours.
4. Do not violate processor or chipset limitations on the $\overline{INIT}$ pin.

# Operating Conditions

Temperature and $V_{CC}$

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|--------|-----------|----------------|-----|-----|------|
| $T_C$ | Operating Temperature[1] | Case Temperature | 0 | +85 | $°C$ |
| $V_{CC}$ | $V_{CC}$ Supply Voltage | | 3.0 | 3.6 | V |

Note: 1. This temperature requirement is different from the normal commercial operating condition of Flash memories.

# LPC Interface DC Input/Output Specifications

| Symbol | Parameter | Conditions | Min | Max | Units |
|--------|-----------|------------|-----|-----|-------|
| $V_{IH}$[3] | Input High Voltage | | 0.5 $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{IH}$ ($\overline{INIT}$)[5] | $\overline{INIT}$ Input High Voltage | | 1.35 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ ($\overline{INIT}$)[5] | $\overline{INIT}$ Input Low Voltage | | | 0.85 | V |
| $V_{IL}$[3] | Input Low Voltage | | -0.5 | 0.3 $V_{CC}$ | V |
| $I_{IL}$[4] | Input Leakage Current[1] | 0 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = -500 µA | 0.9 $V_{CC}$ | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 1500 µA | | 0.1 $V_{CC}$ | V |
| $C_{IN}$ | Input Pin Capacitance | | | 13 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 3 | 12 | pF |
| $L^{pin}$[2] | Recommended Pin Inductance | | | 20 | nH |

Notes: 1. Input leakage currents include high-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Refer to PCI spec.
3. Inputs are not "5-volt safe."
4. $I_{IL}$ may be changed on IC and ID pins (up to 200 µA) if pulled against internal pull-downs. Refer to the pin descriptions.
5. Do not violate processor or chipset specifications regarding the $\overline{INIT}$ pin voltage.

## Power Supply Specifications – All Interfaces

| Symbol | Parameter | Conditions | Min | Max | Units |
|--------|-----------|------------|-----|-----|-------|
| $V_{PPH1}$ | $V_{PP}$ Voltage | | 0 | 3.6 | V |
| $V_{PPH2}$ | $V_{PP}$ Voltage | | 11.4 | 12.6 | V |
| $V_{PPLK}$ | $V_{PP}$ Lockout Voltage | | 1.5 | | V |
| $V_{LKO}$ | $V_{CC}$ Lockout Voltage | | 1.5 | | V |
| $I_{CCSL1}$ | $V_{CC}$ Standby Current (LPC Interface)[2] | Voltage range of all inputs is $V_{IH}$ to $V_{IL}$, $\overline{LFRAME} = V_{IH}$,[3]  $V_{CC} = 3.6V$, CLK f = 33 MHz  No internal operations in progress | | 100[4] | µA |
| $I_{CCSL2}$ | $V_{CC}$ Standby Current (LPC Interface)[2] | $\overline{LFRAME} = V_{IL}$[3]  $V_{CC} = 3.6V$, CLK f = 33 MHz  No internal operations in progress | | 10[4] | mA |
| $I_{CCA}$ | $V_{CC}$ Active Current[2] | $V_{CC} = V_{CC}$ Max,[3] CLK f = 33 MHz  Any internal operation in progress,  $I_{OUT} = 0$ mA | | 67[4] | mA |
| $I_{PPR}$ | $V_{PP}$ Read Current[2] | $V_{PP} \geq V_{CC}$ | | 200 | µA |
| $I_{PPWE}$ | $V_{PP}$ Program or Erase Current | $V_{PP} = 3.0 - 3.6V$[2] | | 40 | mA |
| | | $V_{PP} = 11.4 - 12.6V$ | | 15 | mA |

Notes: 1. All currents are in RMS unless otherwise noted. These currents are valid for all packages.
2. $V_{PP} = V_{CC}$.
3. $V_{IH} = 0.9\ V_{CC}$, $V_{IL} = 0.1\ V_{CC}$ per the PCI output $V_{OH}$ and $V_{OL}$ spec.
4. This number is the worst case of $I_{PP} + I_{CC}$ Memory Core + $I_{CC}$ LPC Interface.

## LPC Interface AC Input/Output Specifications

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{oh}(AC)$ | Switching Current High | $0 < V_{OUT} \leq 0.3\ V_{CC}$ | $-12\ V_{CC}$ | | mA |
| | | $0.3\ V_{CC} < V_{OUT} < 0.9\ V_{CC}$ | $-17.1\ (V_{CC} - V_{OUT})$ | | mA |
| | | $0.7\ V_{CC} < V_{OUT} < V_{CC}$ | | Note 2 | |
| | (Test Point) | $V_{OUT} = 0.7\ V_{CC}$ | | $-32\ V_{CC}$ | mA |
| $I_{ol}(AC)$ | Switching Current Low | $V_{CC} > V_{OUT} \geq 0.6\ V_{CC}$ | $16\ V_{CC}$ | | mA |
| | | $0.6\ V_{CC} > V_{OUT} > 0.1\ V_{CC}$ | $-17.1\ (V_{CC} - V_{OUT})$ | | mA |
| | | $0.18\ V_{CC} > V_{OUT} > 0$ | | Note 3 | |
| | (Test Point) | $V_{OUT} = 0.18\ V_{CC}$ | | $38\ V_{CC}$ | mA |
| $I_{cl}$ | Low Clamp Current | $-3 < V_{IN} \leq 1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| $I_{ch}$ | High Clamp Current | $V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$ | $25 + (V_{IN} - V_{CC} - 1)/0.015$ | | mA |
| slewr | Output Rise Slew Rate | $0.2\ V_{CC} - 0.6\ V_{CC}$ load[1] | 1 | 4 | V/ns |
| slewf | Output Fall Slew Rate | $0.6\ V_{CC} - 0.2\ V_{CC}$ load[1] | 1 | 4 | V/ns |

Notes: 1. PCI specification output load is used.
2. $I_{OH} = (98.0/V_{CC}) * (V_{OUT} - V_{CC}) * (V_{OUT} + 0.4\ V_{CC})$.
3. $I_{OL} = (256/V_{CC}) * V_{OUT}\ (V_{CC} - V_{OUT})$.

## LPC Interface AC Timing Specifications

### Clock Specification

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{CYC}$ | CLK Cycle Time[1] | | 30 | $\infty$ | ns |
| $t_{HIGH}$ | CLK High Time | | 11 | | ns |
| $t_{LOW}$ | CLK Low Time | | 11 | | ns |
| - | CLK Slew Rate | peak-to-peak | 1 | 4 | V/ns |
| - | $\overline{RST}$ or $\overline{INIT}$ Slew Rate[2] | | 50 | | mV/ns |

Notes: 1. PCI components must work with any clock frequency between nominal DC and 33 MHz. Frequencies less than 16 MHz may be guaranteed by design rather than testing.
2. Applies only to rising edge of signal.

### Clock Waveform

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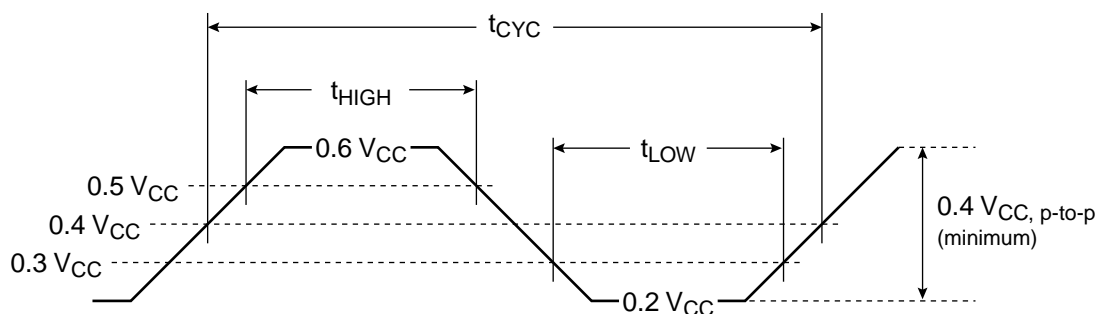
## Signal Timing Parameters

| Symbol | PCI Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{CHQX}$ | $t_{val}$ | CLK to Data Out[1] | 2 | 11 | ns |
| $t_{CHQX}$ | $t_{on}$ | CLK to Active (Float to Active Delay)[2] | 2 | | ns |
| $t_{CHQZ}$ | $t_{off}$ | CLK to Inactive (Active to Float Delay)[2] | | 28 | ns |
| $t_{AVCH}$ $t_{DVCH}$ | $t_{su}$ | Input Set-up Time[3] | 9 | | ns |
| $t_{CHAX}$ $t_{CHDX}$ | $t_{h}$ | Input Hold Time[3] | 0 | | ns |
| $t_{VSPL}$ | $t_{rst}$ | Reset Active Time after Power Stable | 1 | | ms |
| $t_{CSPL}$ | $t_{rst-clk}$ | Reset Active Time after CLK Stable | 100 | | µs |
| $t_{PLQZ}$ | $t_{rst-off}$ | Reset Active to Output Float Delay[2] | | 48 | ns |

Notes:  1. Minimum and maximum times have different loads. See PCI spec.
2. For purposes of Active/Float timing measurements, the high-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
3. This parameter applies to any input type (excluding CLK).

## Output Timing Parameters
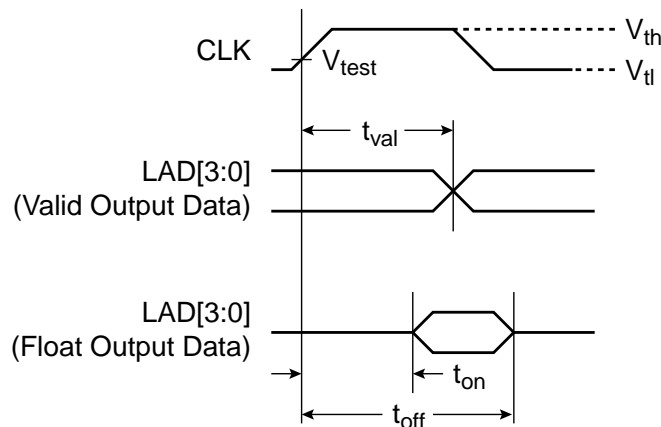


## Input Timing Parameters

3273C–FLASH–5/03
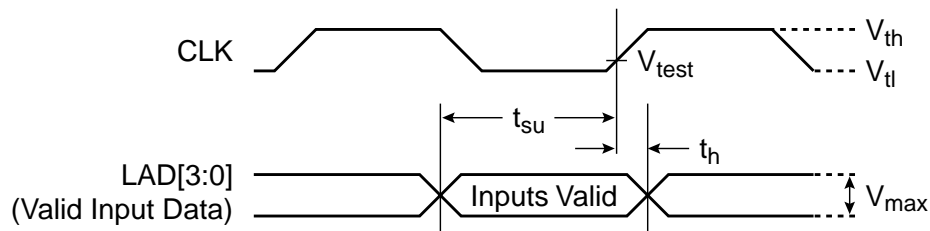
## Interface Measurement Condition Parameters

| Symbol | Value | Units |
|---|---|---|
| $V_{th}$[1] | 0.6 $V_{CC}$ | V |
| $V_{tl}$[1] | 0.2 $V_{CC}$ | V |
| $V_{test}$ | 0.4 $V_{CC}$ | V |
| $V_{max}$[1] | 0.4 $V_{CC}$ | V |
| Input Signal Edge Rate | 1 V/ns | |

Note: 1. The input test environment is done with 0.1 $V_{CC}$ of overdrive over $V_{IH}$ and $V_{IL}$. Timing parameters must be met with no more overdrive than this. $V_{max}$ specifies the maximum peak-to-peak waveform allowed for measuring the input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

## Reset Operations

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PLPH}$[1] | $\overline{RST}$ or $\overline{INIT}$ Pulse Low Time (If $\overline{RST}$ or $\overline{INIT}$ is tied to $V_{CC}$, this specification is not applicable) | 100 | | ns |

Note: 1. A reset latency of 20 μs will occur if a reset procedure is performed during a programming or erase operation.

## AC Waveform for Reset Operation
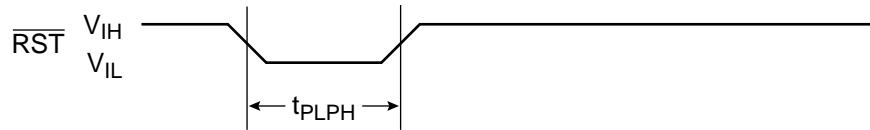


## Sector Programming Times

| Parameter | 3.3V $V_{PP}$ | | 12V $V_{PP}$ | | Unit |
|---|---|---|---|---|---|
| | Typ[1] | Max | Typ[1] | Max | |
| Byte Program Time[2] | 30.0 | 300 | 12.0 | 125 | μs |
| Sector Program Time[2] | 2.0 | 20.0 | 0.8 | 8.0 | sec |
| Sector Erase Time[2] | 0.8 | 1.0 | 0.35 | 0.6 | sec |

Notes: 1. Typical values measured at $T_A$ = +25° C and nominal voltages.
2. Excludes system-level overhead.

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**ELECTRICAL CHARACTERISTICS IN A/A MUX MODE:** Certain specifications differ from the previous sections, when programming in A/A Mux Mode. The following subsections provide this data. Any information that is not shown here is not specific to A/A Mux Mode and uses the LPC Mode specifications.

## A/A Mux Mode Interface DC Input/Output Specifications

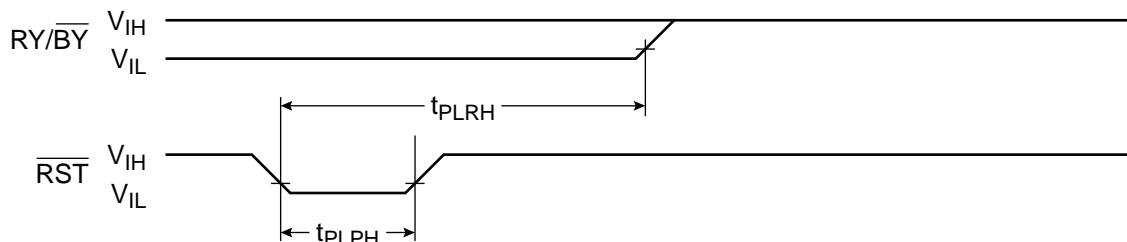| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}^{(3)}$ | Input High Voltage | | $0.5\ V_{CC}$ | $V_{CC} + 0.5$ | V |
| $V_{IL}^{(3)}$ | Input Low Voltage | | -0.5 | 0.8 | V |
| $I_{IL}^{(4)}$ | Input Leakage Current | $V_{CC} = V_{CC}$ max, $V_{out} = V_{CC}$ or GND | | ±10 | µA |
| $V_{OH}$ | Output High Voltage | $V_{CC} = V_{CC}$ min, $I_{OH}$ = -2.5 mA $V_{CC} = V_{CC}$ min, $I_{OH}$ = -100 µA | $0.85\ V_{CC}$ Min $V_{CC} = 0.4$ | | V V |
| $V_{OL}$ | Output Low Voltage | $V_{CC} = V_{CC}$ min, $I_{OL}$ = 2 mA | | 0.4 | V |
| $C_{IN}$ | Input Pin Capacitance | | | 13 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 3 | 12 | pF |
| $L_{PIN}^{(2)}$ | Recommended Pin Inductance | | | 20 | nH |

Notes: 1. Input leakage currents include high-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Refer to PCI spec.
3. Inputs are not "5-volt safe."
4. $I_{IL}$ may be changed on IC and ID pins (up to 200 µA) if pulled against internal pull-downs. Refer to the pin descriptions.

## Reset Operations

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PLPH}$ | $\overline{RST}$ Pulse Low Time (If $\overline{RST}$ is tied to $V_{CC}$, this specification is not applicable.) | 100 | | ns |
| $t_{PLRH}$ | $\overline{RST}$ Low to Reset during Sector Erase or Program$^{(1)(2)}$ | | 20 | µs |

Notes: 1. If $\overline{RST}$ is asserted when the WSM is not busy (RY/$\overline{BY}$ = 1), the reset will complete within 100 ns.
2. A reset time, $t_{PHAV}$, is required from the latter of RY/$\overline{BY}$ or $\overline{RST}$ going high until outputs are valid.

## AC Waveforms for Reset Operations

## A/A Mux Read-only Operations[1][2][3]

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| $t_{AVAV}$ | Read Cycle Time | 250 | | ns |
| $t_{AVCL}$ | Row Address Setup to R/$\overline{C}$ Low | 50 | | ns |
| $t_{CLAX}$ | Row Address Hold from R/$\overline{C}$ Low | 50 | | ns |
| $t_{AVCH}$ | Column Address Setup to R/$\overline{C}$ High | 50 | | ns |
| $t_{CHAX}$ | Column Address Hold from R/$\overline{C}$ High | 50 | | ns |
| $t_{CHQV}$ | R/$\overline{C}$ High to Output Delay[2] | | 150 | ns |
| $t_{GLQV}$ | $\overline{OE}$ Low to Output Delay[2] | | 50 | ns |
| $t_{PHAV}$ | $\overline{RST}$ High to Row Address Setup | 1 | | µs |
| $t_{GLQX}$ | $\overline{OE}$ Low to Output in Low-Z | 0 | | ns |
| $t_{GHQZ}$ | $\overline{OE}$ High to Output in High-Z | | 50 | ns |
| $t_{QXGH}$ | Output Hold from $\overline{OE}$ High | 0 | | ns |

Notes: 1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. $\overline{OE}$ may be delayed up to $t_{CHQV}$ - $t_{GLQV}$ after the rising edge of R/$\overline{C}$ without impact on $t_{CHQV}$.
3. $T_C = 0°$C to +85$°$C, 3.3V ± 0.3V $V_{CC}$.

## A/A Mux Read Timing Diagram
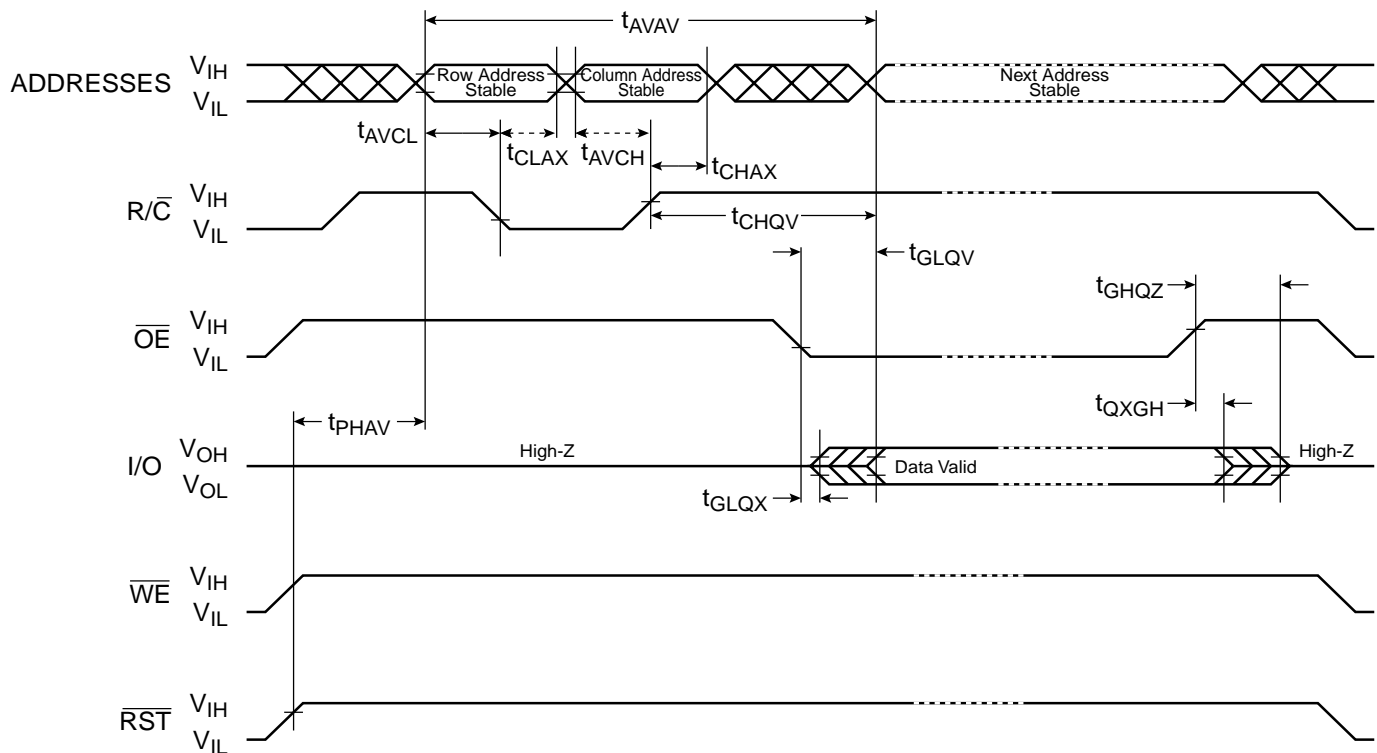
## A/A Mux Write Operations[1][2]

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{PHWL}$ | $\overline{RP}$ High Recovery to $\overline{WE}$ Low | 1 | | µs |
| $t_{WLWH}$ | Write Pulse Width Low | 100 | | ns |
| $t_{DVWH}$ | Data Setup to $\overline{WE}$ High[1] | 50 | | ns |
| $t_{WHDX}$ | Data Hold from $\overline{WE}$ High[1] | 8 | | ns |
| $t_{AVCL}$ | Row Address Setup to R/$\overline{C}$ Low[1] | 50 | | ns |
| $t_{CLAX}$ | Row Address Hold from R/$\overline{C}$ Low[1] | 50 | | ns |
| $t_{AVCH}$ | Column Address Setup to R/$\overline{C}$ High[1] | 50 | | ns |
| $t_{CHAX}$ | Column Address Hold from R/$\overline{C}$ High[1] | 50 | | ns |
| $t_{WHWL}$ | Write Pulse Width High | 100 | | ns |
| $t_{CHWH}$ | R/$\overline{C}$ High Setup to $\overline{WE}$ High | 50 | | ns |
| $t_{VPWH}$ | $V_{PP1,2}$ Setup to $\overline{WE}$ High | 100 | | ns |
| $t_{WHGL}$ | Write Recovery before Read | | 150 | ns |
| $t_{WHRL}$ | $\overline{WE}$ High to RY/$\overline{BY}$ Going Low | 0 | | ns |
| $t_{QVVL}$ | $V_{PP1,2}$ Hold from Valid SRD, RY/$\overline{BY}$ High | 0 | | ns |

Notes: 1. Refer to "A/A Mux Read-only Operations" for valid $A_{IN}$ and $D_{IN}$ for sector erase or program, or other commands.
2. $T_C = 0° C$ to $+85° C$, 3.3V ± 0.3V $V_{CC}$.

## A/A Mux Write Timing Diagram
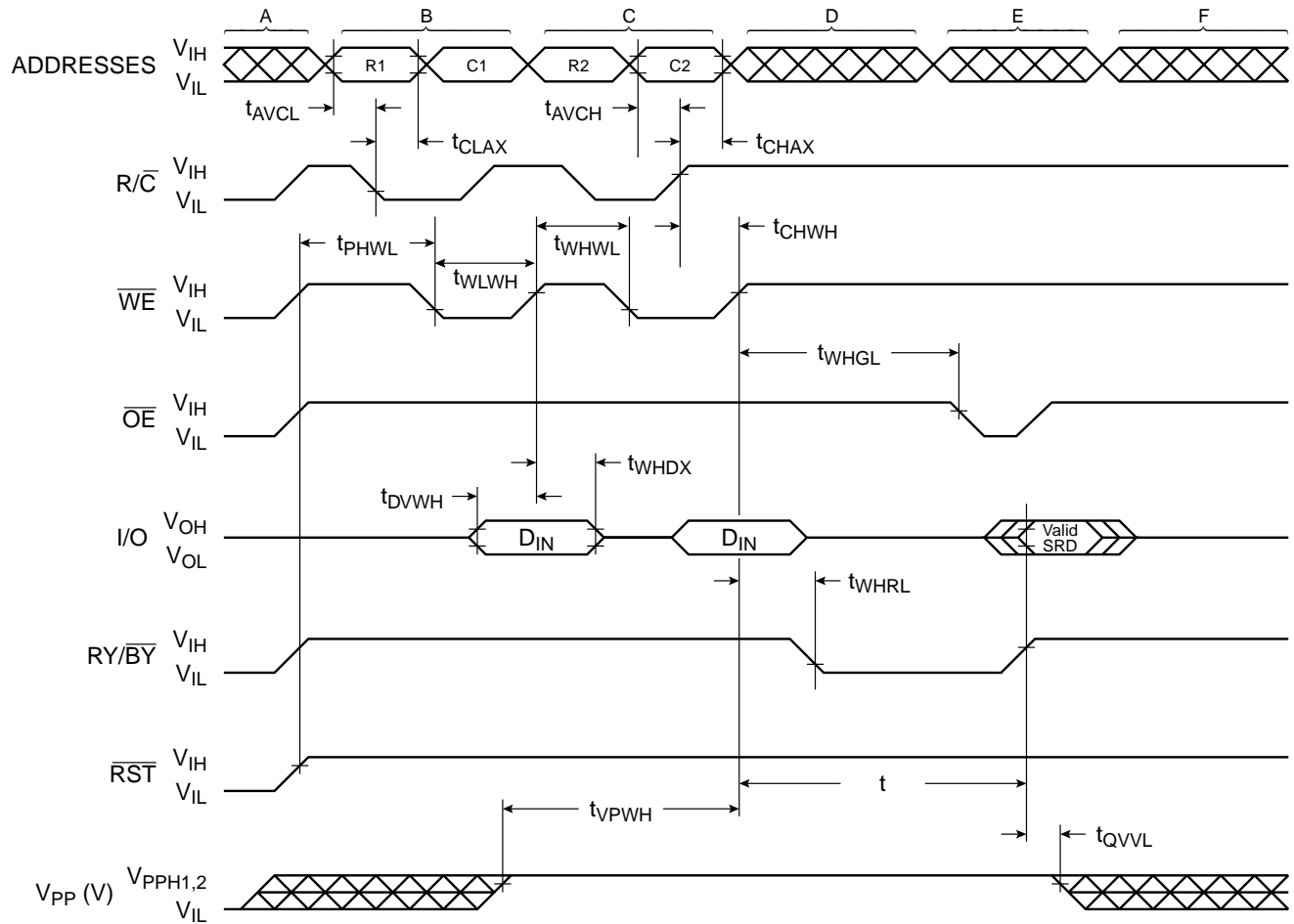


**NOTES**

A = $V_{CC}$ power-up and standby
B = Write sector erase or program setup
C = Write sector erase confirm or valid address and data
D = Automated erase or program delay
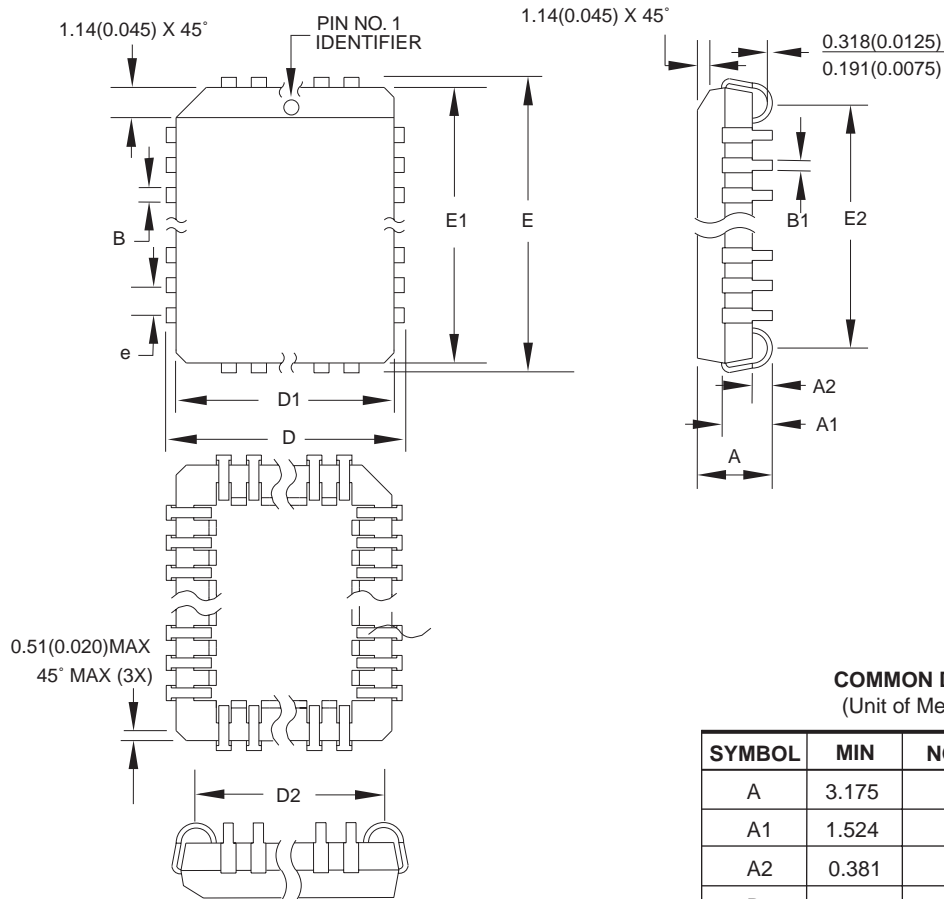E = Read status register data
F = Ready to write another command

## AT49LL080 Ordering Information

| $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| **Active** | **Standby** | | | |
| 67 | 0.10 | AT49LL080-33JC | 32J | Extended Commercial |
| | | AT49LL080-33TC | 40T | (0° to 85°C) |

| Package Type | |
|---|---|
| **32J** | 32-lead, Plastic J-leaded Chip Carrier Package (PLCC) |
| **40T** | 40-lead, Plastic Thin Small Outline Package, Type I (TSOP) |

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# Packaging Information

## 32J – PLCC

1.14(0.045) X 45˚

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45˚

0.318(0.0125)
0.191(0.0075)

B1  E2

B

E1  E

e

A2

A1

D1

A

D

0.51(0.020)MAX
45˚ MAX (3X)

D2

Notes:  1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion.
Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
and E1 include mold mismatch and are measured at the extreme
material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----|-----|-----|------|
| A | 3.175 | – | 3.556 | |
| A1 | 1.524 | – | 2.413 | |
| A2 | 0.381 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.354 | – | 11.506 | Note 2 |
| D2 | 9.906 | – | 10.922 | |
| E | 14.859 | – | 15.113 | |
| E1 | 13.894 | – | 14.046 | Note 2 |
| E2 | 12.471 | – | 13.487 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| **ATMEL** 2325 Orchard Parkway San Jose, CA  95131 | **32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC) | 32J | B |

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## 40T – TSOP, Type I

PIN 1

Pin 1 Identifier

0º ~ 8º

c

D1  D

L

L1

e     b

E     A2   A

A1

SEATING PLANE — GAGE PLANE

Notes:  1. This package conforms to JEDEC reference MO-142, Variation CD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.
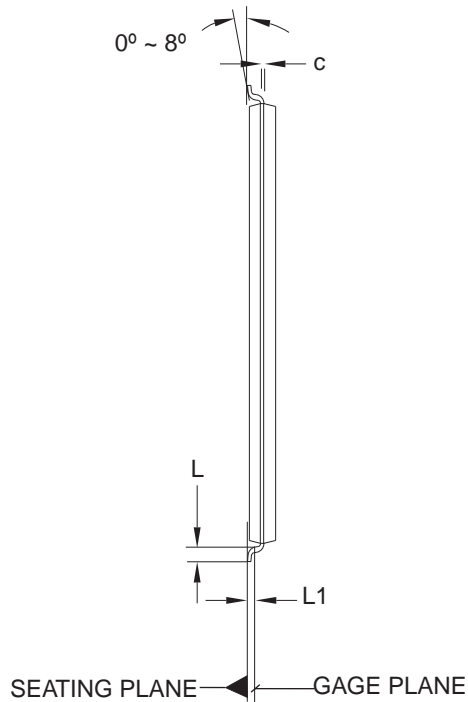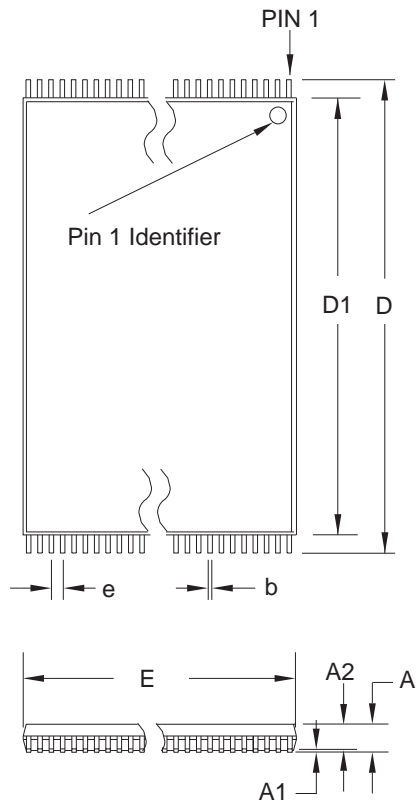
**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 9.90 | 10.00 | 10.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

10/18/01

| | | TITLE | DRAWING NO. | REV. |
|---|---|---|---|---|
| **AImEl** | 2325 Orchard Parkway San Jose, CA 95131 | **40T**, 40-lead (10 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP) | 40T | B |

3273C–FLASH–5/03

![ATMEL logo]

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