

Features and Benefits

Dual low noise, low offset, fully programmable amplifier chain
 12 bit on-chip ADC
 Powerful signal conditioning and linearisation unit
 Multiple output options: 12 bit digital through SPI, 8 bit resolution analog linear signal outputs or 10 bit PWM, both for ambient and object temperature.
 On-chip programmable digital moving average LPF for ultimate low noise performance
 ISP I/O-configuration and analog settings, accessible by SPI serial interface.
 Wide supply voltage range from 4.5V-80V

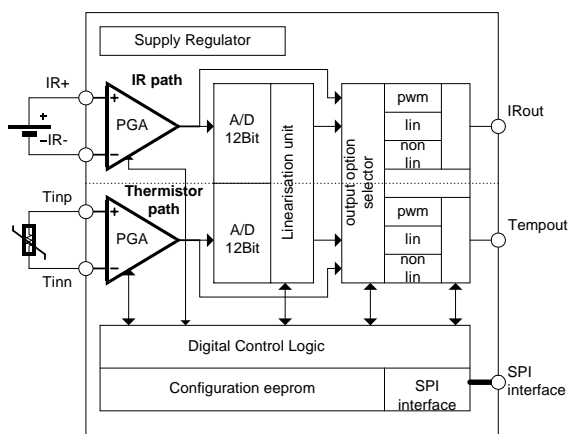
Applications

Thermopile + thermistor amplification chain
 Digital or analog, linear, ambient-compensated IR sensor interface
 General purpose programmable sensor amplifier/ signal conditioner

Ordering Information

| | | | |
|----------|--------------------|---------|-------------------------|
| Part No. | Temperature Suffix | Package | Temperature Range |
| MLX90313 | K | DF | -40C to 125C Automotive |

Functional Diagram



Description

The MLX90313 is a versatile in-circuit programmable interface, which performs signal conditioning, linearisation and ambient temperature compensation, particularly for infrared sensors combined with a thermistor. Other types of sensors can also be used in various configurations. Sensors that can be used include pressure sensors, strain gauges, acceleration sensors etc.

The amplifier chains in MLX90313 are programmable in very broad ranges of gain. Both chains consist of high performance, chopper-stabilized amplifiers, providing excellent noise performance and low offset. The I/O configuration as well as analog settings are in-circuit programmable by means of the SPI-serial interface. This serial link can also be used to read out the output signals digitally. The circuit can either provide linear analog or PWM (Pulse Width Modulated) signal outputs. Additionally, the circuit can perform simple control applications using on-board comparators.

MLX90313 Electrical Specifications

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{DD} = 4.5\text{V}$ to 80V (unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|------------------|--------------------------------|-----|-------|-----|----------------|
| Regulator and consumption | | | | | | |
| Supply voltage range | Vin1 | VDD1 | 7 | | 80 | V |
| Supply voltage range | Vin | VDD | 4.5 | 5 | 5.5 | V |
| Supply current | I _{dd} | @ $T_A=25^{\circ}\text{C}$ | | 5 | 5.6 | mA |
| Regulated supply voltage | V _{reg} | VDD, 10 μF ext. cap | 4.7 | 5 | 5.3 | V |
| Regulated voltage temperature coefficient | TC _{vr} | | | -2.35 | | mV/ $^{\circ}$ |
| POR threshold voltage | V _{por} | | 1.1 | 1.3 | 1.5 | V |

Band-gap reference

| | | | | | | |
|---|-------------------|--|-----|-----|-----|------------------------|
| Analog ground voltage | A _{gnd} | | 2.3 | 2.5 | 2.7 | V |
| Analog ground thermal coefficient | TC _{bg} | | | 15 | 50 | $\mu\text{V}/^{\circ}$ |
| Reference current mirror load drive voltage | V _{cref} | | 1.8 | 2 | 2.2 | V |

IR-chain amplifier and output driver

| | | | | | | |
|---------------------------------------|------------------------|--|------|-----|----------------------|------------------------|
| Common mode input range | CMIR | | -0.1 | | V _{dd} -3 | V |
| Common mode rejection ratio | CMRR | $f \leq 100\text{kHz}$ $R_{\text{sens}} < 60\text{k}\Omega^*$ | 75 | | | dB |
| Power supply rejection ratio | PSSR | $f \leq 100\text{kHz}$ | 75 | | | dB |
| Available gain settings | Air | | 55 | | 5500 | V/V |
| Gain tolerance | δG_{ir} | | -6.5 | | +6.5 | % |
| Amplifier offset | V _{off} | | | | 4 | μV |
| Input referred white noise | V _{nir} | rms-value | | | 25 | nV/ $\sqrt{\text{Hz}}$ |
| Chopper frequency | f _c | | | 8 | | KHz |
| Output voltage range | | I _{ROUT} | 0 | | V _{dd} -0.2 | V |
| Output source current | I _{od} | I _{ROUT} | 1 | | | mA |
| Output sink current | I _{os} | I _{ROUT} | 20 | | | μA |
| DC Output impedance, drive | r _{od} | I _{ROUT} | | | 10 | Ω |
| DC Output impedance, sink | r _{os} | I _{ROUT} | | | 100 | Ω |
| Capacitive load I _{ROUT} pin | C _{max} | I _{ROUT} | | | 50 | pF |
| Amplifier bandwidth | BW | | | 500 | | Hz |

Temp-chain amplifier and output driver

| | | | | | | |
|------------------------------|-------------------|------------------------|-----|--|---------------------|---------------------|
| Common mode input range | CMIR | | 0.1 | | V _{dd} -3V | V |
| Common mode rejection ratio | CMRR | $f \leq 100\text{kHz}$ | 75 | | | dB |
| Power supply rejection ratio | PSSR | $f \leq 100\text{kHz}$ | 75 | | | dB |
| TINP bias current | I _{tpb} | bias current enabled | 1/7 | | .1 | i _{Cref} * |
| Available gain settings | A _{temp} | | 1 | | 40 | V/V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------------------------|-------------------|----------------------|------|-----|---------|-----------------|
| Gain tolerance | δG_{temp} | bias current enabled | -6.5 | | +6.5 | % |
| Amplifier offset | Voff | | | | 4 | μV |
| Input referred white noise | Vtemp | rms-value | | | 400 | nV/ \sqrt{Hz} |
| Chopper frequency | fc | | | 8 | | kHz |
| Output voltage range | ORtemp | TEMPOUT | 0 | | Vdd-0.2 | V |
| Output source current | Iod | TEMPOUT | 1 | | | mA |
| Output sink current | Ios | TEMPOUT | 20 | | | μA |
| DC Output impedance, drive | rod | TEMPOUT | | | 10 | Ω |
| DC Output impedance, sink | ros | TEMPOUT | | | 100 | Ω |
| Capacitive load TEMPOUT pin | Cmax | TEMPOUT | | | 50 | pF |
| Amplifier bandwidth | BW | | | 500 | | Hz |

Rel1 open drain relay driver

| | | | | | | |
|-------------------------|----|--|----|----|--|----------|
| High voltage protection | | | 32 | | | V |
| output impedance | Ro | | | 10 | | Ω |

Comp1 comparator

| | | | | | | |
|---------------------------|---------|-------|---|--|-----|------------|
| Potentiometer input range | IRirout | IROUT | 0 | | 100 | % of Vrefp |
|---------------------------|---------|-------|---|--|-----|------------|

ADC

| | | | | | | |
|-----------------------------|---------|------------|----------------------|-----|------|---------|
| Input stage gain | | | 2.95 | 3 | 3.05 | V/V |
| External Reference voltage | Vrefpex | | 1 | | 3.3 | V |
| Internal Reference voltage | Vrefp | | 2.4 | 2.5 | 2.6 | V |
| Vrefp input leakage current | Ilvrefp | @150°C | | | 5 | μA |
| Resolution | | | | 12 | | bit |
| Monotonicity | | | guaranteed by design | | | |
| Differential non-linearity | DNL | | | | 0.4 | LSB |
| Integral non-linearity | INL | | | | 1/2 | LSB |
| Gain error | | full scale | | | 1 | LSB |
| Total input-referred noise | | Vref=3V | | | 0.2 | LSB |

DAC

| | | | | | | |
|----------------------------|-----|--|----------------------|---|-----|-----|
| Resolution | | | | 8 | | bit |
| Monotonicity | | | guaranteed by design | | | |
| Differential non-linearity | DNL | | | | 1/2 | LSB |
| Integral non-linearity | INL | | | | 1/2 | LSB |

*Rsens is the impedance of the sensor connected between IRINP and IRINN for the IR-chain amplifier.

**Icref is the current flowing out of pin CREF

General Description

The MLX90313 is a versatile in-circuit programmable interface, which performs signal conditioning, linearisation and ambient temperature compensation, particularly for infrared sensors combined with a thermistor. Other types of sensors can also be used in various configurations. Sensors that can be used include pressure sensors, strain gauges, acceleration sensors etc.

The amplifier chains in MLX90313 are programmable in very broad ranges of gain, between 50 and 12000 for the IR-chain and between 1 and 120 for the Temp-chain. Both chains consist of high performance, chopper-stabilized amplifiers, providing excellent noise performance and low offset. The I/O configuration as well as analog settings are in-circuit programmable by means of the SPI-serial interface. This serial link can also be used to read out the output signals digitally. The circuit can either provide linear analog or PWM (Pulse Width Modulated) signal outputs, relative to an analog ground, or several combinations of analog and digital comparator driven outputs. Two comparators controlled by either one of the two linearised signals are available on chip with different possibilities for the threshold level, polarity and switching hysteresis. One of the comparators drives the open drain output. The user can provide the threshold for this comparator at the IROUT I/O pin with a simple potentiometer.

A bias current for the thermistor can be obtained at the TINP input by connecting an external resistor between the CREF pin and VSS. The standard package is SOIC-20.

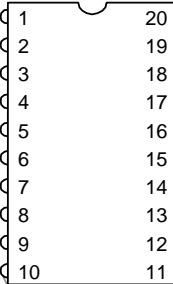
Unique Features

The MLX90313 integrates dual low noise programmable gain amplifier stages. Both thermistor and IR signal path can be configured to suit a large number of components and applications. The onboard analog to digital converter (ADC) combined with the digital linearisation unit results in linear output signals. These output signals are available as analog or digital output signal. Applications requiring digital temperature information can use single wire PWM output or SPI serial communication. The complete configuration and calibration is in-system programmable through the SPI interface. Combination of all these integrated features combined with a thermopile sensor make the MLX90313 a true high accuracy automotive grade single-chip infrared thermometer.

Absolute Maximum Ratings

| | |
|---|---------------|
| Supply Voltage, V_{in1} (overvoltage) | 80V |
| Supply Voltage, V_{in} (overvoltage) | 6V |
| Supply Voltage, V_{in1} (operating) | 16V |
| Supply Voltage, V_{in} (operating) | 5.5V |
| Reverse Voltage Protection | -5V |
| Supply Current, I_{DD} | 5.6 mA |
| Output Current, I_{OUT} | 3 mA |
| Operating Temperature Range, T_A | -40C to +125C |
| Operating Temperature Range, T_S | -55C to +150C |
| ESD Susceptibility | 2 kV |
| Rel1 output impedance | 10 ohms |

Pin-out



| | | | |
|-------|----|----|---------|
| TINP | 1 | 20 | TEMPOUT |
| TINN | 2 | 19 | CSB |
| IRINP | 3 | 18 | SDOUT |
| IRINN | 4 | 17 | SCLK |
| VSS | 5 | 16 | TSTCLK |
| REL1 | 6 | 15 | VDD |
| IROUT | 7 | 14 | VDD1 |
| SDIN | 8 | 13 | AGND |
| TOUT1 | 9 | 12 | VREFP |
| TOUT2 | 10 | 11 | CREF |

| Pin | Symbol | Description |
|-----|---------|---|
| 1 | TINP | Temp-chain amplifier positive input |
| 2 | TINN | Temp-chain amplifier negative input |
| 3 | IRINP | IR-chain amplifier positive input |
| 4 | IRINN | IR-chain amplifier negative input |
| 5 | VSS | Supply pin |
| 6 | REL1 | Open-drain relay driver output |
| 7 | IROUT | IR-chain amplifier output |
| 8 | SDIN | SPI data input |
| 9 | TOUT1 | Test pin/ Oscillator output |
| 10 | TOUT2 | Test pin, leave open |
| 11 | CREF | Bias current reference |
| 12 | VREFP | Reference voltage input/output |
| 13 | AGND | Analog ground, band-gap reference voltage |
| 14 | VDD1 | Automotive Ignition supply pin |
| 15 | VDD | Regulated supply pin |
| 16 | TSTCLK | Clock for test mode; leave open |
| 17 | SCLK | SPI clock input |
| 18 | SDOUT | SPI data output |
| 19 | CSB | SPI chip select active low |
| 20 | TEMPOUT | Temp-chain amplifier output |

Pin Descriptions

TINP

Temperature sensor positive input pin. The pin connects to the temp-chain amplifier and the on-chip biasing current source. The source is a mirrored version of the current running into CREF with programmable ratio. The current source can be switched off for use of external current biasing.

TINN

Temperature sensor negative input.

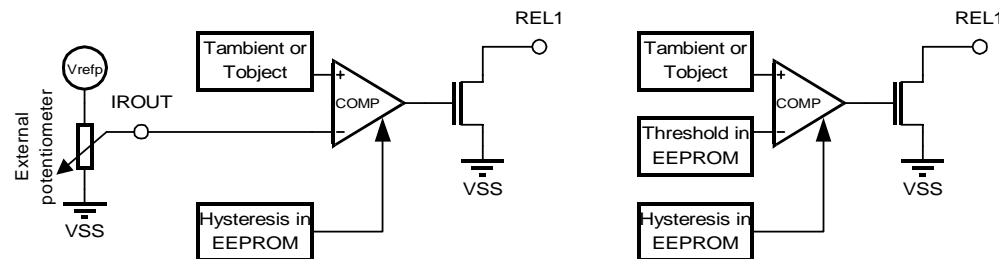
IRINP - IRINN

Thermopile sensor input pins.

VSS: Supply pin

REL1

Open drain relay driver output. The typical on-resistance of this driver is $<10\Omega$ with a supply voltage of $VDD=5V$. Different configurations are possible as shown below.



The comparator is a 12 bit digital comparator. The input polarity can be inverted or not. The threshold and hysteresis registers are 16 bit registers of which the 11 MSBs are used in the comparator circuitry. The voltage on the IROUT pin is sampled with 8 bit ADC referred between VREFP and VSS pins. Note. In case of potentiometer use the linearised analog output is not available. In this case the DAC is used as 8-Bit ADC for potentiometer (or other voltage source) monitoring.

IROUT

IROUT/POTin analog/digital I/O pin. This pin can be configured as analog output of the IR sensor or as input for an external potentiometer. (see pin description of REL1). As analog output, this pin can either be connected to the analog amplified IR sensor signal or to the linearised object temperature by means of the DAC. The driver can source at least 1mA and sink at least 20 μ A to/from an external load. If the capacitive load on this pin exceeds 50pF, this load should be de-coupled by means of a series resistor. This pin can be configured also as digital output to transmit the IR temperature in PWM format. The pin is protected for over-voltage and can withstand 16V.

SDIN

Serial data input pin for the SPI. Data is accepted on the rising edge of the serial data clock (SCLK)

SDOUT

Serial data output pin for the SPI. Data is valid on the rising edge of the serial data clock (SCLK)

SCLK

Serial data clock from the external master to be supplied to this pin. Maximum frequency = 125kHz.

CSB

Active low, chip select pin for the SPI. Communication is started on the falling edge of CS and ended on the rising edge of CS.

TOUT1 - TOUT2:

Test pins. In normal mode, the internal clock signal of 1Mhz is present on TOUT1 and the clock of the chopper amplifier is present on TOUT2.

CREF

Current reference output. CREF is the reference voltage output for the temperature independent current source. The requirements for the resistor to be connected between CREF and VSS depend on the required accuracy and range of the ambient temperature measurement. The voltage level at CREF depends directly on the internal band-gap.

VREFP

Voltage reference I/O pin. This level is by default dependent on the on-chip band-gap reference source and can be programmed in range 2-4.5V from eeprom . This voltage is used as reference for the DAC, external applied potentiometer and 8-bit ADC. The chip can be configured to use an external reference voltage instead of the on-chip reference.

The pin is protected from over-voltage and can withstand 16V

AGND

Analog ground reference pin. This voltage is derived from the on-chip band-gap and has a typical level of 2.5V for maximum output range of the amplifiers. When IROUT and/or TEMPOUT are connected directly to the amplified analog signals, then these signals are referred to AGND. The regulator can be stopped from the eeprom configuration register. In this case the pin can be used for external reference for the 12-bit ADC.

The pin is protected from over voltage and can withstand 16V

VDD1

High voltage supply pin. This supply pin can be connected directly to an automotive ignition supply voltage. The internal regulator can operate with voltages between 7V and 80V.

VDD

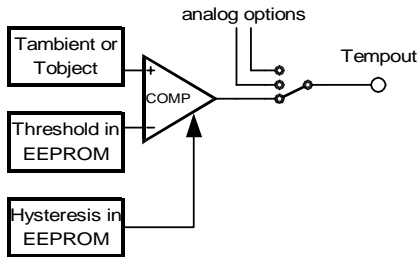
5V regulated supply pin. The 5V regulated voltage from the on-chip regulator is available on this pin. The internal regulator can supply up to 20mA to external circuitry. VDD can also be used to supply the chip directly with an external 5V regulated supply.

TEMPOUT

TEMPOUT analog output/Comparator output pin. This pin can be configured as analog output of the

temperature sensor or as output of the internal comparator circuit. As analog output, this pin can either be connected to the analog amplified temperature sensor signal or to the linearised ambient temperature by means of the DAC.

When used as comparator output, different configurations are possible as shown below.



The driver can source at least 1mA and sink at least 20 μ A to an external load. If the capacitive load on this pin exceeds 50pF, the load should be de-coupled by means of a series resistor. The pin is also output for linearised Tambient in PWM mode. The pin is protected from over-voltage and can withstand 16V

Analog Section

Supply regulator and Power-ON Reset

The on-chip supply regulator and can be powered by an automotive ignition supply line (7V-80V). The chip can withstand SAE standard ignition transients. The resulting voltage of the regulator is available on VDD (5V±300mV). The VDD pin can source up to 20mA to external circuitry. The chip can also be supplied directly with a 5V regulated supply on pin VDD.

The power-on reset (POR) circuitry is completely internal. The chip is fully operational 16ms from the time the supply crosses 1.3V. The POR circuit will issue another POR if the supply voltage goes below 1.3V.

Band-gap, DAC and ADC references

The on-chip trimmable, curvature compensated band-gap circuitry provides a stable reference level (less than 10ppm per °C) for several derived reference potentials used for normal operation in MLX90313.

The analog ground at the AGND pin is directly derived from this band-gap voltage. The output voltages from both amplifier chains are relative to this potential. The AGND reference can be trimmed internally to (2.5V±20mV). The regulator at AGND pin can be switched off to minimize the current consumption. The pin can be also used as external input for the internal 12-bit ADC.

The reference voltages for ADC and DAC are also derived from the band-gap. The DAC reference is available at pin VREFP. The MLX90313 DAC reference voltage can be programmed on chip to one of the following values: 2, 2.5, 3, 3.5, 4 and 4.5 V. Depending on the customer application Melexis can program the linearised analog outputs for object and ambient temperatures providing absolute voltage/temperature dependence. The internal regulator for the DAC reference voltage can be switched off to minimize the consumption (if linearised analog output is not in use) or to use externally supplied reference for DAC reference in range 2 to 5V

The ADC reference is 2.5V typically. The chip can be also programmed to use external ADC reference connected to pin AGND. The current reference bias voltage (present at CREF pin) is also derived from the on-chip band-gap reference.

IR-amplifier chain

MLX90313 is available with gain settings for the IR-amplifier chain ranging from 55 to 5500. The gain can be selected by setting the appropriate bits of the 'Irgain1'-register (EEPROM address 00h) according to the table below. Any gain between the abovementioned limits can be obtained within an accuracy of ±6.5%. The amplifier input-referred white noise level is below 23nVrms/√Hz. In the application with IR-sensors, with output resistance of 50kΩ typical, the total system noise will however depend mainly on the noise of the sensor and will rise up to 45nVrms/√Hz. The offset for the chopper stabilized amplifier path can be largely calibrated out and amounts to maximum 4μV.

The common mode input range of the amplifier is -100mV to VDD - 3V. The output range of the amplifier is 0V to VDD-0.2V. The output of the amplifier is referred to the potential on AGND.

IR chain gain settings

| $G_{IR} = G_{pr} \times G_b \times G_{pa} \times G_l$ | | | | | | | | | | | | |
|---|----------|-----|-------|------|------|-------|----------|---|-------|------|------|-------|
| stage | G_{pr} | | G_b | | | | G_{pa} | | G_l | | | |
| contr. bits | GCI0 | | GCI3 | GCI2 | GCI1 | | GCI4 | | GCI7 | GCI6 | GCI5 | |
| setting | 0 | 10 | 0 | X | X | 5 | 0 | 1 | 0 | 0 | 0 | 1.067 |
| | | | 1 | 0 | 0 | 10 | | | 0 | 0 | 1 | 1.143 |
| | | | 1 | 0 | 1 | 15 | | | 0 | 1 | 0 | 1.231 |
| | | | 1 | 1 | 0 | 20 | | | 0 | 1 | 1 | 1.333 |
| | 1 | 20* | 1 | 1 | 1 | 25 | 1 | 5 | 1 | 0 | 0 | 1.455 |
| | | | 1 | 0 | 1 | 1.600 | | | | | | |
| | | | 1 | 1 | 0 | 1.778 | | | | | | |
| | | | 1 | 1 | 1 | 2.000 | | | | | | |

* This option is available only if ENLN=1

The pin ENLN controls both the noise level and distortion of the amplifier. If ENLN=1 the noise of the amplifier is 23nVrms/√Hz, the gain of 20 in first stage is available but the input signal must be less than 4 mV for less than 0.05% full scale distortion.

If ENLN is 0 then the span of the input signal can be ± 40mV with distortion less than 0.1% full scale. In this case the noise floor of the amplification chain increases 3 times.

Temp-amplifier chain

MLX90313 is available with gain settings for the Temp-amplifier ranging from 5 to 50. The gain can be selected by setting the appropriate bits of the 'Temp gain and current control'-register (EEPROM address 02h) according to the table below. Any gain between the abovementioned limits can be obtained within an accuracy of ±6.5%. It is also possible to completely bypass the temperature amplifier and force the input signal directly to the ADC. The amplifier input-referred white noise level is below 400nVrms/√Hz. The common mode input range of the amplifier is -100mV to VDD-3V. The output range of the amplifier is 0V to VDD-0.2V. The output of the amplifier is referred to the potential on AGND.

Temp chain gain settings

| $G_T = G_{pr} \times G_l \times M$ | | | | | | | | | | | | |
|------------------------------------|----------|------|------|----|-------|------|------|-------|--------|--------|--------|-----|
| stage | G_{pr} | | | | G_l | | | | M | | | |
| contr. bits | GCT2 | GCT1 | GCT0 | | GCT5 | GCT4 | GCT3 | | IRSEL2 | IRSEL1 | IRSEL0 | |
| | 0 | 0 | 0 | 1 | X | X | X | | | | | |
| settin g | 0 | 1 | 1 | 5 | 0 | 0 | 0 | 1.067 | 0 | 0 | 0 | off |
| | | | | | 0 | 0 | 1 | 1.143 | 0 | 0 | 1 | 1/7 |
| | 1 | 0 | 0 | 10 | 0 | 1 | 0 | 1.231 | 0 | 1 | 0 | 2/7 |
| | 1 | 0 | 1 | 15 | 0 | 1 | 1 | 1.333 | 0 | 1 | 1 | 3/7 |
| | 1 | 1 | 0 | 20 | 1 | 0 | 0 | 1.455 | 1 | 0 | 0 | 4/7 |
| | | | | | 1 | 0 | 1 | 1.600 | 1 | 0 | 1 | 5/7 |
| | 1 | 1 | 1 | 25 | 1 | 1 | 0 | 1.778 | 1 | 1 | 0 | 6/7 |
| | | | | | 1 | 1 | 1 | 2.000 | 1 | 1 | 1 | 1 |

Note: When the current mirror is on (all settings except IRSEL[2:0] = 000b) the gain is defined as follows:

$$G_T = \frac{V_{out}}{R_{sens} \cdot I_{cref}}$$

where Vout is the output of the analog amplifier chain, Rsens is the resistance of the sensor connected between TINP and TINN and Icref is the current out of CREF.

When the current mirror is off (IRSEL[2:0]=000b), M should be replaced by 1 and the gain is defined as follows:

$$G_T = \frac{V_{out}}{V_{in}}$$

where Vin is the voltage difference between TINP and TINN

If GCT[2:0]=0 then the temp chain will be completely off, the Timp pin will be connected directly to the ADC input, providing Gain=1

Current Reference

The thermistor (or sensor) connected to TINP must be biased with a current source. This bias current is mirrored from the current through the external resistor between CREF and VSS. The voltage maintained at the CREF pin is derived from internal band-gap voltage, and thus constant. The typical value of the voltage at CREF pin is 2V.

The current mirror ratio can be set between 1/7 and 1 according to the table for the Temp-chain gain settings. The setting with IRSEL[2:0]=000b switches the current mirror off. In this case the thermistor must be biased by external circuitry.

Analog-to-Digital Converter (ADC)

MLX90313 contains a 12-bit internal analog to digital converter. Real 12 bit conversion is achieved by a fully differential signal path of the converter. The input amplifier of the ADC has a fixed gain of 3. Automatic calibration is implemented in the background, which allows precise conversion in a very wide temperature range. The ADC sampling rate is 7k samples/second. The reference voltage for the ADC is normally a scaled version of the internal band-gap reference and is fixed to be 2.5V. Alternatively MLX90313 can be configured to work with an external reference potential applied to the AGND pin. In this case the appropriate bit in the configuration register (SELADREF bit in Confreg1) must be cleared. Internal ADC can work with references down to 1 V keeping the 12-bit resolution.

The ADC contains an interface circuit to scale and offset the analog signals in order to make the most efficient use of the available resolution. After amplification the IR and Temp sensor signals are referred to AGND voltage level (typical value 2.5V). The additional offset is scaled version of the AGND.

The ADC interface circuit is given below. The output of the Temp-chain is amplified relative to the voltage reference VrefT, which can be controlled with 2 bits (bit10 and bit9, EEPROM address 02h). The possible values for VrefT can be calculated according to the equation:

$$V_{refT} = \frac{V_{Agnd} \times 1.4 \times (63 + K)}{70}, \text{ where } K = 0 \text{ to } 3, \text{ corresponding to the value of the control bits.}$$

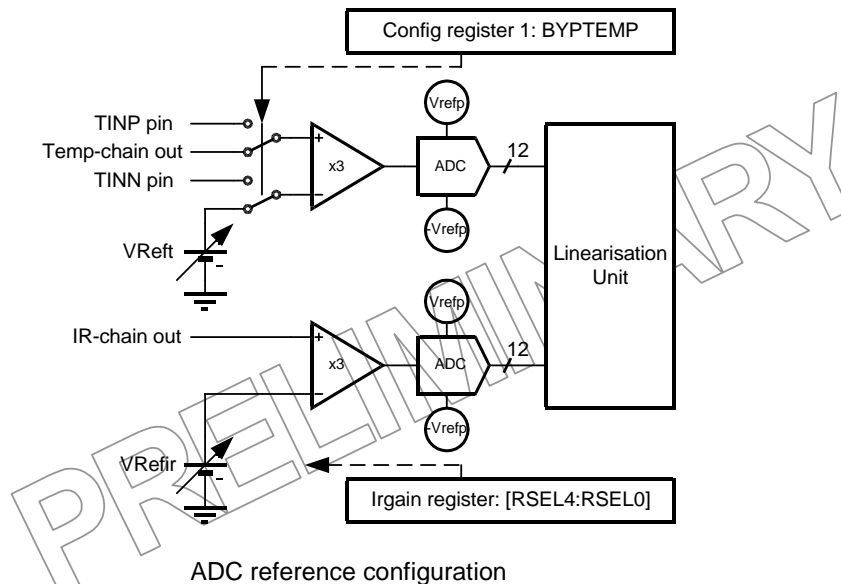
The typical values are 3.15, 3.20, 3.25 and 3.3V. If the temp path amplifier is bypassed then VrefT will be fixed to: $A_{gnd} \times 0.28 = 0.7V$ typical.

The output of the IR-chain is amplified relative to Refir and can be calculated according to the following equation:

$$V_{refir} = \frac{V_{Agnd} \times 1.4 \times (34 + K)}{70}, \text{ Where } K=0:31 \text{ depending on the selected value of Rsel}[4:0]$$

The typical values (for Agnd=2.5V) are listed in the table below:

| ADC interface setting | | | | | | | |
|-----------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| RSEL[4:0] | Refir [V] | RSEL[4:0] | Refir [V] | RSEL[4:0] | Refir [V] | RSEL[4:0] | Refir [V] |
| 11111b | 3.25 | 10111b | 2.85 | 01111b | 2.45 | 00111b | 2.05 |
| 11110b | 3.20 | 10110b | 2.80 | 01110b | 2.40 | 00110b | 2.00 |
| 11101b | 3.15 | 10101b | 2.75 | 01101b | 2.35 | 00101b | 1.95 |
| 11100b | 3.10 | 10100b | 2.70 | 01100b | 2.30 | 00100b | 1.90 |
| 11011b | 3.05 | 10011b | 2.65 | 01011b | 2.25 | 00011b | 1.85 |
| 11010b | 3.00 | 10010b | 2.60 | 01010b | 2.20 | 00010b | 1.80 |
| 11001b | 2.95 | 10001b | 2.55 | 01001b | 2.15 | 00001b | 1.75 |
| 11000b | 2.90 | 10000b | 2.50 | 01000b | 2.10 | 00000b | 1.70 |



Digital-to-Analog Converter (DAC)

A 8 bit digital to analog converter can be used to output the data for the linearised Tobject- and Tambient signals. The DAC can work with a internal programmable reference voltage, as well as with an external one. In case the internal reference voltage is used, this voltage can be monitored on the VREFP pin. If one wants to use his own reference voltage, this can be done by applying this voltage to the VREFP pin, and setting the appropriate configuration bit.

The result from D/A conversion is stored on hold capacitors and buffered. The signals are available at IROUT and TEMPOUT respectively, if the appropriate bits are set in the configuration register (EEPROM address 04h).

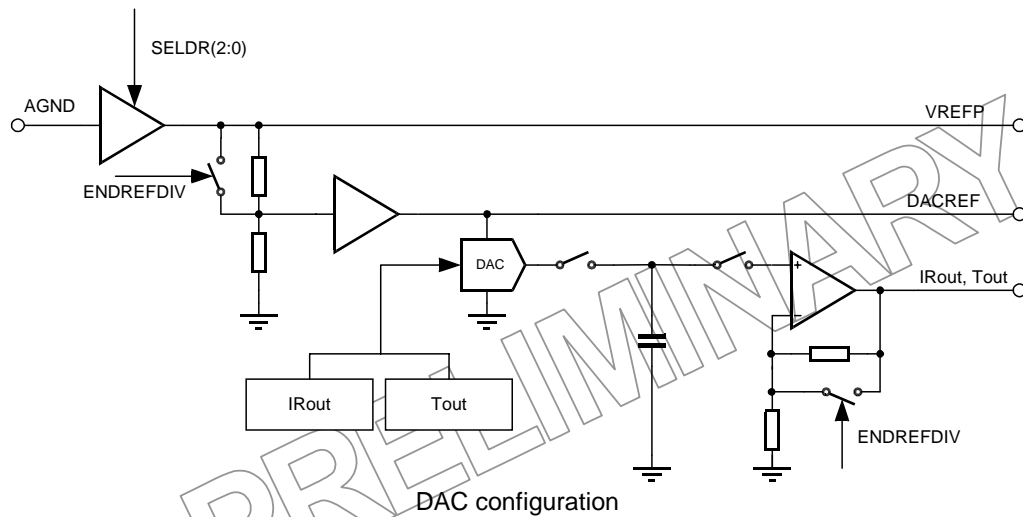
The reference value for the D/A can be programmed with 3 bits: SELDR[2:0] (register Irgain2) according to the table below:

| SELDR2 | SELDR1 | SELDR0 | ENDREFDIV | VREFP |
|--------|--------|--------|-----------|-------|
| 0 | 0 | 0 | 0 | 2 |
| 0 | 0 | 1 | 0 | 2.5 |
| 0 | 1 | 0 | 0 | 3 |
| 0 | 1 | 1 | 1 | 3.5 |
| 1 | 0 | 0 | 1 | 4 |
| 1 | 0 | 1 | 1 | 4.5 |

For reference voltages higher than 3V the ENDREFDIV bit must be set. In this case the ASIC will divide internally the reference by 2 to provide proper input common mode for the output buffer amplifiers at pins IROUT and TEMPOUT. In this case the result of the D/A conversion result will be amplified times 2 by the output amplifiers, which will ensure the requested signal swing.

Melexis can rescale the DAC reference and eeprom table for the linearisation unit to provide absolute analog output. This way, at maximum calibrated temperature, the voltage of IROUT or TEMPOUT pin will always correspond to the requested D/A reference voltage.

The regulator for the VREFP voltage can be stopped and an external reference voltage can be forced and used from the D/A. The regulator for DAC reference voltage can also be stopped (bit ENDACREF=0) when DAC is not in use. This will save some supply current.



Output drivers

The IROUT and TEMPOUT outputs can be connected to various signals available: The amplified analog signals (IRINP-IRINN and TINP-TINN), the linearised object respectively ambient temperature signals, or to the comparator circuitry. The IROUT and TEMPOUT pin drivers can source 1mA and sink 20µA and are reverse voltage protected down to -5V relative to VSS. The available configurations are described in table below.

| Input/Output Setting | | | | |
|----------------------|-------------|----------------------|------------|-----------------|
| I/O pin | IROUT | | TEMPOUT | |
| Control Bits | IROUTC[1:0] | Configuration | TOUTC[1:0] | Configuration |
| Setting | 00b | IR-chain out | 00b | Temp-chain out |
| | 01b | Linear Tobject | 01b | Linear Tambient |
| | 10b | Threshold Rel1 input | 10b | Comp1 out |
| | 11b | PWM out | 11b | PWM out |

REL1 is an open drain relay driver output controlled by the on-chip comparator circuitry. The available configurations are described in the section on the comparator circuitry.

Digital Section

The digital unit on board of MLX90313 realizes all functions for control, configuration, measurements and linearisation. It contains several registers, ALU and control logic. All functions of the ASIC are hardware fixed and controlled by different state machines, which execute in sequence all procedures necessary for normal chip operation.

Internal registers overview

The table below contains all internal registers, their addresses for access via SPI serial interface and short functional description. Depending on their function they can be divided in 3 groups:

- Control registers: they keep the configuration of the chip including all gain settings of the amplifiers, analog ground level, band-gap and oscillator trimming data, etc. All this data is stored in eeprom and after POR the system loads it in the corresponding peripheral registers.
- Data registers: they keep all data for offsets, results from measurements and linearisation of both chains. This registers can be read via spi in normal mode and are write accessible during test mode.
- Computation registers. These registers support the computation unit and keep all temporary data necessary for digital low pass filtering, linearisation and comparator functions. They are not accessible via SPI in normal mode.

| Internal Register Table. | | | | | |
|--------------------------|-----------------------------|---------|---------|----------------|--------|
| Register | Function | Address | | Access via spi | |
| | | Dec | Hex | Write | Read |
| IRGAIN1 | IR-chain settings | 0 | 00h | Test mode | No |
| IRGAIN2 | IR-chain settings | 1 | 01h | Test mode | No |
| TEMPGAIN | Temp-chain settings | 2 | 02h | Test mode | No |
| CONFREG1 | Configuration | 3 | 03h | Test mode | Always |
| CONFREG2 | Configuration | 4 | 04h | Test mode | Always |
| OSCILLATOR | Oscillator | 5 | 05h | Test mode | No |
| BGCONTROL | Bandgap control | 6 | 06h | Test mode | No |
| LPF | Low Pass Filter | 7 | 07h | Test mode | No |
| ADCREG | ADC output data | 8 | 08h | Test mode | Always |
| IROUT | Tobject (lin) | 9 | 09h | Test mode | Always |
| TOUT | Tambient (lin) | 10 | 0Ah | Test mode | Always |
| IRDATA | IR-chain output | 11 | 0Bh | Test mode | Always |
| TDATA | Temp-chain output | 12 | 0Ch | Test mode | Always |
| IROS | IR-chain offset | 13 | 0Dh | Test mode | Always |
| TOS | Temp-chain offset | 14 | 0Eh | Test mode | Always |
| MAINSTM | Main state machine | 15 | 0Fh | Test mode | No |
| TEST | Test mode control | 16 | 10h | Always | No |
| REG TEMP | Temporary register for test | | | Test mode | No |
| REG A | Accumulator A | | | Test mode | No |
| REG B | Accumulator B | | | Test mode | No |
| TESTCTRL 1 | Test control | 20 | 14h | Test mode | No |
| REG C | Accumulator C | | | Test mode | No |
| REG E | Accumulator E | | | Testmode | No |
| TESTCTRL 2 | ADC test control | 23 | 17h | Test mode | No |
| WP | Eeprom write protect | 24-31 | 18h-1Fh | Always | No |

Configuration and control registers overview and bit functions as they are read from the module

| Bit functions | | | | | | | | |
|----------------------------|--------------------|--------------------|-------------------|----------------------|-----------|-----------|----------|----------|
| REGISTERH REGISTERL | B15 B7 | B14 B6 | B13 B5 | B12 B4 | B11 B3 | B10 B2 | B9 B1 | B8 B0 |
| IRGAIN1H IRGAIN1L | ENDREFDIV GCI2 | ENDAC GCI1 | ENLN GCI0 | GCI7 | GCI6 | GCI5 | GCI4 | GCI3 |
| IRGAIN2H IRGAIN2L | AGNDC3 RSEL2 | AGNDC2 RSEL1 | AGNDC1 RSEL0 | AGNDC0 | SELDR2 | SELDR1 | SELDR0 | RSEL3 |
| TEMPGAINH TEMPGAINL | TRSEL1 GCT2 | TRSEL0 GCT1 | IRSEL2 GCT0 | IRSEL1 | IRSEL0 | GCT5 | GCT4 | GCT3 |
| CONFREG1H CONFREG1L | ERROR REL1V | ENVR REL1P | HVSUP EEWREN | SELADREF TESTMODE | POTMET | COMP1V | COMP1P | BYPTEMP |
| CONFREG0H CONFREG0L | IROUTC1 TIMEOS2 | IROUTC0 TIMEOS1 | TOUTC1 TIMEOS0 | TOUTC0 | SUBINC | SUBDEC | NTC | TIMEOS3 |
| OSCH OSCL | | | | | | | | ENAGNDB |
| BGH BGL | | | | | | | | |
| LPFH LPFL | RSEL4 LPFT2 | ENOSM LPFT1 | ENTAV LPFT0 | IROS | TOS | LPFIR2 | LPFIR1 | LPFIR0 |
| TESTH TESTL | 1 | 0 | 1 | 0 | 0 | 1 | | |
| TESTCTRL1H TESTCTRL1L | | | | | | | | |
| TESTCTRL 2H TESTCTRL 2L | | | | | | | | |
| WPH WPL | | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

Register Descriptions

IRGAIN1

Read access: No. The data is accessible for read via SPI only from eeprom address 00h.
Write access: Directly to the register in test mode. To eeprom if WP-register is correctly set.

| IRGAIN1 bit functions | | | |
|-----------------------|-----|-------------------|--|
| Name | POR | val | Function |
| ENDREFDIV | X | 1 | Divide the reference for the DAC and enable output amplification by 2 of the To and Ta outputs. Must be set for Vref=3.5V,4V,4.5V. |
| ENDAC | X | 1 | Enable the DAC regulator |
| ENLIN | X | 1 | Enable low noise. |
| GCI[7:0] | X | 00000000-11111111 | Control the gain of the IR amplifier chain (see 'IR amplifier chain') |

IRGAIN2

Read access: No. The data is accessible for read via SPI only from eeprom address 01h.
Write access: Directly to internal register in test mode. To EEprom if WP-register is correctly set.

| IRGAIN2 bit functions | | | |
|-----------------------|-----|-----------|----------------------------------|
| Bit | POR | val | Function |
| AGNDC [3:0] | X | 0000-1111 | Reserved |
| SELDR [2:0] | X | | Adjustment of the DAC reference. |
| | X | 000 | Vref = 2V |
| | X | 001 | Vref = 2.5V |
| | X | 010 | Vref = 3V |
| | X | 011 | Vref = 3.5V |

| IRGAIN2 bit functions | | | |
|-----------------------|-----|-----------|---|
| Bit | POR | val | Function |
| | X | 100 | Vref = 4V |
| | X | 101 | Vref = 4.5V |
| RSEL[3:0] | X | 0000-1111 | Select the value of the analog ground for IR signal path. The bits are 5, RSEL4 is in LPF register (see 'ADC' part) |

TEMPGAIN

Read access: No. The data is accessible for read via SPI only from eeprom address 02h.

Write access: Directly to internal register in test mode. To EEprom if WP-register is correctly set.

| TEMPGAIN bit functions | | | |
|------------------------|-----|---------------|--|
| Bit | POR | val | Function |
| TRSEL[1:0] | X | 00-11 | Reference voltage for Tambient measurement at ADC interface input. |
| IRSEL[2:0] | X | 000-111 | Current mirror ratio: See under M in table 'Temp chain gain settings' in the section on the Temp-amplifier chain (analog features) |
| GCT[5:0] | X | 000000-111111 | Temp-gain: See table 'Temp-chain gain settings' in the section on the temp-amplifier chain (analog features) |

CONFREG1

Read access: Directly from internal registers or EEprom.

Write access: Directly to internal register in test mode. To EEprom if WP-register is correctly set.

| CONFREG1 bit functions | | | |
|------------------------|-----|-----|--|
| Bit | POR | val | Function |
| Fatal Error | X | 1 | Flags Multiple eeprom failure. Hamming coding can detect and correct only one bit per address. Bit will be cleared when going in test mode, disabling EEPROM protection and returning in normal mode. (for diagnostics only) |
| ENVR | X | 1 | Stops the internal reference for DAC (Pin VREF). The reference voltage can be supplied externally. If ENDAC=0 then VREF is input. |
| HVSUP | 1 | 1 | Enable the regulator for battery supply. NOTE!!! After POR this regulator will be always on. It can be stopped from EEPROM data. |
| SELADREF | X | 0 | External supply of ADC reference to AGND pin. |
| | | 1 | Enable the internal ADC reference (connected to AGND pin). |
| POTMET | X | 0 | Sets threshold level for Rel1 to THRel1 in EEprom (address 75h) |
| | | 1 | Sets potentiometer input (pin IROUT) as threshold level |
| COMP1V | X | 0 | Sets Tobject as target voltage for comparator Comp1 |
| | | 1 | Sets Tambient as target voltage for comparator Comp1 |
| COMP1P | X | 0 | Sets polarity of Comp1: Inverting |
| | | 1 | Sets polarity of Comp1: Non-inverting |
| BYPTEMP | X | 0 | Output of Temp amplifier path is connected to ADC |
| | | 1 | Connects TINP-TINN directly to the ADC, bypassing the Temp-chain |
| REL1V | X | 0 | Sets Tobject as target voltage for Rel1 |
| | | 1 | Sets Tambient as target voltage for Rel1 |
| REL1P | X | 0 | Sets polarity of Rel1: Inverting |
| | | 1 | Sets polarity of Rel1: Non-inverting |
| EEWREN | 0 | 1 | Enables write access in EEPROM *write protect |
| TESTMODE | 0 | 1 | Indicates chip is in test mode *write protect |

*control bits EEWREN and TESTMODE are write protected. Their values can be set only with writing the appropriate data in 'Test' and 'WP' registers. These bits are flags which indicate the system operation

mode.

CONFREG0

| CONFREG0 bit functions | | | |
|------------------------|-----|------|---|
| Bit | POR | val | Function |
| IROUTC[1:0] | | 00b | IROUT pin function: IR-chain out |
| | | 01b | IROUT pin function: Linear Tobjct |
| | | 10b | IROUT pin function: Threshold Ref1 input |
| | | 11b | IROUT pin function: PWM out |
| TOUTC[1:0] | | 00b | TEMPOUT pin function: Temp-chain out |
| | | 01b | TEMPOUT pin function: Linear Tambient |
| | | 10b | TEMPOUT pin function: Comp1 out |
| | | 11b | TEMPOUT pin function: PWM out |
| SUBINC | | 0 | 2nd order derivative of thermistor function is positive (used if NTC=0) |
| | | 1 | 2nd order derivative of thermistor function is negative (used if NTC=0) |
| SUBDEC | | 0 | 2nd order derivative of thermistor function is positive (used if NTC=1) |
| | | 1 | 2nd order derivative of thermistor function is negative (used if NTC=1) |
| NTC | | 0 | Used thermistor is PTC |
| | | 1 | Used thermistor is NTC |
| TIMEOS[3:0] | | 0000 | Offset calibration interval: 0'00" |
| | | 0001 | Offset calibration interval: 0'02" |
| | | 0010 | Offset calibration interval: 0'17" |
| | | 0011 | Offset calibration interval: 0'19" |
| | | 0100 | Offset calibration interval: 1'07" |
| | | 0101 | Offset calibration interval: 1'09" |
| | | 0110 | Offset calibration interval: 1'24" |
| | | 0111 | Offset calibration interval: 1'26" |
| | | 1000 | Offset calibration interval: 2'14" |
| | | 1001 | Offset calibration interval: 2'16" |
| | | 1010 | Offset calibration interval: 2'31" |
| | | 1011 | Offset calibration interval: 2'33" |
| | | 1100 | Offset calibration interval: 3'21" |
| | | 1101 | Offset calibration interval: 3'23" |
| | | 1110 | Offset calibration interval: 3'38" |
| | | 1111 | Offset calibration interval: 3'40" |

OSCCTRL

Read access: No. The data is accessible for read via SPI only from eeprom address 05h.

Write access: Only in test mode for both writing directly to internal registers and writing to Eeprom if WP register is correctly set.

BGO: Reserved

Read access: No. The data is accessible for read via SPI only from eeprom address 06h.

Write access: Only in test mode for both writing directly to internal registers and writing to Eeprom if the WP register is correctly set.

LPF

Read access: No. The data is accessible for read via SPI only from eeprom address 07h.

Write access: Only in test mode for both writing directly to internal registers and writing to Eeprom if the WP register is correctly set.

This register keeps the calibration data for the time constants of digital low pass filters of both channels (see section Linearisation Unit).

| LPF bit functions | | | |
|-------------------|-----|--|---|
| Bit | POR | Val | Function |
| RSEL4 | | 0 | Refer to ADC interface setting |
| ENOSMB | | 0 | Enable offset measurement of both IR & Temp channels. |
| | | 1 | Disable offset measurement of both IR & Temp channels. |
| ENTAV | | 0 | Reserved for future development. Reset it for all applications. |
| | | 1 | Reserved for future development. Reset it for all applications. |
| IROS* | | 0 | Number of averaged offset measurements for IR chain: 512 |
| | | 1 | Number of averaged offset measurements for IR chain: 1024 |
| TOS* | | 0 | Number of averaged offset measurements for Temp chain: 512 |
| | | 1 | Number of averaged offset measurements for Temp chain: 1024 |
| LPFIR[2:0] | | Number of averaged points for IR measurement | |
| | | 00b | 64 |
| | | 01b | 128 |
| | | 10b | 256 |
| | | 11b | 512 |
| | | 100b | 1024 |
| LPFT[2:0] | | Number of averaged points for Temp measurement | |
| | | 00b | 64 |
| | | 01b | 128 |
| | | 10b | 256 |
| | | 11b | 512 |
| | | 100b | 1024 |

ADCREG

Read access: Directly via SPI in all modes.
Write access: Directly to internal register in test mode.

This register keeps the result from last analog to digital conversion..

IROUT

Read access: Directly from internal register.
Write access: Directly to internal register in test mode.

This register keeps the linearised object temperature. (Tobject)

Register format:

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|----|----|----|----|----|----|----|----|----|----|-----|-----|----|-----|
| Name | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OVH | OVL | FE | Res |

D11..D0 : 12 bit temperature data
OVH: Overflow flag for Tambient measurement, Ta>Tamax, D[11:0] set to FFFh
OVL: Underflow flag for Tambient measurement, Ta<Tamin, D[11:0] set to 000h
FE: Fatal Error in eeprom.
Res Not used, always zero.

Note that the last 4 bits are the status register.

TOUT

Read access: Directly from internal register.

Write access: Directly to internal register in test mode.

This register keeps the linearised ambient temperature. (T_{ambient})

Register format:

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|-----|----|----|----|----|----|----|----|----|----|----|-----|-----|----|-----|
| Name | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | OVH | OVL | FE | Res |

D11..D0 : 12 bit temperature data

OVH: Overflow flag for T_{ambient} measurement, $T_a > T_{\text{amax}}$, D[11:0] set to FFFh

OVL: Underflow flag for T_{ambient} measurement, $T_a < T_{\text{amin}}$, D[11:0] set to 000h

FE: Fatal Error in eeprom.

Res Not used, always zero.

Note that the last 4 bits are the status register. These bits are identical to the last 4 bits of the IROUT register.

IRDATA

Read access: Directly from internal register.

Write access: Directly to internal register in test mode.

This register keeps the measured IR data, compensated with the current offset of the amplifier (stored in Iros register).

TDATA

Read access: Directly from internal register.

Write access: Directly to internal register in test mode.

This register keeps the measured Temp data, compensated with the current offset of the Temp amplifier (stored in Tos register).

IROS

Read access: Directly from internal register.

Write access: Directly to internal register in test mode.

This register keeps the offset of the IR amplifier. Each measurement from IR amplifier will be compensated with this offset.

TOS

Read access: Directly from internal register.

Write access: Directly to internal register in test mode.

This register keeps the offset of the Temp amplifier. Each measurement from Temp amplifier will be compensated with this offset.

MAINSTM: Reserved

Read access: No
Write access: Directly to internal register in test mode

TEST

Read access: No.
Write access: Directly to internal register.

This register determines the chip mode. It is cleared after POR which corresponds to normal mode. Writing the proper data in this register will put the chip in test mode which will be indicated with bit 'Test' from confreg0.

| Test register | | | |
|---------------|-----------|-----------|--------------------------|
| Bit | POR | val | Function |
| B[15:9] | 0000000b | 1011001b | Forces chip in test mode |
| | | any other | Normal mode (default) |
| B[8:0] | 00000000b | X | |

WP

Read access: No.
Write access: Directly to internal register via SPI.

The register controls the write access to the eeprom. After POR this register is cleared and the eeprom is protected, no write access available. Writing the proper data in this register will remove the write protection of the eeprom and bit EEWREN (bit 1 in Confreg1) will be set.

| Eeprom write protect register | | | |
|-------------------------------|-----------|-----------|---------------------------------|
| Bit | POR | val | Function |
| B[15:9] | 00000000b | X | |
| B[6:0] | 0000000b | 1100101b | Enables write access to Eeprom* |
| | | any other | Sets EEprom write protect |

* The addresses 00-07h and 79-7Fh will be still protected. Write access here requires also 'Test mode'.

Eeprom Description

MLX90313 contains 128 x 16 EEPROM memory. The memory can be accessed through the serial interface. The 11 most significant bits are data bits and the 5 less significant bits are control bits used for the Error Check and Correction system (ECC). After POR the ASIC reads the full eeprom contents, checks it and corrects the single errors (1 wrong bit per address). If higher order error is discovered then the bit 'fatal error' will be set (see Confreg1 description in previous section).

The memory has two levels of protection. After POR the write access to the eeprom will be disabled. The external unit can remove this level of protection writing proper data in WP register. In this case all addresses in range 08-77h will be available for write access. The first and last 8 addresses will still be disabled. The write access to these cells is available only if the write protection is removed and the chip is in test mode.

Eeprom map overview

| Address list eeprom | | | | |
|---------------------|-----------------------------------|---------|---------|--------------|
| Register name | Function | Address | | Write access |
| | | Dec | Hex | |
| IRGAIN1 | IR-chain settings | 0 | 00h | test mode** |
| IRGAIN2 | IR-chain settings | 1 | 01h | test mode |
| TEMPGAIN | Temp-chain settings | 2 | 02h | test mode |
| CONFREG1 | Configuration | 3 | 03h | test mode |
| CONFREG2 | Configuration | 4 | 04h | test mode |
| OSCCTRL | Oscillator control | 5 | 05h | test mode |
| BGCTRL | Bandgap control | 6 | 06h | test mode |
| LPF | Low Pass Filter | 7 | 07h | test mode |
| CALIBRATION | Look up table linearisation. | 8-111 | 08h-6Fh | WP* |
| IOS-TEMP | Initial offset Temp-chain | 112 | 70h | WP |
| IOS-IR | Initial offset IR-chain | 113 | 71h | WP |
| RESERVED | | 114 | 72h | WP |
| THCOMP1 | Threshold for comparator Comp1 | 115 | 73h | WP |
| HSCOMP1 | Hysteresis for comparator Comp1 | 116 | 74h | WP |
| THREL1 | Threshold for comparator of Rel1 | 117 | 75h | WP |
| HSREL1 | Hysteresis for comparator of Rel1 | 118 | 76h | WP |
| RESERVED | | 119 | 77h | |
| CHIP-ID | Data | 120-127 | 78h-7Fh | test mode |

*WP: Write access to EEprom is controlled by the content of the internal register WP

**Test mode: Write access controlled by the internal register WP and only available in test mode

The last 8 addresses 0x78 to 0x7F are free to use for the user. They can hold some calibration data or identification number. All data programmed into the eeprom must pass the error checking. Therefore, one must add 5 hamming bits to the eeprom data, in the 5 least significant bits.

Eeprom bit definitions

Following table gives the bit definitions for all addresses that can be modified by the user. All other addresses contain specific calibration data and should be left unchanged.

Note that some bits marked "RES" are reserved and should never not be changed by the user. If other bits in such an address must be changed, read original contents first to get the status of the reserved bits.

| EEPROM BIT DEFENITIONS | | | | | | | | | |
|------------------------|------------------------|--------------------|--------------------|-------------------|-------------|--------------|--------------|---------------|---------------|
| ADDRESS (HEX) | REGISTERH REGISTERL | B15 B7 | B14 B6 | B13 B5 | B12 B4 | B11 B3 | B10 B2 | B9 B1 | B8 B0 |
| 0x00 | IRGAIN1H IRGAIN1L | ENDREFDIV GCI2 | ENDAC GCI1 | ENEN GCI0 | GCI7 K | GCI6 H4 | GCI5 H3 | GCI4 H2 | GCI3 H1 |
| 0x01 | IRGAIN2H IRGAIN2L | AGNDC3 RSEL2 | AGNDC2 RSEL1 | AGNDC1 RSEL0 | AGNDC0 K | SELDR2 H4 | SELDR1 H3 | SELDR0 H2 | RSEL3 H1 |
| 0x02 | TEMPGAINH TEMPGAINL | TRSEL1 GCT2 | TRSEL0 GCT1 | IRSEL2 GCT0 | IRSEL1 K | IRSEL0 H4 | GCT5 H3 | GCT4 H2 | GCT3 H1 |
| 0x03 | CONFREG1H CONFREG1L | ENVR REL1P | HVSUP RES | SELADREF RES | POTMET K | COMP1V H4 | COMP1P H3 | BYPTEMP H2 | REL1V H1 |
| 0x04 | CONFREG0H CONFREG0L | IROUTC1 TIMEOS2 | IROUTC0 TIMEOS1 | TOUTC1 TIMEOS0 | TOUTC0 K | SUBINC H4 | SUBDEC H3 | NTC H2 | TIMEOS3 H1 |
| 0x05 | OSCH OSCL | RES RES | RES RES | ENAGNDB RES | RES K | RES H4 | RES H3 | RES H2 | RES H1 |
| 0x06 | BGH BGL | RES RES | RES RES | RES RES | RES K | RES H4 | RES H3 | RES H2 | RES H1 |
| 0x07 | LPFH LPFL | RSEL4 LPFT2 | ENOSM LPFT1 | ENTAV LPFT0 | IROS K | TOS H4 | LPFIR2 H3 | LPFIR1 H2 | LPFIR0 H1 |
| 0x73 | THComp1 | THR10 THR2 | THR9 THR1 | THR8 THR0 | THR7 K | THR6 H4 | THR5 H3 | THR4 H2 | THR3 H1 |
| 0x74 | HSComp1 | HST10 HST2 | HST9 HST1 | HST8 HST0 | HST7 K | HST6 H4 | HST5 H3 | HST4 H2 | HST3 H1 |
| 0x75 | THRel1 | THR10 THR2 | THR9 THR1 | THR8 THR0 | THR7 K | THR6 H4 | THR5 H3 | THR4 H2 | THR3 H1 |
| 0x76 | HSRel1 | HST10 HST2 | HST9 HST1 | HST8 HST0 | HST7 K | HST6 H4 | HST5 H3 | HST4 H2 | HST3 H1 |
| 0x78 - 0x7F | USER1..7 | UDATA10 UDATA2 | UDATA9 UDATA1 | UDATA8 UDATA0 | UDATA7 K | UDATA6 H4 | UDATA5 H3 | UDATA4 H2 | UDATA3 H1 |

Eeprom Hamming coding

All addresses in the eeprom are coded using hamming code. Therefore, if one wants to program data into any eeprom address, the hamming bits must be calculated first. This is not done by the

There are 11 bits + 4 hamming bits + 1 extra redundant bit in the eeprom. Data bits are numbered D10..D0, Hamming H4..H1, the extra bit is called K.

The bit definitions in the eeprom words are:

| | | | | | | | | | | | | | | | | |
|------|-----|----|----|----|----|----|----|----|----|----|----|---|----|----|----|----|
| Pos | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| name | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | K | H4 | H3 | H2 | H1 |

The hamming bits are calculated as follows:

$$H1 = P(D0, D1, D3, D4, D6, D8, D10)$$

H2 = P(D0,D2,D3,D5,D6,D9,D10)
H3 = P(D1,D2,D3,D7,D8,D9,D10)
H4 = P(D4,D5,D6,D7,D8,D9,D10)

The extra K bit is calculated as:

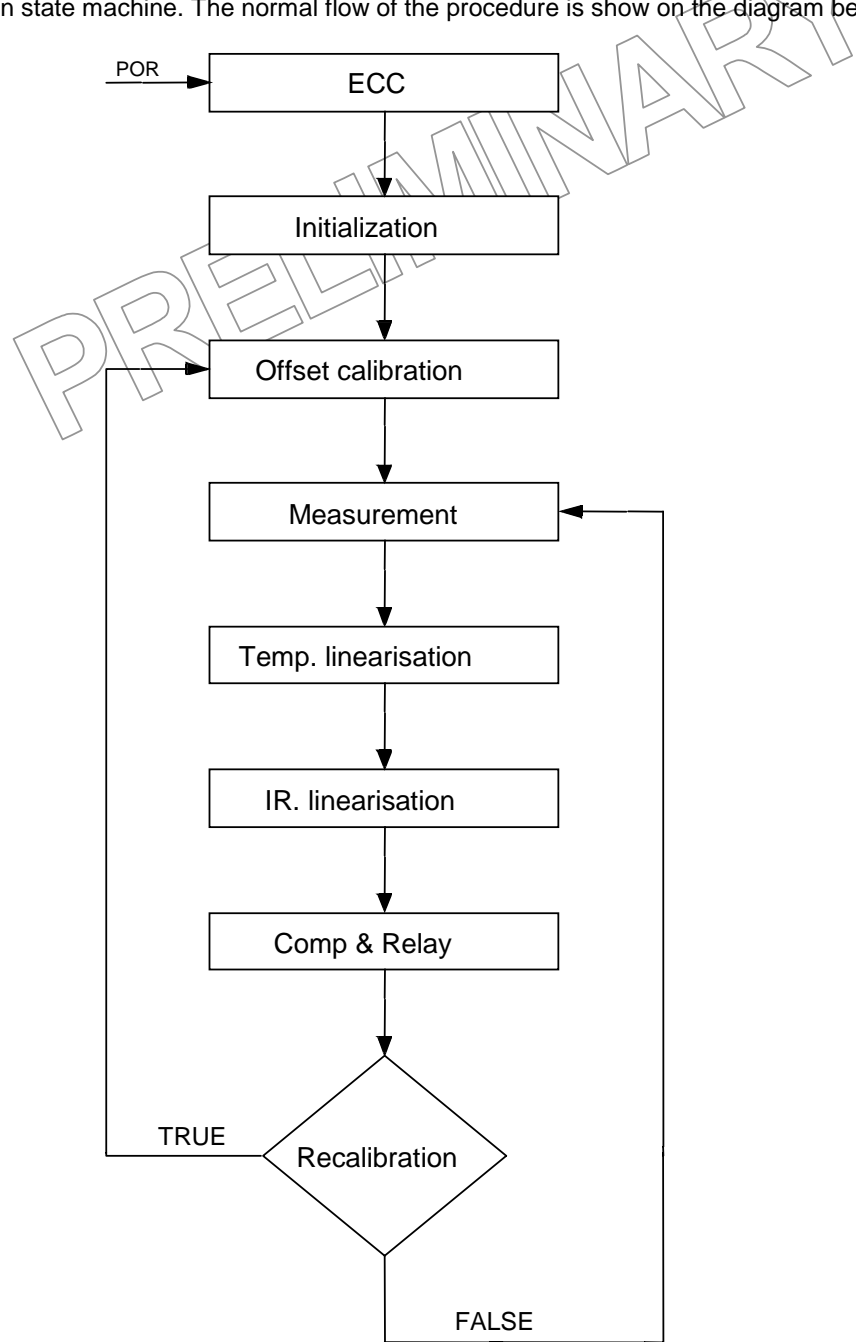
K = P(D10,D9,D8,D7,D6,D5,D4,D3,D2,D1,D0,H4,H3,H2,H1)

Note :P is parity over the noted data bits. Parity is 1 if the number of ones is odd.
When reading eeprom addresses, the numerical value can be found by simply dividing the returned data by 32.

PRELIMINARY

90313 Algorithm

The algorithm of the ASIC is divided in several operations: ECC, initialization, offset measurement, object and ambient measurement and offset cancellation, linearisation, comparator functions. Each of this operation is controlled from the main state machine. The sequence and control of all these state machines is controlled from main state machine. The normal flow of the procedure is show on the diagram below.



Main state machine control flow

Error Check and Correction (ECC)

The ASIC starts this procedure only after Power On Reset. The state machine reads all data in the eeprom and corrects all single errors (1 wrong bit per address) if necessary. The wrong information from the eeprom will be refreshed with correct one. In case of double error (2 wrong bits per address) which can only be detected, not corrected, the system will leave the data in the address and will set the flag 'Fatal error' (bit 1 in status register). This data is available through SPI or PWM.

Initialization

At this step the system reads its configuration from the eeprom. All data from eeprom addresses 00-07h will be filled in the corresponding peripheral registers. After this step the ASIC is ready for normal operation.

Offset measurement (offset drift compensation)

The offset measurement is run periodically from the main state machine. The customer can select one of 16 possible interval times for offset measurement (see 'CONFREG0 bit functions'). Depending on the selected values for bits IROS and TOS in LPF register (address 07h in EEPROM) the average of 512 or 1024 measurements is stored. The time this measurement takes is about 75ms or 150ms, depending on the number of measurements taken. Note that during this time the outputs are kept on their last value before calibration started, so the current temperature is not available during offset calibration. The measured offset results will be stored in IROS (for IR amplifier chain) and TOS (for Temp amplifier chain) registers.

Measurement and offset cancellation

The results from analog to digital conversion for both channels will be the mean of custom defined number of measurements, controlled from the LPF register (address 07 in eeprom). This data will be compensated with corresponding offsets, stored in IROS and TOS registers and final offset free data will be stored in IRDATA (for IR amplifier chain) and TDATA (for Temp amplifier chain) registers. The number of measurements of which the averaging is taken can vary between 64 and 1024 (see 'LPF register bit functions') and can be selected independently for both channels.

Linearisation

Linearisation proceeds in two steps and can be described by the picture below. In the first step the ambient temperature is calculated from the measured signal at TINP-TINN. The system outputs a digital value for the ambient temperature based on the calibration data. The value is stored in a dedicated register and from there available for the DAC and PWM (Tambient-register, address 0Ah). The register can also be read digitally by means of the SPI.

The system is developed to support different temperature sensors. 3 bits in the configuration register (EEProm address 03h), determine the type of characteristic. NTC defines the first derivative of the temperature sensor (NTC-type is logical 1, PTC-type is logical 0). SUBDEC and INCDEC define the

second derivative of the temperature sensor $\left(\frac{d^2VRth}{dT^2}\right)$.

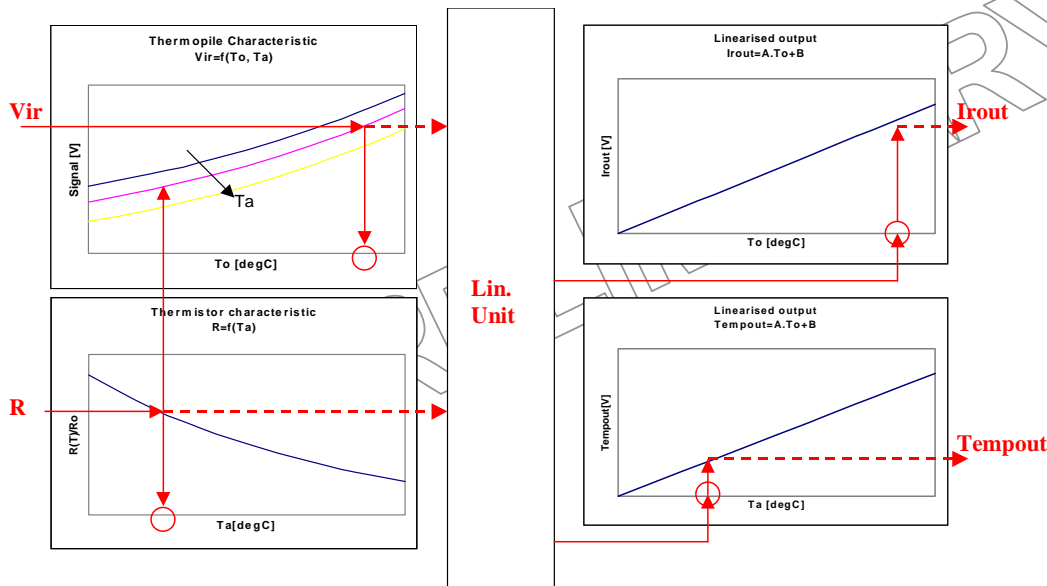
The result of the linearisation is stored as the 12 MSB's of the Tambient-register (or TOUT-register). The code 000h will correspond to Tamin, FFFh will correspond to Tamax. These two limits are determined by

calibration. Accordingly the output resolution will be $\frac{T_{a\ max} - T_{a\ min}}{4096}$ in K per LSB

In the second step the value of the ambient temperature is combined with the measured signal at IRINP-IRINN to obtain a calculated value for the so-called object temperature, based on the calibration data. The value is stored in a dedicated register and from there available for the DAC and PWM (Tobject-register, address 09h). The register can also be read digitally by means of the SPI.

The result of the linearisation is stored as the 12 MSB's of the Tobject-register (or IROUT-register). The

code 000h will correspond to T_{min} , FFFh will correspond to T_{max} . These two limits are determined by calibration. Accordingly the output resolution will be $\frac{T_{o\ max} - T_{o\ min}}{4096}$ in K per LSB.



When reading the linearised data digitally by means of the SPI, a 16-bit word is returned. The 12 MSB's contain the temperature value as described above, the 4 LSB's form a status register, which is the same for both the IROUT address and the TOUT. The meaning of the individual bits is explained in the table below.

| Linearisation Status Register | | | | |
|-------------------------------|---|--|--|--|
| S[3:0] | Meaning | | | |
| 1 X X X | Overflow flag for $T_{ambient}$ measurement, $T_a > T_{amax}$, TOUT[15:4] set to FFFh | | | |
| X 1 X X | Underflow flag for $T_{ambient}$ measurement, $T_a < T_{amin}$, TOUT[15:4] set to 000h | | | |
| X X 1 X | Flag for Fatal Error in eeprom * | | | |
| X X X 0 | Not used, always zero | | | |

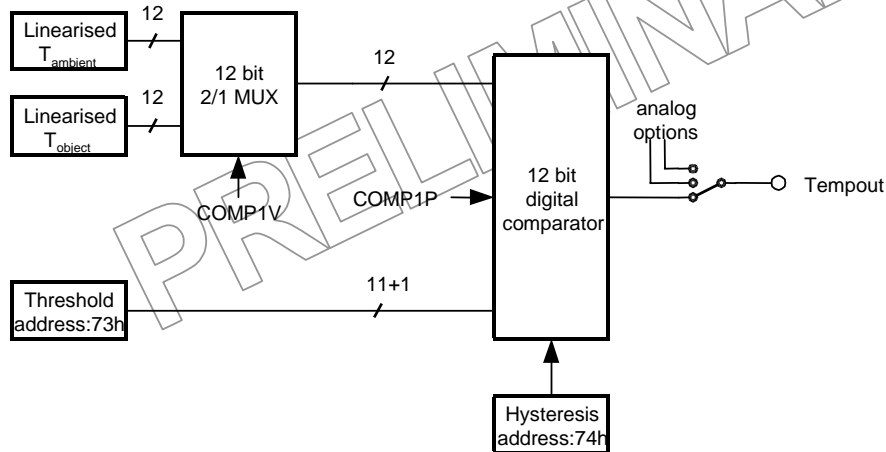
*Fatal Error is the uncorrectable error in EEPROM (more than 2 wrong bits per address). When this error occurs, the normal process flow does not change, but the results may go wrong.

The status register is particularly important when an overflow (or underflow) condition occurs for the T_a -measurement. If the overflow condition occurs IROUT register will be set to FFFh, if underflow - IROUT will be 000h. If the user selects to monitor the analogue output through the DAC, then care must be taken to ensure that $T_{ambient}$ will never exceed the selected range, as the over- or underflow condition is not flagged.

Comparators and relay output

MLX90313 contains two programmable 12 bit digital comparators. For each circuit the target signal, the threshold and hysteresis can be programmed in different configurations, according to the table below. The principle of operation is shown in the following schematics. The threshold and hysteresis values are stored in eeprom, the control bits are part of the configuration register. The REL1 comparator threshold can be either read from EEPROM (address 75h) or controlled by an external potentiometer connected to IROUT. Note that the threshold and hysteresis registers in eeprom are only 11 bits wide. Therefore a zero is added in the LSB position to the threshold and hysteresis registers, making this register also 12 bits.

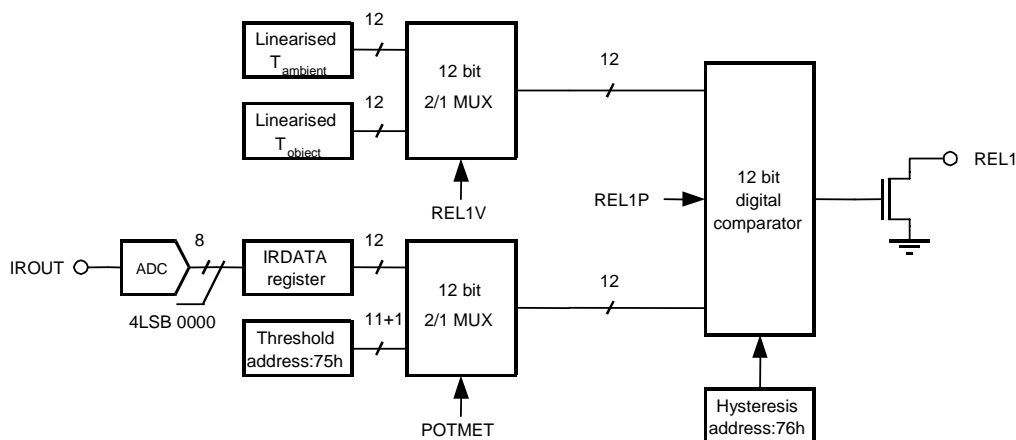
| Comp1 circuitry setting | | | | |
|-------------------------|---------------------|----------|----------------|---------------|
| | Comp1 source signal | | Comp1 Polarity | |
| Control Bit | COMP1V | | COMP1P | |
| Setting | 0 | Tobject | 0 | Inverting |
| | 1 | Tambient | 1 | Non-inverting |



Comparator1 (COMP1) Configuration diagram

Note that the threshold for COMP1, is always in eeprom address 0x73.

| Rel1 circuitry setting | | | | | | |
|------------------------|--------------------|----------|-----------------------|--------------|---------------|---------------|
| | Rel1 source signal | | Rel1 Threshold source | | Rel1 Polarity | |
| Control Bit | REL1V | | POTMET | | REL1P | |
| Setting | 0 | Tobject | 0 | [75h] | 0 | Inverting |
| | 1 | Tambient | 1 | IRDATA [03h] | 1 | Non-inverting |



Comparator2 (REL1 pin) Configuration diagram

After the temperature data is updated in TOUT and IROUT registers (the current Ta&To are calculated) the main state machine will enable the comparator functions of the chip if one of them is enabled. Threshold data for both outputs is stored in addresses 73h (for Comp1) and 74h (for Rel1) in eeprom.

The threshold data can be calculated by the formula:

$$\text{Threshold value} = \frac{T_{thr} - T_{\min}}{T_{\max} - T_{\min}} \times 2048.$$

where: T_{thr} is the target temperature for the comparator
 T_{\min} , T_{\max} are the minimum and maximum temperature under calibration.

The hysteresis value can be calculated by following formula:

$$\text{Hysteresis value} = \frac{Thys}{T_{\max} - T_{\min}} \times 2048$$

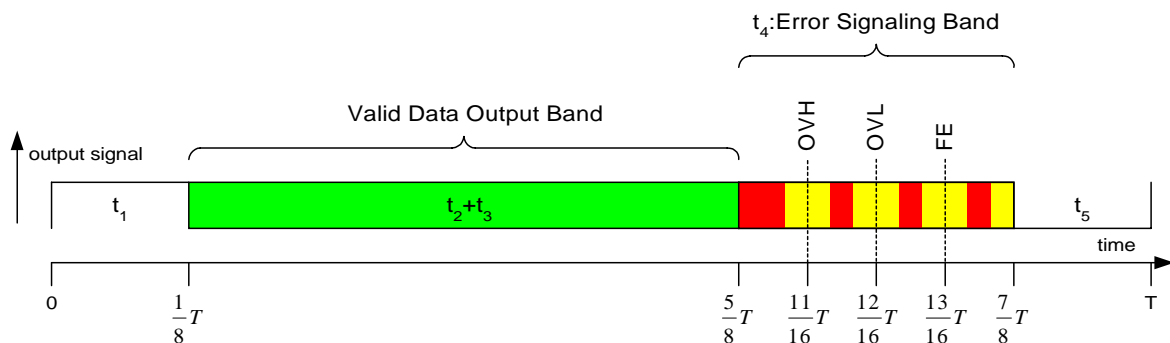
where: $Thys$ is the desired hysteresis in deg C.
 T_{\min} , T_{\max} are the minimum and maximum temperature under calibration

Both formulas are valid for ambient and IR temperatures. The data for hysteresis must be stored at addresses 74h (for Comp1) and 76h (for Rel1) after adding the hamming bits in the 5 least significant bit places. Refer to Hamming Coding in eeprom description section for details.

Pulse Width Modulation

The PWM signal has a period of 102.4ms typical consisting of 2048 clock cycles of 50µs. Every frame starts with a leading buffer time, t_1 , during which the signal is always high, as shown in the figure below. The leading buffer time is followed by a slot for the useful data signal, t_2 and t_3 , where the ration $t_2/(t_2+t_3)$ is the representation of the output value. t_4 is a slot for signaling of special conditions, such as out of range measurement of the sensor temperature, T_{ambient} and the occurrence of a fatal EEprom error, i.e. an error that can no longer be corrected automatically by the ECC circuitry of MLX90313.

| Error signaling band | | |
|-------------------------|------------|----------------|
| Condition | Duty cycle | nominal timing |
| OVH: Tambient overflow | 68.75 % | 70.4 ms |
| OVL: Tambient underflow | 75 % | 76.8 ms |
| FE: Fatal Error EEprom | 81.25% | 83.2 ms |

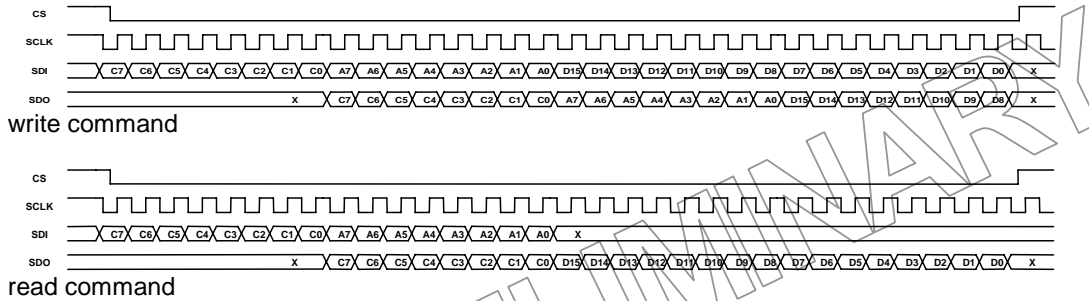


Serial Interface

Protocol

The digital interface implemented in MLX90313 is SPI compatible. It can be used to access the on-chip EEPROM and all internal registers. The chip will always work as a slave device. The format of any

command is always 32 bits: 8 bits for the operation code, 8 bits for the address and 16 bits of data. The communication protocol is presented below.



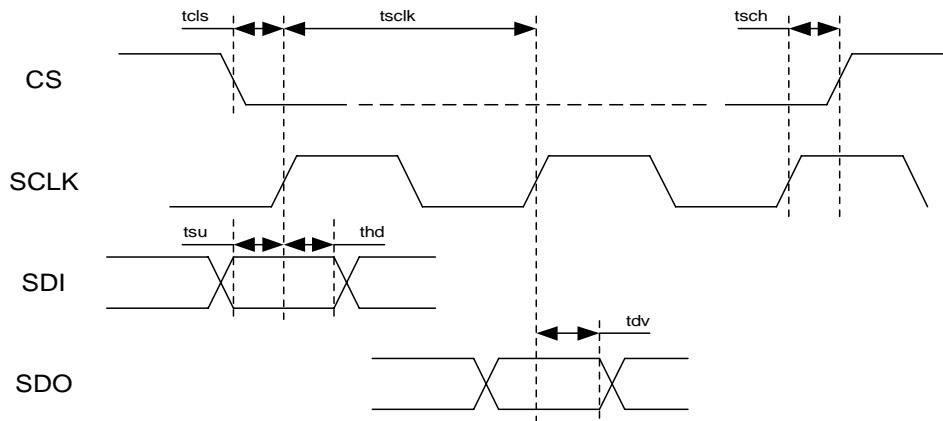
Every write command starts with a high to low transition of CS and ends by a low to high transition of CS after 32 periods of the serial data clock (SCLK). MLX90313 reads the data present on SDI on the rising edge of the clock. With a delay of 8 periods of the serial clock, the SPI will repeat the opcode, address and the first 8 bits of data on pin SDO. This allows the external master to check command and address and terminate the operation in case of an error by forcing CS high before the end of the complete command cycle, i.e. before the end of the 32 clock periods.

The read command is build up similarly, except that no data has to be passed of course. On SDO the opcode will be followed directly by the requested data, the address is not returned in this case.

The data on SDO is valid on the rising edge of the clock. In case of a read command, the SPI output will be valid on SDO starting on the 17th rising edge of the clock (after CS low) as indicated in the figure above.

Timing/speed

The bit-rate depends on the serial data clock (SCLK) supplied by the master controller and is limited to 125kb/s. The timing requirements are given in the figure and table below



| SPI timing requirements | | | |
|-------------------------|---------------------|---------|------|
| Symbol | Parameter | Value | Unit |
| tsclk | Sclk period | min 8 | µs |
| tcls | CS low to SCLK high | min 50 | ns |
| tsch | SCLK low to CS high | min 50 | ns |
| tsu | data in setup time | min 200 | ns |
| thd | data in hold time | min 200 | ns |

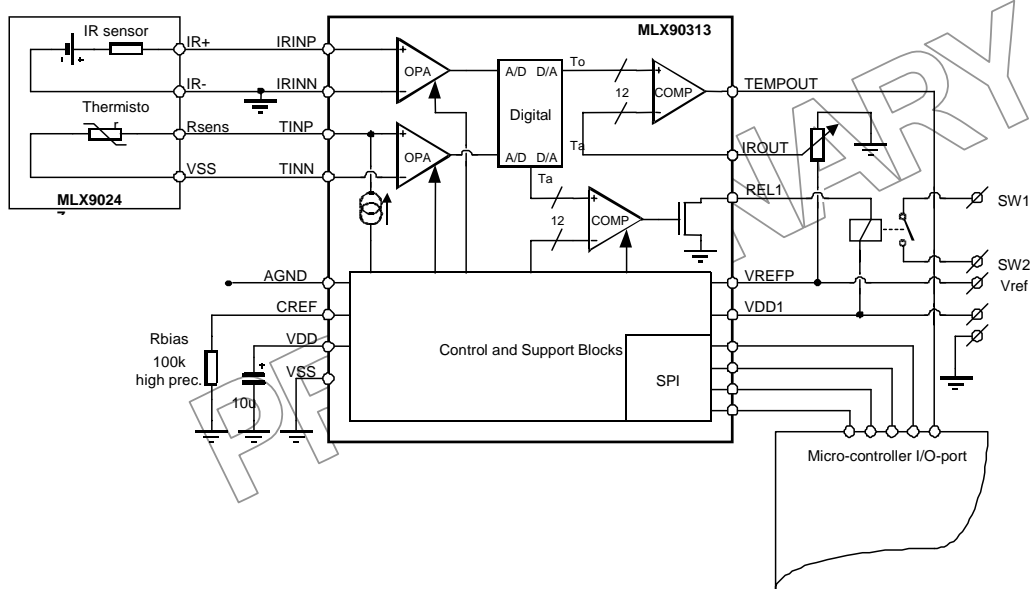
| | | | |
|-----|----------------|-------|----|
| tdv | data out valid | min 1 | μs |
|-----|----------------|-------|----|

operation codes

The operation code is the first series of 8bits in a command, C[7:0] in the figure on the protocol above. Below table summarizes the operations available in MLX90313.

| Operation Codes | | | | | | | | | |
|-----------------|--------|---|---|---|---|---|---|---|-------------------------|
| mnem. | C[7:0] | | | | | | | | Command |
| WR | X | 1 | 0 | 1 | X | 0 | X | X | Write internal register |
| RD | X | 1 | 0 | 0 | 1 | 0 | X | X | Read internal register |
| WEPR | 0 | 0 | 0 | 1 | X | X | X | X | Write Eeprom |
| ER | 0 | 0 | 1 | X | X | X | X | X | Erase EEprom |
| REPR | X | 0 | 0 | 0 | 1 | X | X | X | Read Eeprom |
| BLWR | 1 | 0 | 0 | 1 | X | X | X | X | Block Write Eeprom |
| BLER | 1 | 0 | 1 | X | X | X | X | X | Block erase Eeprom |

Applications Information



Typical application diagram

In the above application diagram, a simple thermometer with alarm function is depicted. As external components there are only a thermopile (like the MLX90247x) and a current setting resistor is used. Because the current needs to be constant over temperature and time, it is advised to use a precision resistor. The tempout pin is the output of a comparator which compares the measured object temperature with the threshold set by the external potentiometer. The second comparator operates the relay. It compares the ambient temperature with a fixed threshold programmed in eeprom. Both ambient and object temperatures can be read continuously by the microprocessor using the SPI interface.

For more application examples, take a look at our MLX90601 Infrared thermometer module, which incorporates a MLX90247 thermopile sensor and the MLX90313 IR sensor interface.

Support Tools

In a short time Melexis will provide a demo board which can demonstrate all MLX90313's features. This will come with software which allows easy configuration of the MLX90313. Please have a look at www.melexis.com for latest info.

ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

FAQ

Q: When is the MLX90313 available ?

A: Currently Melexis only delivers the MLX90313 as part of the MLX90601x Infrared Thermometer module. Please refer to MLX90601 datasheet for details. Samples can be obtained Q3/2001, full production starts Q4/2001.

Glossary of Terms

| | |
|---------------------------------|---|
| ADC | Analog-to-digital converter |
| Ambient Compensation | The IR signal captured by a thermopile sensor is not only dependent on the temperature of the object (T _{object}) but also on the temperature of the sensor itself. Therefore the IR signal is compensated for this effect by means of the measured sensor temperature (T _{ambient}). This rather complex calculation is performed in the linearisation unit of MLX90313. |
| ASIC | application specific integrated circuit |
| Band-gap | Circuit to generate accurate absolute voltages. Usually they are independent of temperature and supply voltage, like the one used in the MLX90313 |
| Chopper compensated amplifier | Special amplifier configuration aimed at ultra low offset |
| DAC | Digital-to-analog converter |
| Differential nonlinearity (DNL) | The deviation of any code from an ideal 1 LSB step |
| ECC | Error Checking and Correction |
| Eeprom | non-volatile memory that can be electrically erased and rewritten. This type of memory is used to store configuration and calibration data needed by the MLX90313. |
| Hamming coding | By giving a message a extra number of bits (= so called hamming bits), one can not only detect, but also correct a error that occurs in the stored data or the hamming bits. The eeprom memory of the MLX90313 uses hamming coding to do a error check and correction if needed and possible. |
| Integral nonlinearity (INL) | This is the maximum deviation from the ideal output curve and the actual output |
| IR | Infrared. Every object emits infrared radiation in relation to its temperature. This effect can be used to measure this temperature without the need for physical contact. |
| Linearisation | The signal from a thermopile is not linear with the object temperature. MLX90313 is therefore equipped with a digital calculation unit that produces an output that is linear with the object temperature. |
| LSB,MSB | Least Significant Bit, Most Significant Bit |
| NTC | See Thermistor. |
| PGA | Programmable gain amplifier. |

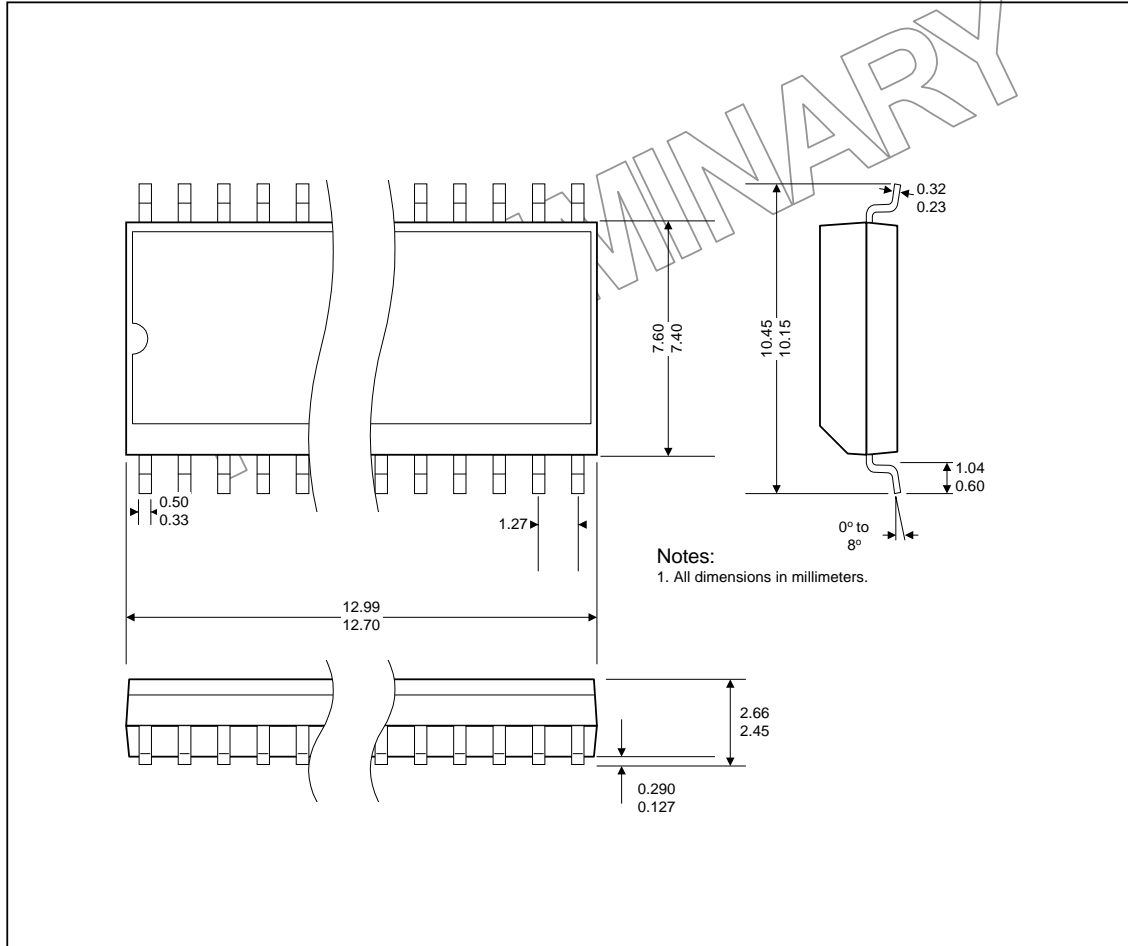
| | |
|--|---|
| POR | power –on reset: reset circuit that starts the digital system in a known state whenever the supply voltage is cycled |
| PSSR | Power Supply Rejection Ratio: Measure for an amplifier's immunity to disturbances on the supply connections. |
| PTC | See Thermistor. |
| SPI | Serial Peripheral Interface. Commonly used 4 wire serial link to connect different circuits over a short distance. |
| Ta, Tambient, ambient temperature Thermistor | The temperature of the IR sensor. Temperature dependant resistor. Basically there are 2 types. The types that increase their resistance with rising temperature are PTC (positive thermal coefficient) type. The ones that decrease their resistance with rising temperature we call NTC (negative thermal coefficient) type. The MLX90313 can work with both types. |
| Tobject, To and Target Temperature | commonly used terms in infrared thermometry. It refers to the temperature of the target, at which the IR sensor is "looking" |

Disclaimer

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PRELIMINARY

Physical Characteristics



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