◇ STRUCTURE Silicon Monolithic Integrated Circuit

◇ PRODUCT Microwire BUS Serial EEPROMs

◇ SERIES SIGNATURE SERIES

◇ FAMILY BR93C□□ family

◇ TYPE Supply voltage 4.5V～5.5V/Opreating temperature -40℃～+105℃type

◇ PART NUMBER BR93C□□-□□□7TP

PART NUMBER	PACKAGE	DENSITY
BR93C46- MN7TP	SO8 narrow	1Kbit
BR93C56- MN7TP		2Kbit
BR93C66- MN7TP		4Kbit
BR93C76- MN7TP		8Kbit
BR93C86- MN7TP		16Kbit
BR93C46-TMN7TP	SO8 narrow (different pin assignment)	1Kbit
BR93C56-TMN7TP		2Kbit
BR93C66-TMN7TP		4Kbit
BR93C76-TMN7TP		8Kbit
BR93C86-TMN7TP		16Kbit

◇ FEATURES

Microwire BUS interface
Endurance : 1,000,000 erase/write cycles
Data retention : 40 years
Intial Data FFFFh in all address

◇ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	-65	125	℃
V_{OUT}	Output Range(Q=V_{OH} or Hi-Z)	-0.3	Vcc+0.3	V
V_{IN}	Input range	-0.3	Vcc+0.3	V
V_{CC}	Supply Voltage	-0.3	6.5	V

◇ POWER DISSIPATION (Ta=25℃)

PACKAGE	Rating	Unit
SO8 narrow	450 *1	mW

* Degradation is done at 4.5mW/℃(*1) for operation above 25℃

◇ RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature	−40	105	℃

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified, Ta=−40～105℃, Vcc=4.5～5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−	−	±2.5	μA	$0V \leqq V_{IN} \leqq Vcc$
Output Leakage Current	I_{LL}	−	−	±2.5	μA	$0V \leqq V_{OUT} \leqq Vcc$, Q in Hi-Z
Supply Current (CMOS Inputs)	I_{CC}	−	−	2	mA	Vcc=5V,S=V_{IH},f=2MHz
Supply Current(Stand-by)	I_{CC1}	−	−	15	μA	Vcc=2.5V,S=Vss,C=Vss
Input Low Voltage(D,C,S)	V_{IL}	−0.3	−	0.8	V	
Input High Voltage(D,C,S)	V_{IH}	2	−	Vcc+0.3	V	
Output Low Voltage(Q)	V_{OL}	−	−	0.4	V	Vcc=5V,I_{OL}=2.1mA
Output High Voltage(Q)	V_{OH}	2.4	−	−	V	Vcc=5V,I_{OH}=−400 μA

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified, Ta=−40～105℃, Vcc=4.5～5.5V)

Parameter	Symbol	Specification			Unit
		Min.	Typ.	Max.	
Clock Frequency	f_C	D.C	−	2	MHz
Chip Select Low to Clock High	t_{SLCH}	50	−	−	ns
Chip Select Set-up Time	t_{SHCH}	50	−	−	ns
Chip Select Low to Chip Select High	t_{SLSH}	200	−	−	ns
Clock High Time	t_{CHCL} *1	200	−	−	ns
Clock Low Time	t_{CLCH} *1	200	−	−	ns
Data In Set-up Time	t_{DVCH}	50	−	−	ns
Data In Hold Time	t_{CHDX}	50	−	−	ns
Clock Set-up Time(relative to S)	t_{CLSH}	50	−	−	ns
Chip Select Hold Time	t_{CLSL}	0	−	−	ns
Chip Select to Ready/Busy Status	t_{SHQV}	−	−	200	ns
Chip Select Low to Output Hi-Z	t_{SLQZ}	−	−	100	ns
Delay to Output Low	t_{CHQL}	−	−	200	ns
Delay to Output Valid	t_{CHQV}	−	−	200	ns
Erase/Write Cycle time	t_W	−	−	5	ms

*1 $t_{CHCL}+t_{CLCH} \geqq 1/f_C$

◇ BLOCK DIAGRAM

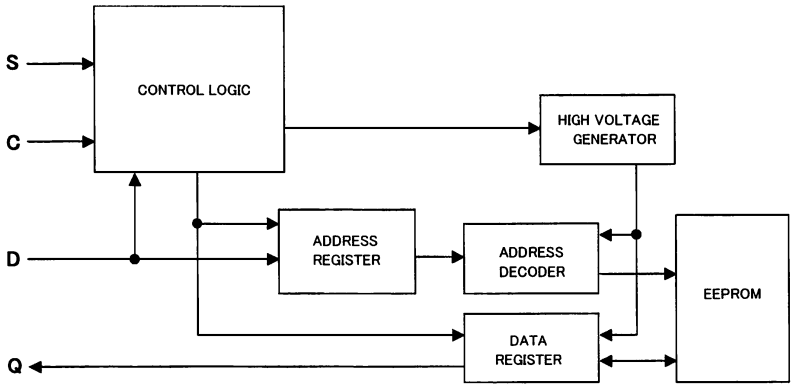


Fig .−1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

PIN No.	PIN NAME	
1	S	DU
2	C	Vcc
3	D	S
4	Q	C
5	Vss	D
6	DU	Q
7	DU	Vss
8	Vcc	DU
PART NUMBER	BR93C46-MN7TP	BR93C46-TMN7TP
	BR93C56-MN7TP	BR93C56-TMN7TP
	BR93C66-MN7TP	BR93C66-TMN7TP
	BR93C76-MN7TP	BR93C76-TMN7TP
	BR93C86-MN7TP	BR93C86-TMN7TP

◇ NOTES FOR POWER SUPPLY

This IC has a POR (Power On Reset) circuit as mistake write countermeasure.
After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if S is "H" at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the following conditions.

1. Set S = "L".
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit operation.

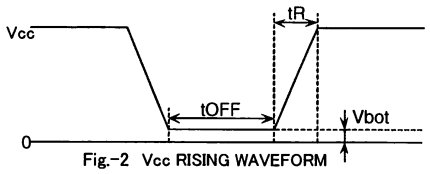


Fig.-2 Vcc RISING WAVEFORM

◇Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

◇CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) Vss electric potential

Set the voltage of Vss terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of Vss terminal.

(3) Thermal design

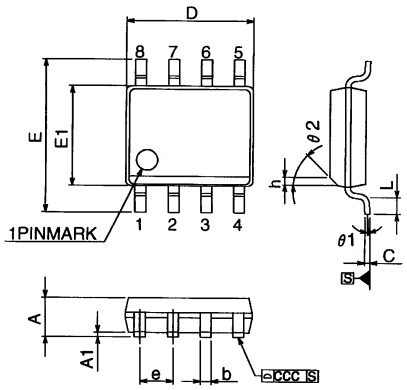
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and Vss owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore , evaluated design sufficiently.

◇ PHYSICAL DIMENSION



Notes
1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MS-012 variation AA.

Fig.-3 SO8 narrow Package Outline

◇ SO8 narrow Package size data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	1.35	1.75	–	0.053	0.069
A1	–	0.10	0.25	–	0.004	0.010
b	–	0.33	0.51	–	0.013	0.020
c	–	0.19	0.25	–	0.007	0.010
D	–	4.80	5.00	–	0.189	0.197
e	1.27	–	–	0.05	–	–
E	–	5.80	6.20	–	0.228	0.244
E1	–	3.80	4.00	–	0.150	0.157
L	–	0.40	1.27	0.05	0.016	0.050
θ1	–	0°	8°	–	0°	8°
ccc	–	–	0.10	–	–	0.004
h	–	0.25	0.50	–	0.010	0.020
θ2	45°	–	–	45°	–	–

Notes

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