◇ STRUCTURE Silicon Monolithic Integrated Circuit
◇ PRODUCT Microwire BUS Serial EEPROMs
◇ SERIES ADVANTAGE SERIES
◇ FAMILY BR93C□□ family
◇ TYPE Supply voltage 2.7V～5.5V/Opreating temperature -40℃～+85℃type
◇ PART NUMBER BR93C□□-10□U-2.7

PART NUMBER	PACKAGE	DENSITY
BR93C46 -10SU-2.7	8-lead JEDECSOIC	1Kbit
BR93C56 -10SU-2.7		2Kbit
BR93C66 -10SU-2.7		4Kbit
BR93C76 -10SU-2.7		8Kbit
BR93C86 -10SU-2.7		16Kbit
BR93C46R-10SU-2.7	8-lead JEDECSOIC(Different pin assignment)	1Kbit
BR93C46 -10TU-2.7	8-lead TSSOP	1Kbit
BR93C56 -10TU-2.7		2Kbit
BR93C66 -10TU-2.7		4Kbit
BR93C76 -10TU-2.7		8Kbit
BR93C86 -10TU-2.7		16Kbit

◇ FEATURE
Microwire BUS interface
Endurance : 1,000,000 erase/write cycles
Data retention : 100 years
Intial Data FFFFh in all address

◇ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	-65	125	℃
V_{OUT}	Output Range(Q=V_{OH} or Hi-Z)	-0.3	Vcc+0.3	V
V_{IN}	Input range	-0.3	Vcc+0.3	V
V_{CC}	Supply Voltage	-0.3	6.5	V

◇ POWER DISSIPATION (Ta=25℃)

PACKAGE	Rating	Unit
8-lead JEDECSOIC	450 *1	mW
8-lead TSSOP	330 *2	mW

* Degradation is done at 4.5mW/℃(*1), 3.3mW/℃(*2)for operation above 25℃

◇ RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage	2.7	5.5	V
T_A	Ambient Operating Temperature	-40	85	℃

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified, Ta=−40～85℃, Vcc=2.7～5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
Supply Voltage	Vcc	2.7	−	5.5	V	
Supply Current	I_{CC}	−	−	2.0	mA	Vcc=5V,READ at f=1MHz
		−	−	2.0	mA	Vcc=5V,WRITE at f=1MHz
Standby Current	I_{SB}	−	−	10	μA	Vcc=2.7V,CS=0V
		−	−	30	μA	Vcc=5.0V,CS=0V
Input Leakage	I_{IL}	−	−	1.0	μA	$0V \leqq V_{IH} \leqq Vcc$
Output Leakage	I_{OL}	−	−	1.0	μA	$0 \leqq V_{OUT} \leqq Vcc$,DO in Hi-Z
Input Low Voltage	V_{IL1}	−0.3	−	0.8	V	$4.0V \leqq Vcc \leqq 5.5V$
Input High Voltage	V_{IH1}	2.0	−	Vcc+0.3		
Input Low Voltage	V_{IL2}	−0.3	−	0.2Vcc	V	$Vcc \leqq 4.0V$
Input High Voltage	V_{IH2}	0.7Vcc	−	Vcc+0.3		
Output Low Voltage	V_{OL1}	−	−	0.4	V	$2.7V \leqq Vcc \leqq 5.5V$
Output High Voltage	V_{OH1}	2.4	−	−		IOL=2.1mA, IOH=−0.4mA

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified, Ta=−40～85℃, V_{CC}=2.7～5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
SK Clock Frequency	f_{SK}	0	−	2	MHz	$4.5V \leqq Vcc \leqq 5.5V$
		0	−	1		$2.7V \leqq Vcc \leqq 5.5V$

◇ NOTES FOR POWER SUPPLY

This IC has a POR (Power On Reset) circuit as mistake write countermeasure.
After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is "H" at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the following conditions.

1. Set CS = "L".
2. Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit operation.

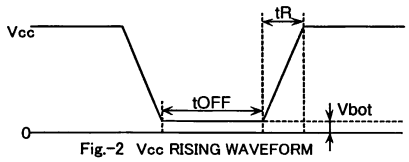


Fig.-2 Vcc RISING WAVEFORM

◇Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

◇ CAUTIONS ON USE

(1) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(3) Thermal design

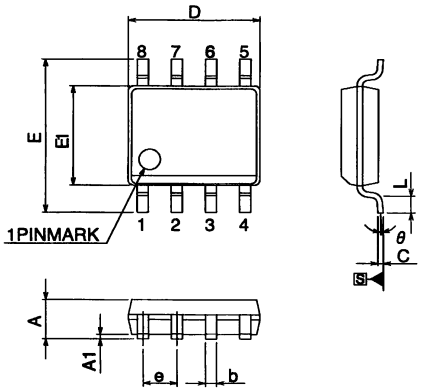
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION

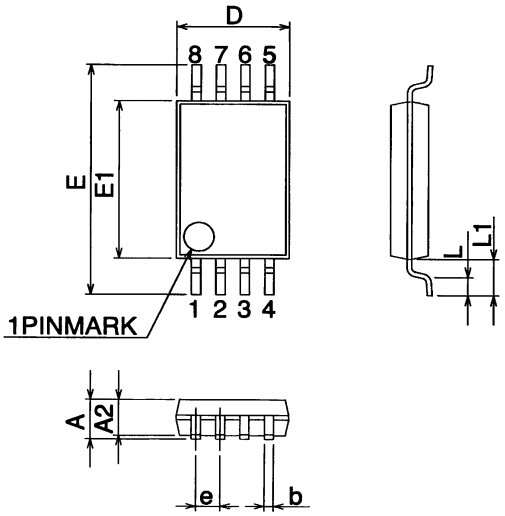


Notes
1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MS-012 variation AA.

Fig-4 8-lead JEDECSOIC Package Outline

◇ 8-lead JEDECSOIC Package Size Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	1.35	1.75	–	0.053	0.069
A1	–	0.10	0.25	–	0.004	0.010
b	–	0.31	0.51	–	0.012	0.020
c	–	0.17	0.25	–	0.007	0.010
D	–	4.80	5.00	–	0.189	0.197
e	1.27 BSC	–	–	0.050 BSC	–	–
E	–	5.79	6.20	–	0.228	0.244
E1	–	3.81	3.99	–	0.150	0.157
L	–	0.40	1.27	–	0.016	0.050
θ	–	0°	8°	–	0°	8°



Notes
1.This drawing is subject to change without notice.
2.Body dimensions do not include mold flash or protrusion, or gate burns.
3.Reference JEDEC MO-153.

Fig-5 8-lead TSSOP Package Outline

◇ 8-lead TSSOP Package Size Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	–	1.20	–	–	0.047
A2	1.00	0.80	1.05	0.039	0.031	0.041
b	–	0.19	0.30	–	0.007	0.012
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65 BSC	–	–	0.025	–	–
E	6.40 BSC	–	–	0.252	–	–
E1	4.40	4.30	4.50	0.173	0.169	0.177
L	0.60	0.45	0.75	0.023	0.017	0.030
L1	1.00 REF	–	–	0.039	–	–

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