

## Features

- Fast Read Access Time – 120 ns, see AT27BV020 for Faster Speeds
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V
  - or Standard 5V  $\pm$  10% Supply Range
- Compatible with JEDEC Standard AT27C020
- Low Power CMOS Operation
  - 20  $\mu$ A Max (Less than 1  $\mu$ A Typical) Standby for  $V_{CC} = 3.6V$
  - 29 mW Max Active at 5 MHz for  $V_{CC} = 3.6V$
- JEDEC Standard Packages
  - 32-lead PLCC
  - 32-lead TSOP
  - 32-lead VSOP
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming Algorithm – 100  $\mu$ s/Byte (Typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTTL
- Integrated Product Identification Code
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

## 1. Description

The AT27LV020A is a high-performance, low-power, low-voltage 2,097,152 bit one-time programmable read-only memory (OTP EPROM) organized as 256K by 8 bits. It requires only one supply in the range of 3.0 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At  $V_{CC} = 3.0V$ , any byte can be accessed in less than 120 ns. With a typical power dissipation of only 18 mW at 5 MHz and  $V_{CC} = 3.3V$ , the AT27LV020A consumes less than one fifth the power of a standard 5V EPROM. Standby mode supply current is typically less than 1  $\mu$ A at 3.3V.

The AT27LV020A is available in industry-standard JEDEC approved one-time programmable (OTP) plastic PLCC, TSOP, and VSOP. All devices feature two-line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to give designers the flexibility to prevent bus contention.

The AT27LV020A operating with  $V_{CC}$  at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at  $V_{CC} = 5.0V$ . The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27LV020A has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100  $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV020A programs exactly the same way as a standard 5V AT27C020 and uses the same programming equipment.



**2-Megabit  
(256K x 8)  
Low Voltage  
OTP EPROM**

**AT27LV020A**

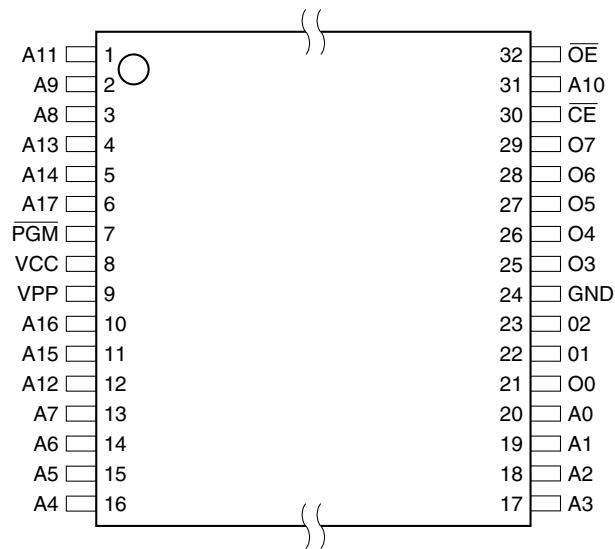
0549G-EPROM-12/07



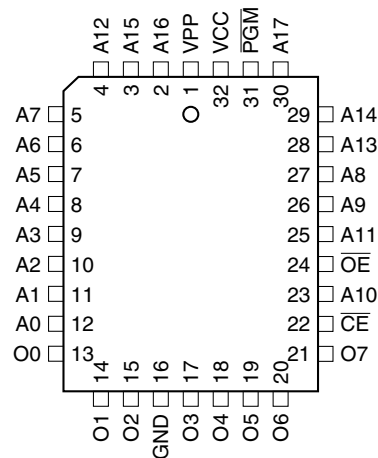
## 2. Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

### 2.1 32-lead TSOP/VSOP (Type 1) Top View



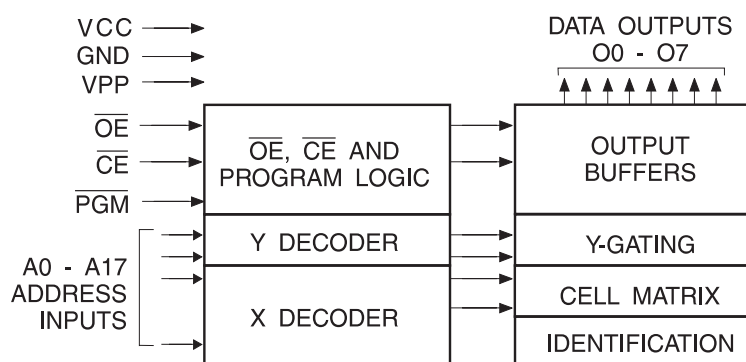
### 2.2 32-lead PLCC – Top View



## 3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu\text{F}$  high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be utilized, again connected between the  $V_{CC}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## 4. Block Diagram



## 5. Absolute Maximum Ratings\*

Temperature Under Bias.....	-40° C to +85° C
Storage Temperature .....	-65° C to +125° C
Voltage on any Pin with with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
$V_{PP}$ Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75\text{V}$  DC which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

## 6. Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V <sub>PP</sub>	V <sub>CC</sub>	Outputs
Read <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	X <sup>(1)</sup>	Ai	X	V <sub>CC</sub>	D <sub>OUT</sub>
Output Disable <sup>(2)</sup>	X	V <sub>IH</sub>	X	X	X	V <sub>CC</sub>	High Z
Standby <sup>(2)</sup>	V <sub>IH</sub>	X	X	X	X	V <sub>CC</sub>	High Z
Rapid Program <sup>(3)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Ai	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>IN</sub>
PGM Verify <sup>(3)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>OUT</sub>
PGM Inhibit <sup>(3)</sup>	V <sub>IH</sub>	X	X	X	V <sub>PP</sub>	V <sub>CC</sub>	High Z
Product Identification <sup>(3)(5)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	X	A9 = V <sub>H</sub> <sup>(4)</sup> A0 = V <sub>IH</sub> or V <sub>IL</sub> A1 - A17 = V <sub>IL</sub>	X	V <sub>CC</sub>	Identification Code

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Read, output disable, and standby modes require,  $3.0V \leq V_{CC} \leq 3.6V$ , or  $4.5V \leq V_{CC} \leq 5.5V$ .
  3. Refer to Programming Characteristics. Programming modes require V<sub>CC</sub> = 6.5V.
  4. V<sub>H</sub> = 12.0 ± 0.5V.
  5. Two identifier bytes may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A9 which is set to V<sub>H</sub> and A0 which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification byte and high (V<sub>IH</sub>) to select the Device Code byte.

## 7. DC and AC Operating Conditions for Read Operation

	AT27LV020A-12
Industrial Operating Temperature (Case)	-40° C - 85° C
V <sub>CC</sub> Power Supply	3.0V to 3.6V
	5V ± 10%

## 8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
<b>V<sub>CC</sub> = 3.0V to 3.6V</b>					
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μA
I <sub>PP1</sub> <sup>(2)</sup>	Read/Standby Current <sup>(1)</sup>	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
I <sub>SB</sub>	V <sub>CC</sub> Standby Current <sup>(1)</sup>	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		20	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		100	μA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, $\overline{CE} = V_{IL}$		8	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.0 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2.0 mA	2.4		V
<b>V<sub>CC</sub> = 4.5V to 5.5V</b>					
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μA
I <sub>PP1</sub> <sup>(2)</sup>	Read/Standby Current <sup>(1)</sup>	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
I <sub>SB</sub>	V <sub>CC</sub> Standby Current <sup>(1)</sup>	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5 MHz, I <sub>OUT</sub> = 0 mA, $\overline{CE} = V_{IL}$		25	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

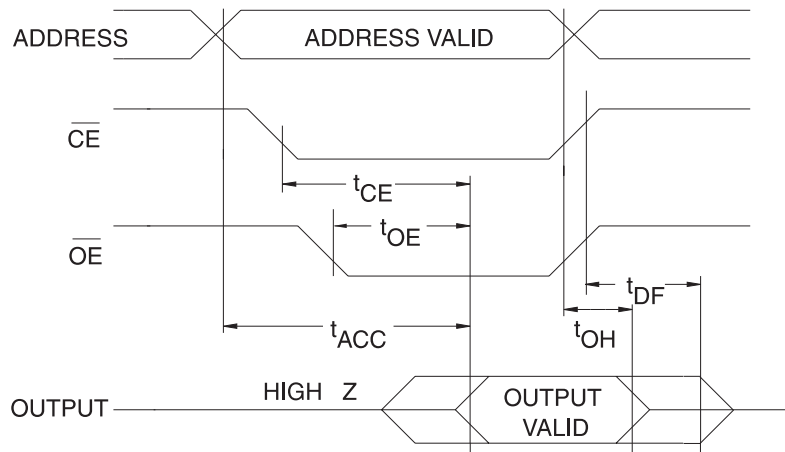
- Notes: 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously with or after V<sub>PP</sub>  
 2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP</sub>

## 9. AC Characteristics for Read Operation

$V_{CC} = 3.0V$  to  $3.6V$  and  $4.5V$  to  $5.5V$

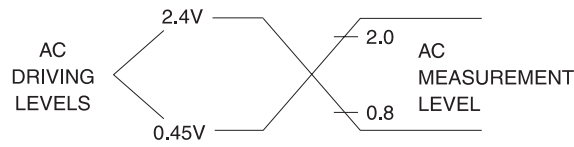
Symbol	Parameter	Condition	AT27LV020A-12		Units
			Min	Max	
$t_{ACC}^{(3)}$	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120	ns
$t_{CE}^{(2)}$	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120	ns
$t_{OE}^{(2)(3)}$	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50	ns
$t_{DF}^{(4)(5)}$	$\overline{OE}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First			40	ns
$t_{OH}$	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ , Whichever Occurred First		0		ns

## 10. AC Waveforms for Read Operation



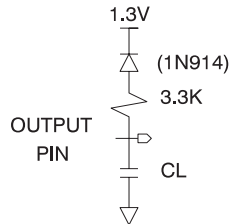
- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
  2.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
  3.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
  4. This parameter is only sampled and is not 100% tested.
  5. Output float is defined as the point when data is no longer driven.

### 11. Input Test Waveform and Measurement Level



$t_R, t_F < 20 \text{ ns (1\% to 90\%)}$

### 12. Output Test Load



Note: CL = 1 pF including jig capacitance.

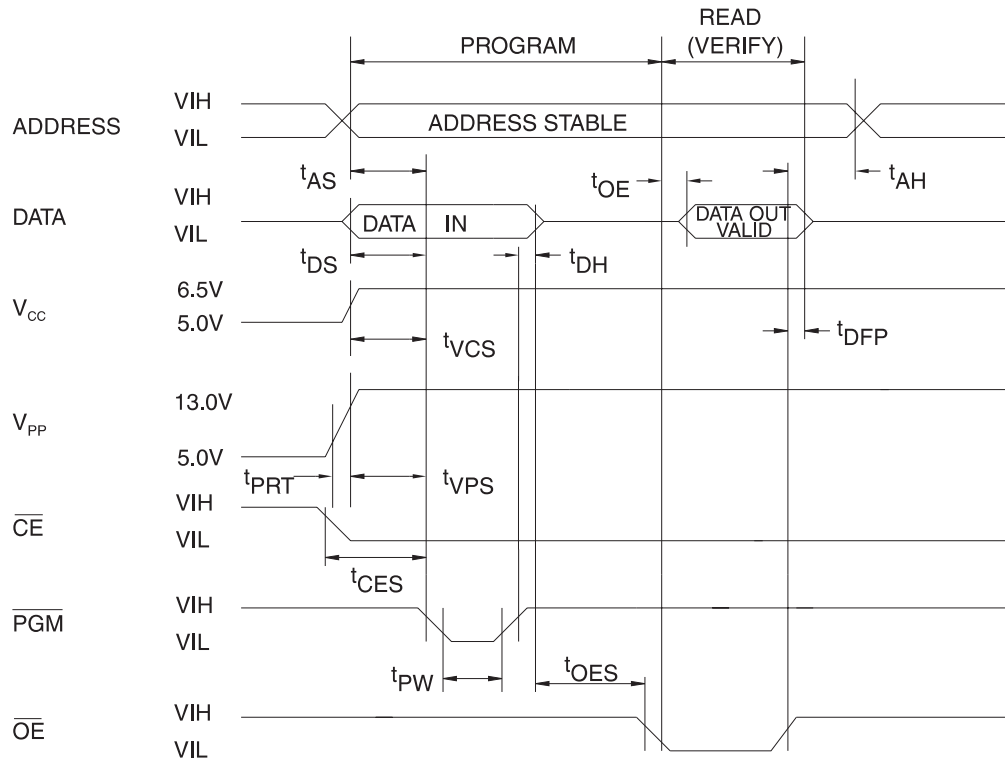
### 13. Pin Capacitance

f = 1 MHz, T = 25° C<sup>(1)</sup>

Symbol	Typ	Max	Units	Conditions
C <sub>IN</sub>	4	8	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	8	12	pF	V <sub>OUT</sub> = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## 14. Programming Waveforms<sup>(1)</sup>



- Notes:
1. The Input Timing Reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
  2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.
  3. When programming the AT27LV020A a 0.1  $\mu\text{F}$  capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.



## 15. DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		$\pm 10$	$\mu\text{A}$
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC} + 0.5$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1\text{ mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400\ \mu\text{A}$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program and Verify)			40	mA
$I_{PP2}$	$V_{PP}$ Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
$V_{ID}$	A9 Product Identification Voltage		11.5	12.5	V

## 16. AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20 ns	2		$\mu\text{s}$
$t_{CES}$	$\overline{CE}$ Setup Time		2		$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ Setup Time		2		$\mu\text{s}$
$t_{DS}$	Data Setup Time		2		$\mu\text{s}$
$t_{AH}$	Address Hold Time	Input Pulse Levels 0.45V to 2.4V	0		$\mu\text{s}$
$t_{DH}$	Data Hold Time		2		$\mu\text{s}$
$t_{DFP}$	$\overline{OE}$ High to Output Float Delay <sup>(3)</sup>	Input Timing Reference Level 0.8V to 2.0V	0	130	ns
$t_{VPS}$	$V_{PP}$ Setup Time		2		$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time		2		$\mu\text{s}$
$t_{PW}$	$\overline{PGM}$ Program Pulse Width <sup>(2)</sup>	Output Timing Reference Level 0.8V to 2.0V	95	105	$\mu\text{s}$
$t_{OE}$	Data Valid from $\overline{OE}$			150	ns
$t_{PRT}$	$V_{PP}$ Pulse Rise Time During Programming		50		ns

- Notes:
- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$
  - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
  - Program Pulse width tolerance is  $100\ \mu\text{sec} \pm 5\%$ .

## 17. Atmel's AT27LV020A Integrated Product Identification Code<sup>(1)</sup>

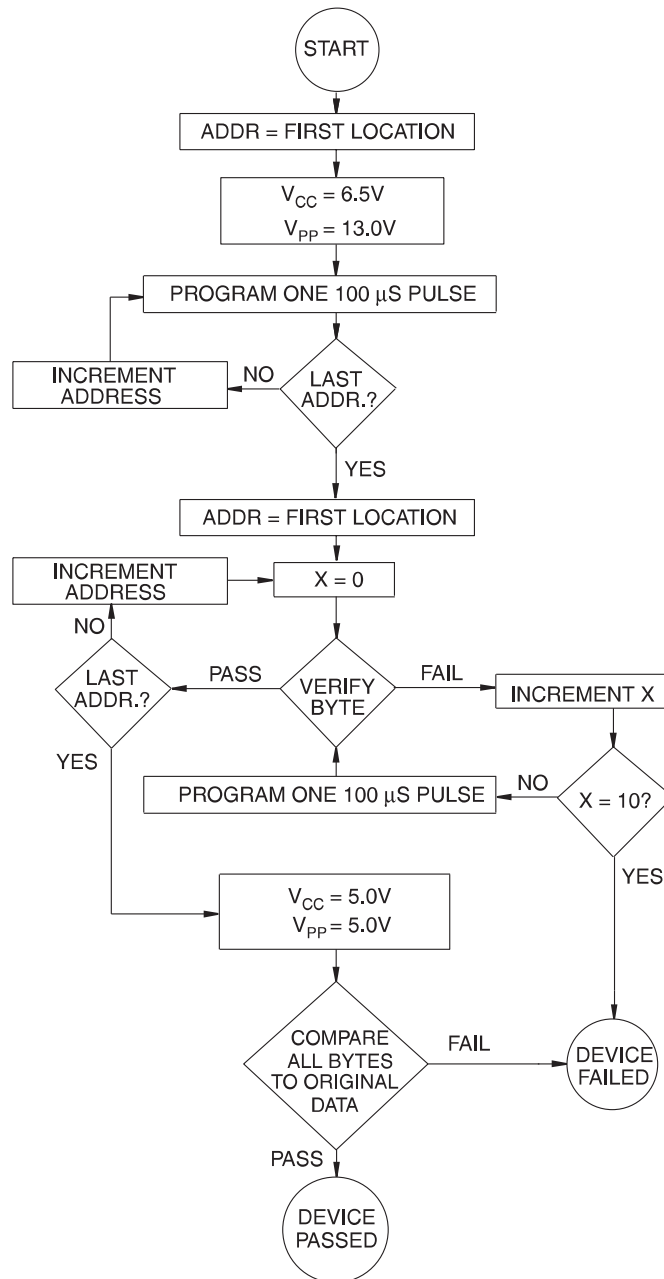
Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	1	0	86

Note: 1. The AT27LV020A has the same Product Identification Code as the AT27C020. Both are programming compatible.



## 18. Rapid Programming Algorithm

A 100  $\mu\text{s}$   $\overline{\text{PGM}}$  pulse width is used to program. The address is set to the first location.  $V_{\text{CC}}$  is raised to 6.5V and  $V_{\text{PP}}$  is raised to 13.0V. Each address is first programmed with one 100  $\mu\text{s}$   $\overline{\text{PGM}}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100  $\mu\text{s}$  pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $V_{\text{PP}}$  is then lowered to 5.0V and  $V_{\text{CC}}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



## 19. Ordering Information

### 19.1 Standard Package

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA) V <sub>CC</sub> = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
120	8	0.02	AT27LV020A-12JI AT27LV020A-12TI AT27LV020A-12VI	32J 32T 32V <sup>(1)</sup>	Industrial (-40° C to 85° C)

Note:  Not recommended for new designs. Use Green package option.

### 19.2 Green Package Option (Pb/Halide-free)

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA) V <sub>CC</sub> = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
120	8	0.02	AT27LV020A-12JU AT27LV020A-12TU AT27LV020A-12VU	32J 32T 32V <sup>(1)</sup>	Industrial (-40° C to 85° C)

Note: 1. The 32-lead VSOP package is not recommended for new designs.

Package Type	
<b>32J</b>	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
<b>32T</b>	32-Lead, Plastic Thin Small Outline Package (TSOP)
<b>32V</b>	32-Lead, Plastic Thin Small Outline Package (VSOP)

## 20. Packaging Information

### 20.1 32J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)**

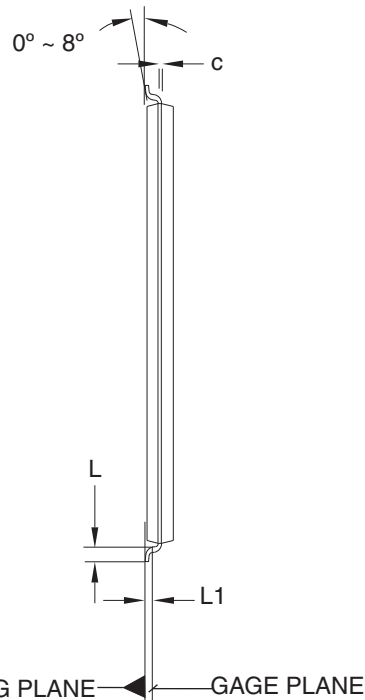
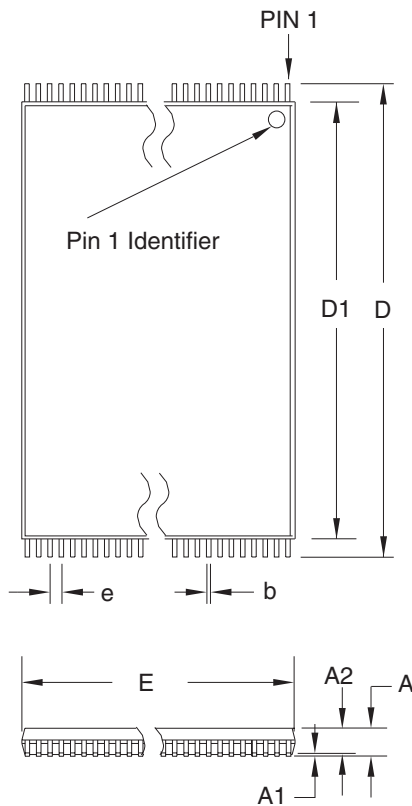
**DRAWING NO.**

32J

**REV.**

B

20.2 32T –TSOP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
  2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
  3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)

**DRAWING NO.**

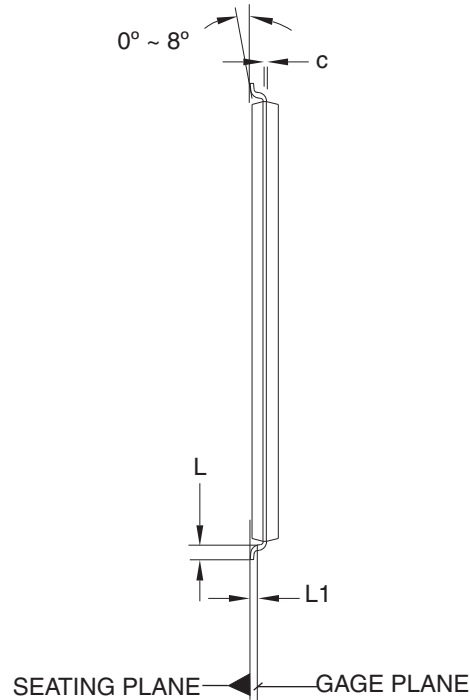
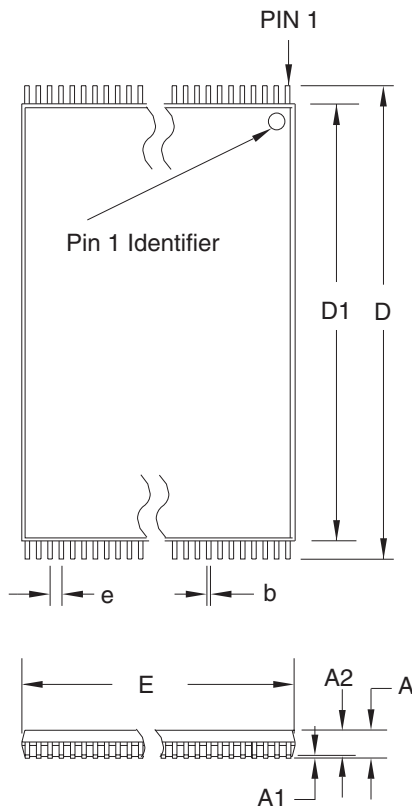
32T

**REV.**

B



### 20.3 32V –VSOP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	13.80	14.00	14.20	
D1	12.30	12.40	12.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BA.
  2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
  3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32V, 32-lead (8 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP)**

**DRAWING NO.**

32V

**REV.**

B



## Headquarters

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