Features

- Write Protect Pin for Hardware Data Protection
  - Utilizes Different Array Protection Compared to the AT24C04B
- Low-voltage and Standard-voltage Operation
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 512 x 8 (4K)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V) and 400 kHz (1.8V, 2.5V, 2.7V) Clock Rate
- 16-byte Page
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms Max)
- High Reliability
  - Endurance: One Million Write Cycles
  - Data Retention: 100 Years
- 8-lead PDIP, 8-lead JEDEC SOIC and 8-lead TSSOP Packages
- Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers

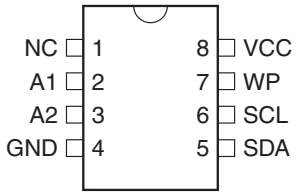
Description

The AT24HC04B provides 4096 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24HC04B is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC and 8-lead TSSOP packages and is accessed via a two-wire serial interface. In addition, the entire family is available in 1.8V (1.8V to 5.5V) version.

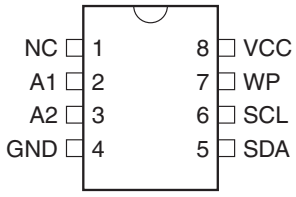
Table 0-1. Pin Configuration

Pin Name	Function
A1, A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No-connect

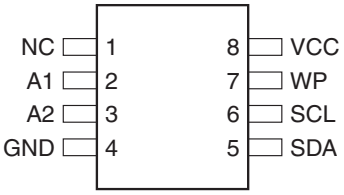
8-lead TSSOP



8-lead PDIP



8-lead SOIC



Two-wire Serial EEPROM

4K (512 x 8)

AT24HC04B

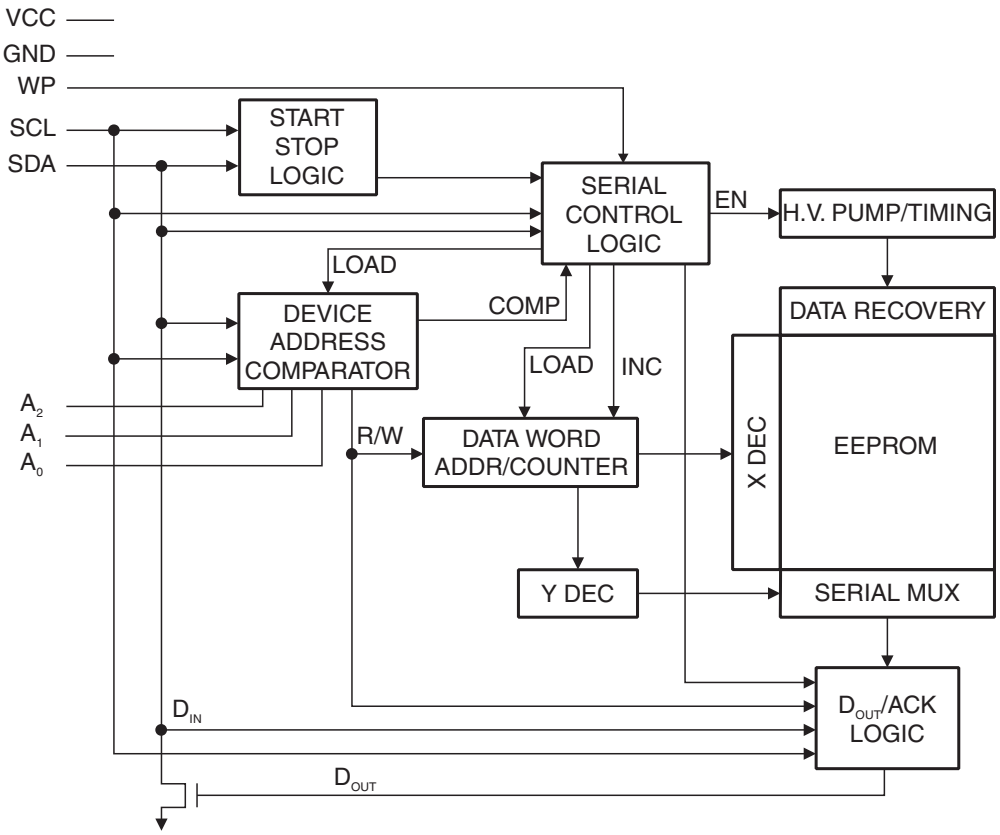
5227E–SEEPR–11/08

Absolute Maximum Ratings*

Operating Temperature	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-1. Block Diagram



1. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2 and A1 pins are device address inputs that must be hardwired for the AT24HC04B. As many as four 4K devices may be addressed on a single bus system. The A0 pin is a no-connect. (Device addressing and Page addressing are discussed in detail under *Device Addressing and Page Addressing,* page 8).

WRITE PROTECT (WP): The AT24HC04B has a WP pin that provides hardware data protection. The WP pin allows normal read/write operations when connected to ground (GND). When the WP pin is connected to V_{CC}, the write protection feature is enabled and operates as shown.

Table 1-1. Write Protect

WP Pin Status	Part of the Array Protected
	24HC04B
At V_{CC}	Upper Half (2K) Array
At GND	Normal Read/Write Operations

2. Memory Organization

AT24HC04B, 4K SERIAL EEPROM: The 4K is internally organized with 32 pages of 16 bytes each. Random word addressing requires an 9-bit data word address.

Table 2-1. Pin Capacitance[1]

Applicable over recommended operating range from T_{AI} = 25°C, f = 1.0 MHz, V_{CC} = +1.8V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 2-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level [1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level [1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 2-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

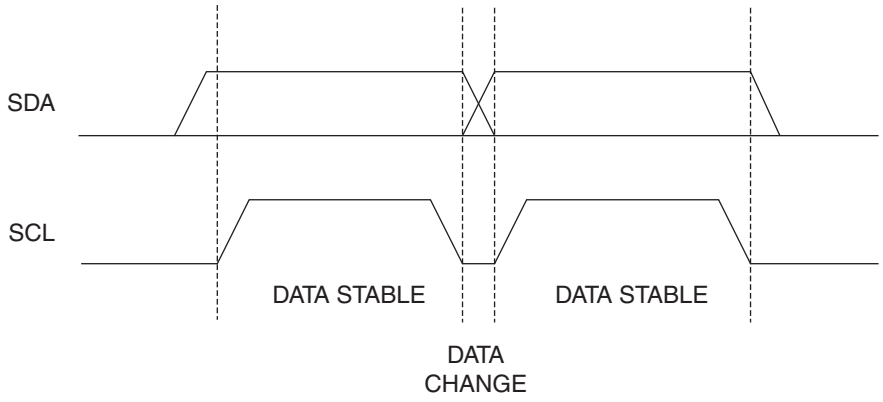
Symbol	Parameter	1.8, 2.5, 2.7		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time		50		40	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Setup Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Setup Time	0.6		.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	5.0V, 25°C, Byte Mode	1 Million				Write Cycles

Note: 1. This parameter is ensured by characterization only.

3. Device Operation

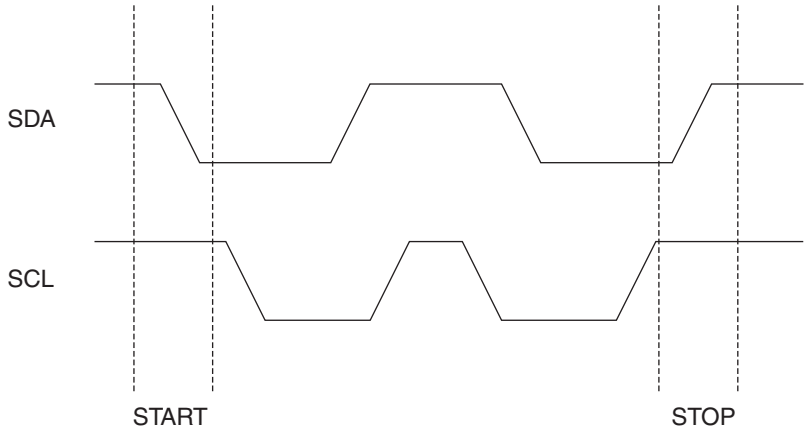
CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 3-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure 3-1. Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command (see Figure 3-2).

Figure 3-2. Start and Stop Definition



STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 3-2).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24HC04B features a low-power standby mode that is enabled: (a) upon power-up and (b) after the receipt of the Stop bit and the completion of any internal operations.

2-WIRE SOFTWARE RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be protocol reset by following these steps: (a) Create a start bit condition, (b) Clock nine cycles, (c) Create another start bit followed by stop bit condition as shown below. The device is ready for next communication after above steps have been completed.

Figure 3-3. Software Reset

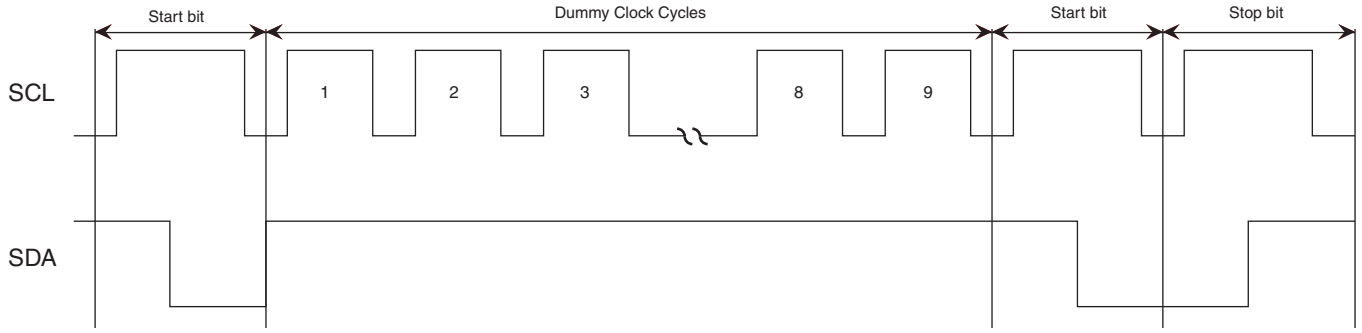


Figure 3-4. Bus Timing

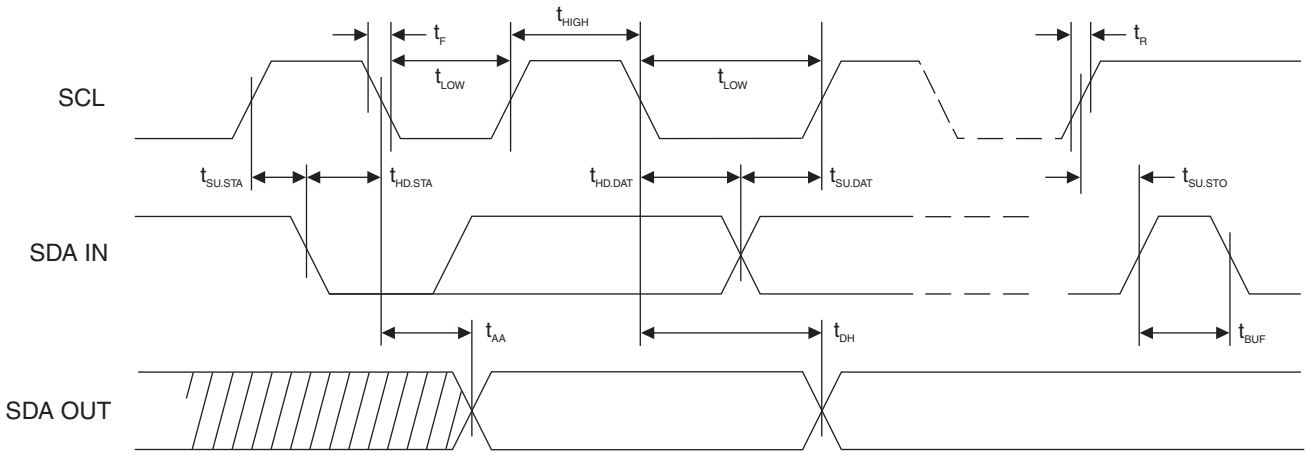
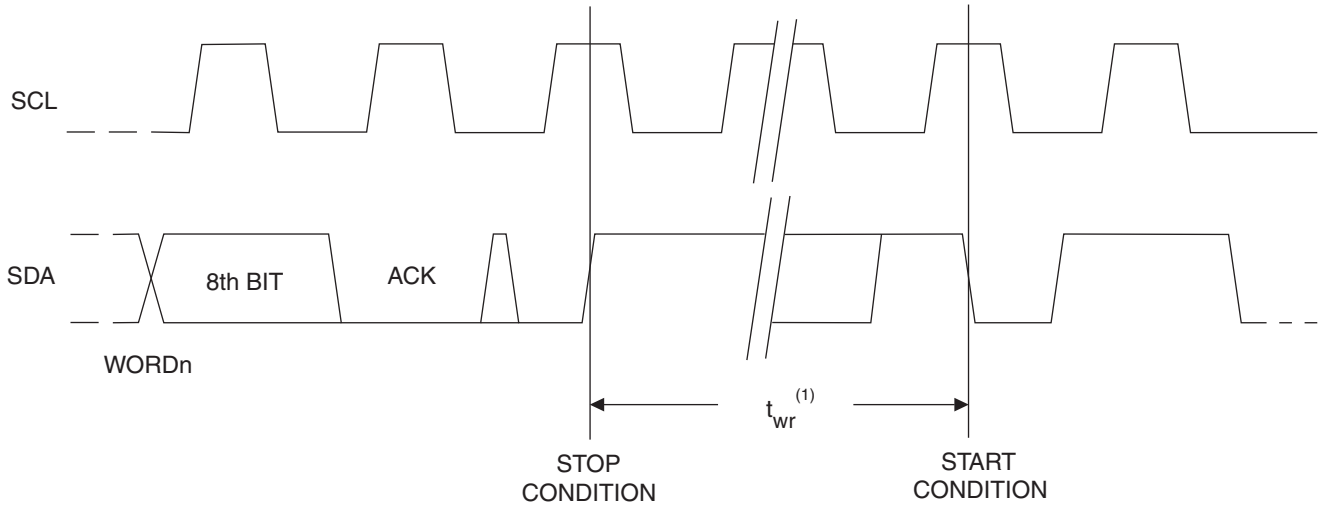
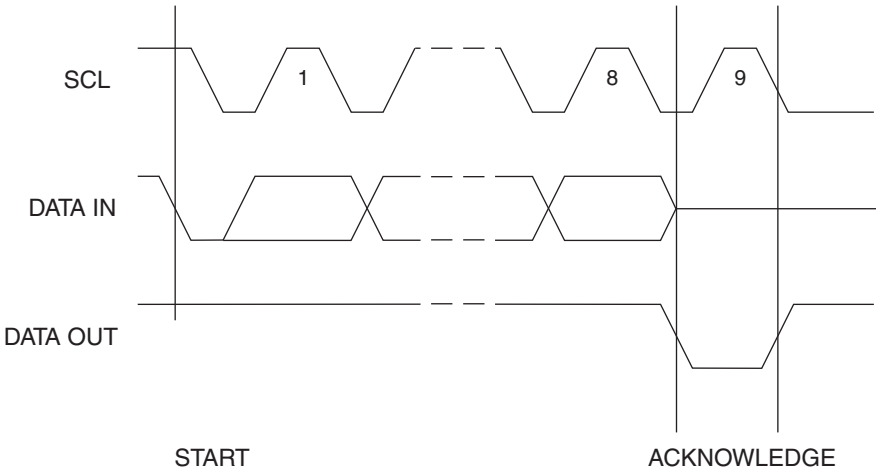


Figure 3-5. Write Cycle Timing



Notes: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

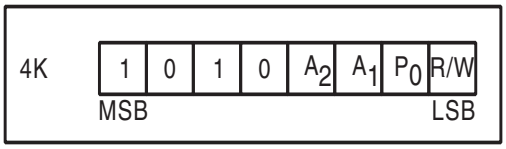
Figure 3-6. Output Acknowledge



4. Device Addressing and Page Addressing

The 4K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation, as shown in Figure 4-1.

Figure 4-1. Device Address



The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next two bits are the A2 and A1 device address bits for the 4K EEPROM. These two bits must compare to their corresponding hardwired input pins. The A0 pin is a no-connect.

The next bit is the memory page address bit. This bit is the MSB of the 9-bit data word address.

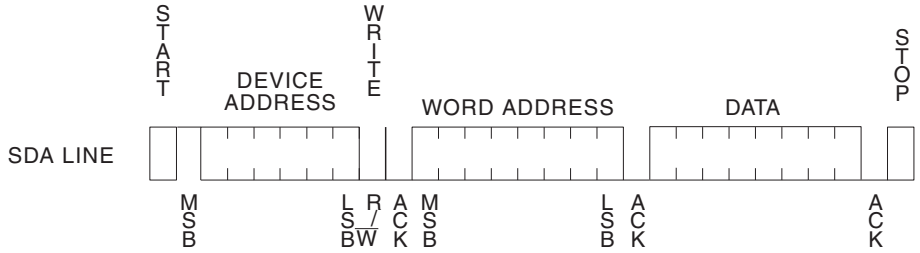
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the chip will return to a standby state.

5. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgement. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time, the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete, see Figure 5-1 on page 9.

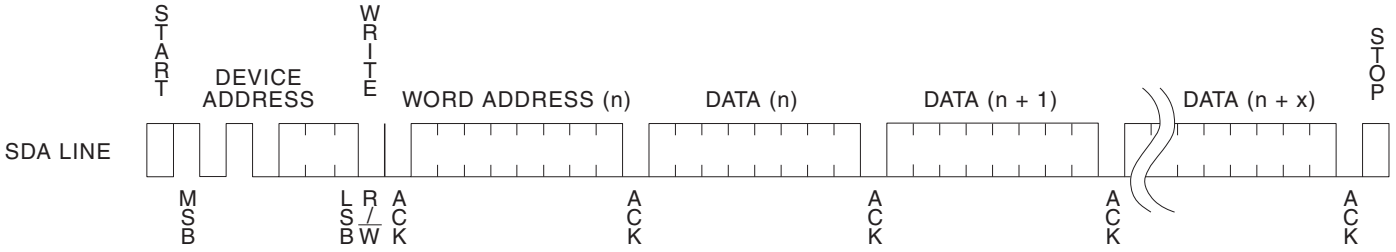
Figure 5-1. Byte Write



PAGE WRITE: The 4K EEPROM is capable of a 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition, see Figure 5-2.

Figure 5-2. Page Write



The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a “0” allowing the read or write sequence to continue.

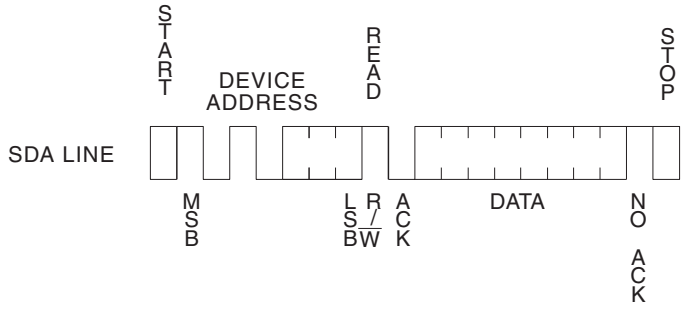
6. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

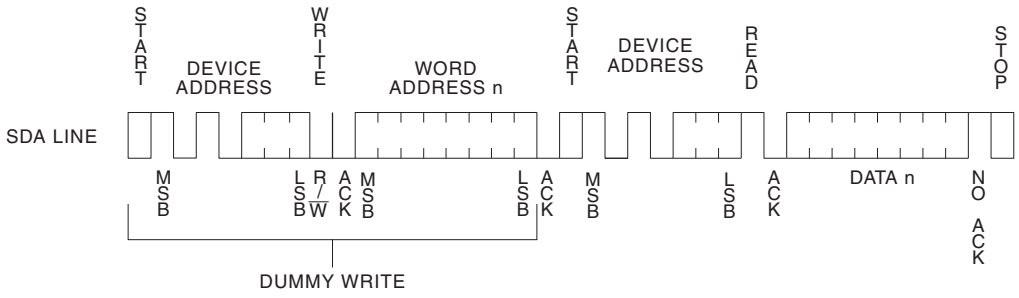
Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition, see Figure 6-1.

Figure 6-1. Current Address Read



RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition, see Figure 6-2.

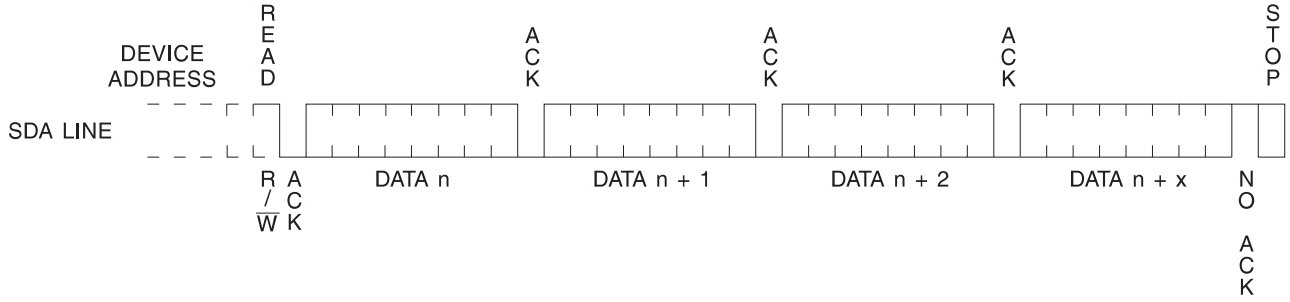
Figure 6-2. Random Read



SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment

the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition, see Figure 6-3.

Figure 6-3. Sequential Read



7. AT24HC04B Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24HC04B-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT24HC04BN-SH-B[1] (NiPdAu Lead Finish)	1.8	8S1	
AT24HC04BN-SH-T[2] (NiPdAu Lead Finish)	1.8	8S1	
AT24HC04B-TH-B[1] (NiPdAu Lead Finish)	1.8	8A2	
AT24HC04B-TH-T[2] (NiPdAu Lead Finish)	1.8	8A2	
AT24HC04B-W-11[3]	1.8	Die Sale	Industrial Temperature (–40°C to 85°C)

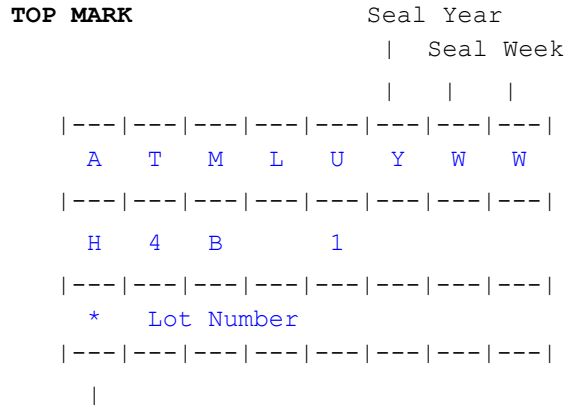
Notes:
1. "-B" denotes bulk.
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP = 5K per reel.
3. Available in tape and reel and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

Package Type	
8P3	8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
Options	
–1.8	Low Voltage (1.8V to 5.5V)

8. Part marking scheme

8-PDIP

TOP MARK



Y = SEAL YEAR		WW = SEAL WEEK
6: 2006	0: 2010	02 = Week 2
7: 2007	1: 2011	04 = Week 4
8: 2008	2: 2012	:: : :::: :
9: 2009	3: 2013	:: : :::: ::
		50 = Week 50
		52 = Week 52

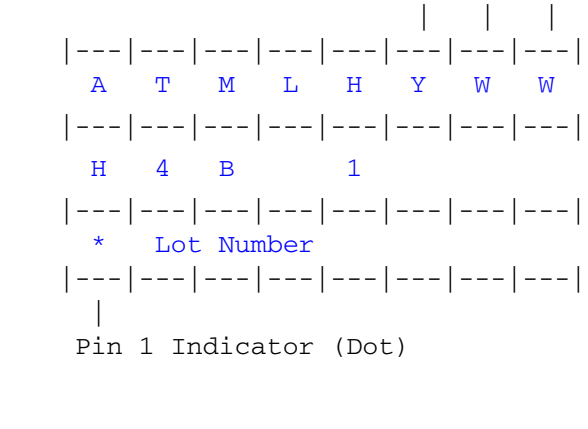
Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark

8-SOIC

TOP MARK



Y = SEAL YEAR		WW = SEAL WEEK
6: 2006	0: 2010	02 = Week 2
7: 2007	1: 2011	04 = Week 4
8: 2008	2: 2012	:: : :::: :
9: 2009	3: 2013	:: : :::: ::
		50 = Week 50
		52 = Week 52

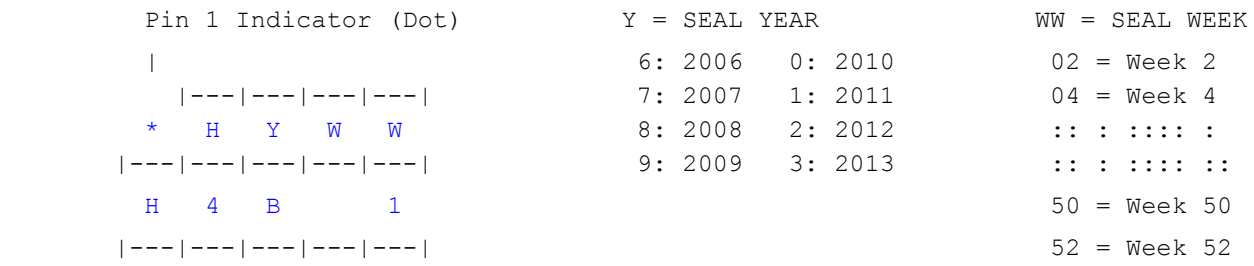
Lot Number to Use ALL Characters in Marking

BOTTOM MARK

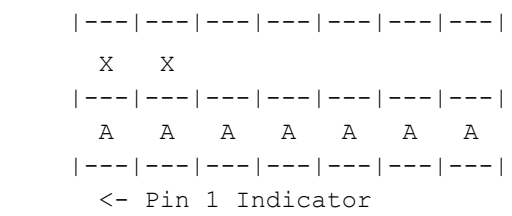
No Bottom Mark

8-TSSOP

TOP MARK



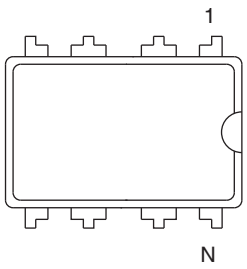
BOTTOM MARK



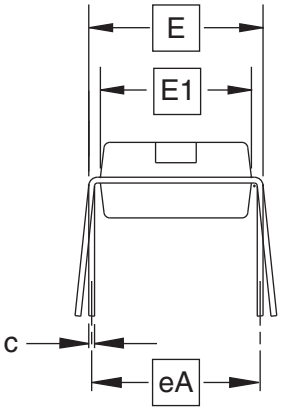
TOP MARK Seal Year Y = SEAL YEAR WW = SEAL WEEK

9. Packaging Information

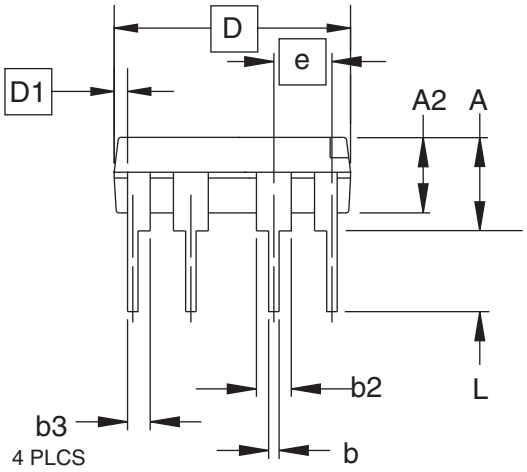
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

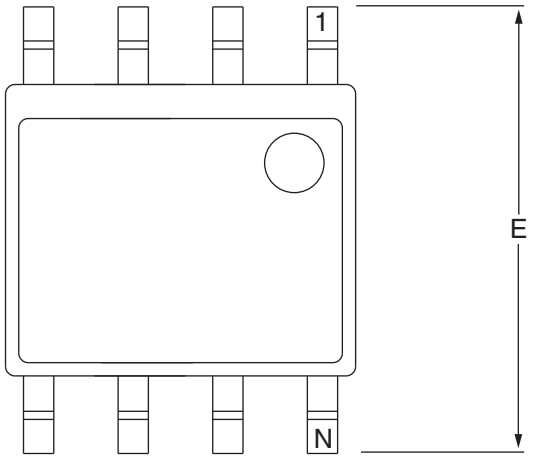
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	–	–	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

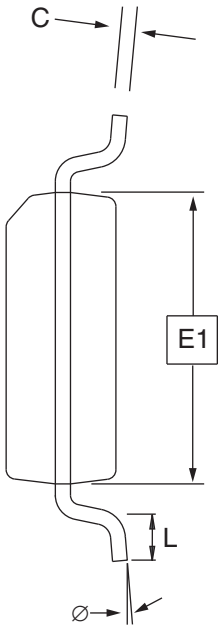
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

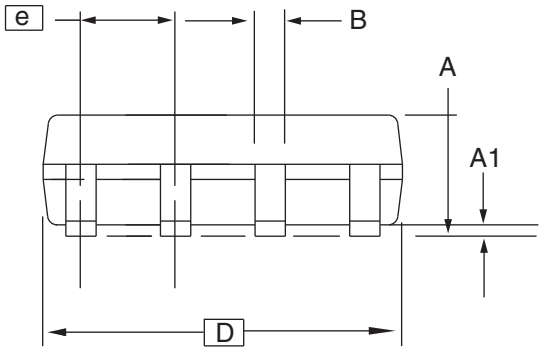
8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

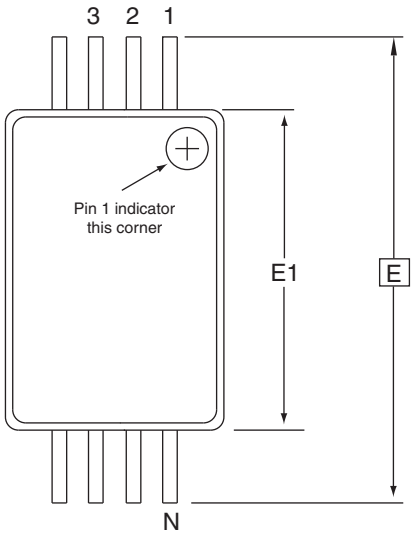
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

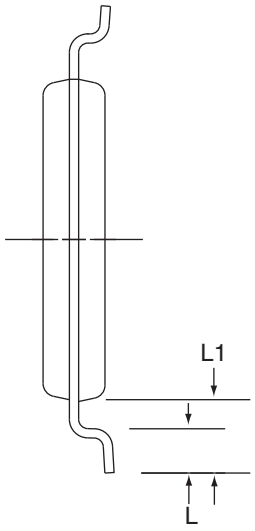
10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

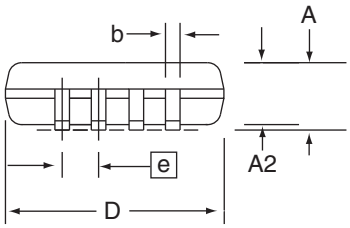
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

Revision History

Doc. Rev.	Date	Comments
5227E	11/2008	Updated pin configurations
5227D	1/2008	Removed ‘preliminary’ status
5227C	8/2007	Added Part Marking Scheme
5227B	8/2007	Updated to new template Updated Common figures Added Part Marking tables
5227A	4/2007	Initial document release.

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