MICROCHIP®

24AA014/24LC014

1K I^{2}C™ Serial EEPROM

Device Selection Table

| Part Number	Vcc Range	Max Clock	Temp. Range
24AA014	1.8V - 5.5V	400 kHz[(1)]	I
24LC014	2.5V - 5.5V	400 kHz	I

Note 1: 100 kHz for V$_{CC}$ < 2.5V

Features:

- Single-supply with operation down to 1.8V
- Low-power CMOS technology:
  - 1 mA active current, typical
  - 1 μA standby current, typical at 5.5V
- Organized as a single block of 128 bytes (128 x 8)
- Hardware write protection for entire array
- 2-wire serial interface bus, I^{2}C™ compatible
- 100 kHz and 400 kHz clock compatibility
- Page write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- 5 ms max. write cycle time
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC, TSSOP, DFN and MSOP packages
- Available for extended temperature ranges:
 - Industrial (I):   -40°C to   +85°C

Description:

The Microchip Technology Inc. 24AA014/24LC014 is a 1 Kbit Serial Electrically Erasable PROM with operation down to 1.8V. The device is organized as a single block of 128 x 8-bit memory with a 2-wire serial interface. Low-current design permits operation with typical standby and active currents of only 1 μA and 1 mA, respectively. The device has a page write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24AA014/24LC014 devices on the same bus for up to 8 Kbits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), TSSOP, 2x3 DFN and MSOP packages.

Package Types
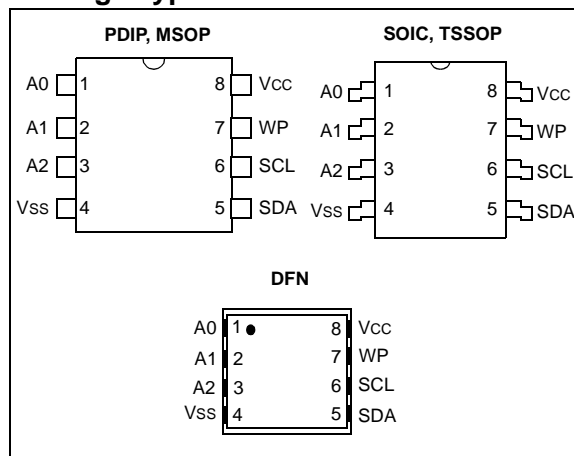
Block Diagram
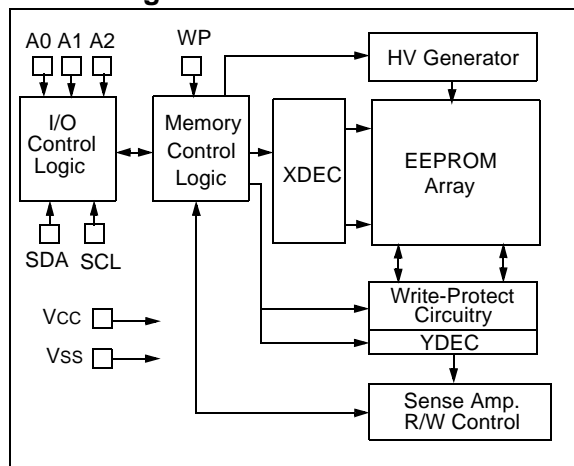
Pin Function Table

Name	Function
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
Vcc	Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write-Protect

© 2005 Microchip Technology Inc.

24AA014/24LC014

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [†]

Vcc..6.5V

All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V

Storage temperature ....-65°C to +150°C

Ambient temperature with power applied..-65°C to +125°C

ESD protection on all pins ....≥ 4 kV

> † NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

| All parameters apply across the specified operating ranges unless otherwise noted.	V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C				
Parameter	Symbol	Min.	Max.	Units	Conditions
SCL and SDA pins: High-level input voltage	V_{IH}	0.7 V_{CC}	—	V	
Low-level input voltage	V_{IL}	—	0.3 V_{CC}	V	
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.05 V_{CC}	—	V	**(Note 1)**
Low-level output voltage	V_{OL}	—	0.40	V	I_{OL} = 3.0 mA, V_{CC} = 4.5V I_{OL} = 2.1 mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	—	±1	µA	V_{IN} = Vss or Vcc, WP = Vss
Output leakage current	I_{LO}	—	±1	µA	V_{OUT} = Vss or Vcc
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	V_{CC} = 5.0V **(Note 1)** T_A = 25°C, f = 1 MHz
Operating current	I_{CC} Read	—	1	mA	V_{CC} = 5.5V, SCL = 400 kHz
	I_{CC} Write	—	3	mA	V_{CC} = 5.5V
Standby current	I_{CCS}	—	1	µA	V_{CC} = 5.5V, SDA = SCL = V_{CC} WP = Vss, A0, A1, A2 = Vss

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.		Vcc = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C					
Parameter	Symbol	Vcc = 1.8V - 5.5V STD MODE		Vcc = 2.5V - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
Start condition hold time	THD:STA	4000	—	600	—	ns	After this period, the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
Stop condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWC	—	5	—	5	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, (Note 4)

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be downloaded from Microchip's web site at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA
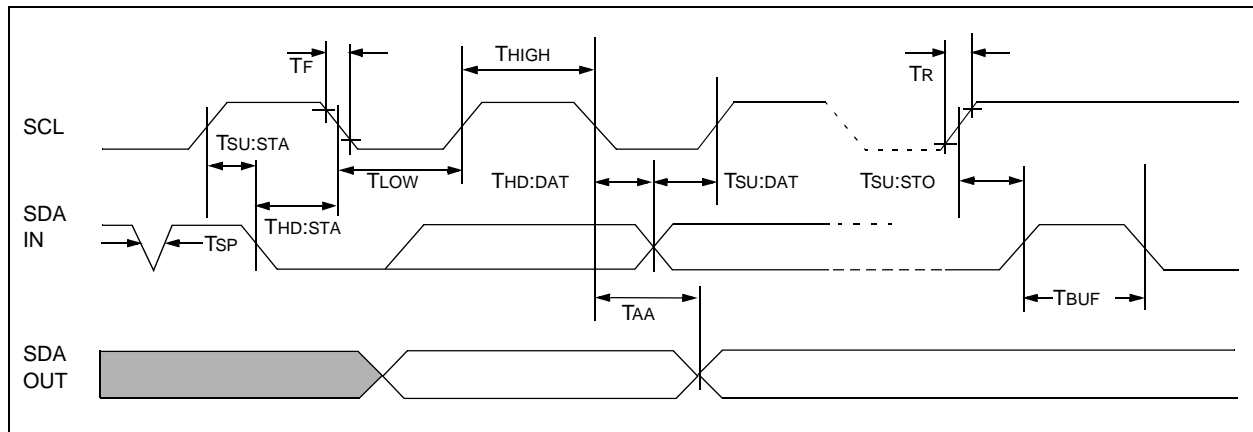
24AA014/24LC014

2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to V$_{CC}$ (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.2 SCL Serial Clock

The SCL input is used to synchronize the data transfer to and from the device.

2.3 A0, A1, A2

The levels on the inputs A0, A1 and A2 are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24AA014/24LC014 devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either V$_{CC}$ or V$_{SS}$.

2.4 WP

WP is the hardware write-protect pin. It must be tied to V$_{CC}$ or V$_{SS}$. If tied to V$_{CC}$, the hardware write protection is enabled. If the WP pin is tied to V$_{SS}$ the hardware write protection is disabled.

2.5 Noise Protection

The 24AA014/24LC014 employs a V$_{CC}$ threshold detector circuit that disables the internal erase/write logic if the V$_{CC}$ is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits that suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24AA014/24LC014 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device that generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions while the 24AA014/24LC014 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0   BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1   Bus Not Busy (A)

Both data and clock lines remain high.

4.2   Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3   Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4   Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited, though only the last sixteen will be stored when doing a write operation. When an over-write does occur, it will replace data in a first-in first-out fashion.
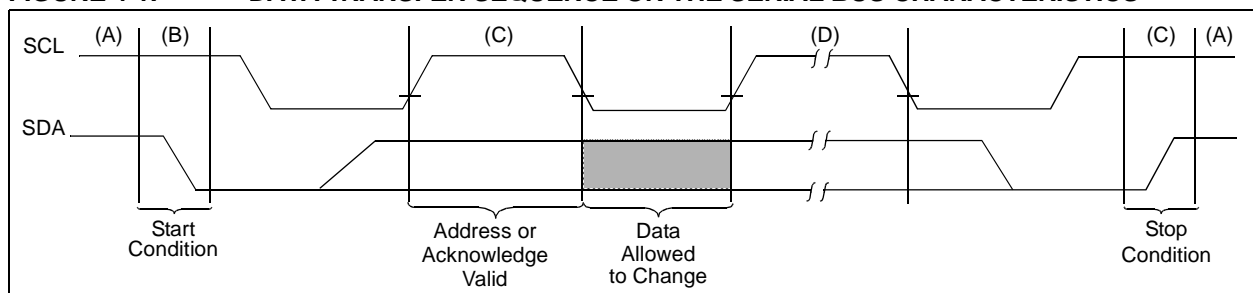
4.5   Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

> **Note:**   The 24AA014/24LC014 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition (Figure 4-2).

FIGURE 4-1:   **DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS**

**FIGURE 4-2:**   **ACKNOWLEDGE TIMING**
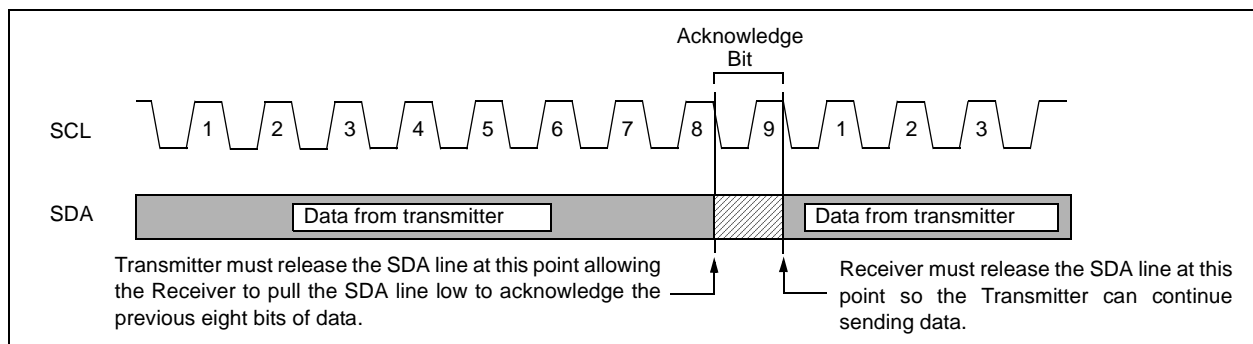
5.0   DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a four-bit control code; for the 24AA014/24LC014 this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24AA014/24LC014 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected. Following the Start condition, the 24AA014/24LC014 monitors the SDA bus, checking the control byte being transmitted. Upon receiving a '1010' code and appropriate Chip Select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{\text{W}}$ bit, the 24AA014/24LC014 will select a read or write operation.

FIGURE 5-1:   CONTROL BYTE FORMAT
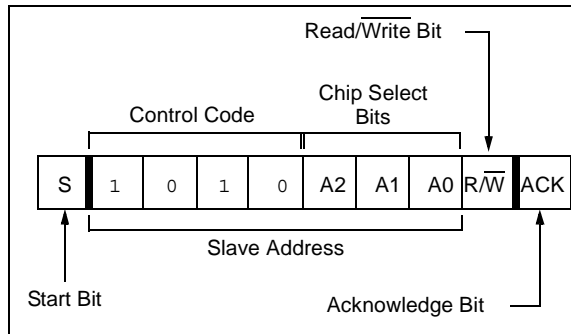
5.1   Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 8K bits by adding up to eight 24AA014/24LC014 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the Chip Select bits (3 bits) and the R/$\overline{W}$ bit (which is a logic low) are placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24AA014/24LC014. After receiving another Acknowledge signal from the 24AA014/24LC014, the master device will transmit the data word to be written into the addressed memory location. The 24AA014/24LC014 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and the 24AA014/24LC014 will not generate Acknowledge signals during this time (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if write protection is enabled.

6.2 Page Write

The write-control byte, word address and the first data byte are transmitted to the 24AA014/24LC014 in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 24AA014/24LC014 that are temporarily stored in the on-chip page buffer and will be written into the memory once the master has transmitted a Stop condition. Upon receipt of each word, the four lower order Address Pointer bits are internally incremented by one.

The higher order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if write protection is enabled.

> **Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary that the application software prevent page write operations that would attempt to cross a page boundary.
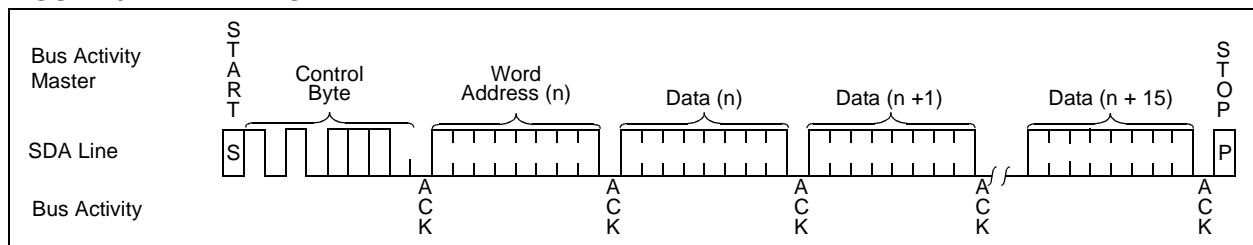
6.3 Write Protection

The WP pin must be tied to V_{CC} or V_{SS}. If tied to V_{CC}, the entire array will be write-protected. If the WP pin is tied to V_{SS}, write operations to all address locations are allowed.

FIGURE 6-1: BYTE WRITE
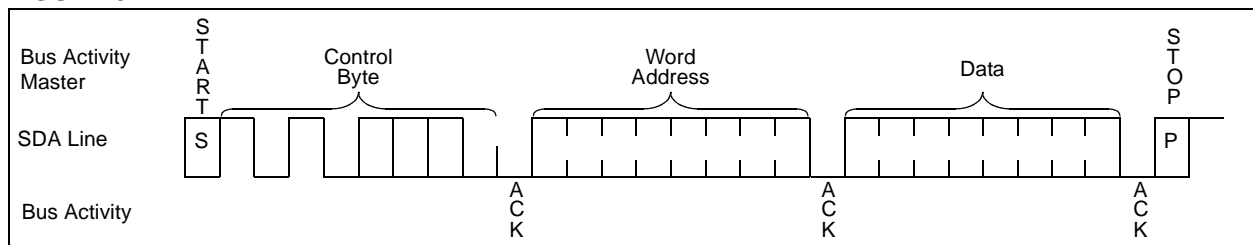
FIGURE 6-2: PAGE WRITE

7.0   ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the master, the device initiates the internally-timed write cycle and ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1:   **ACKNOWLEDGE POLLING FLOW**
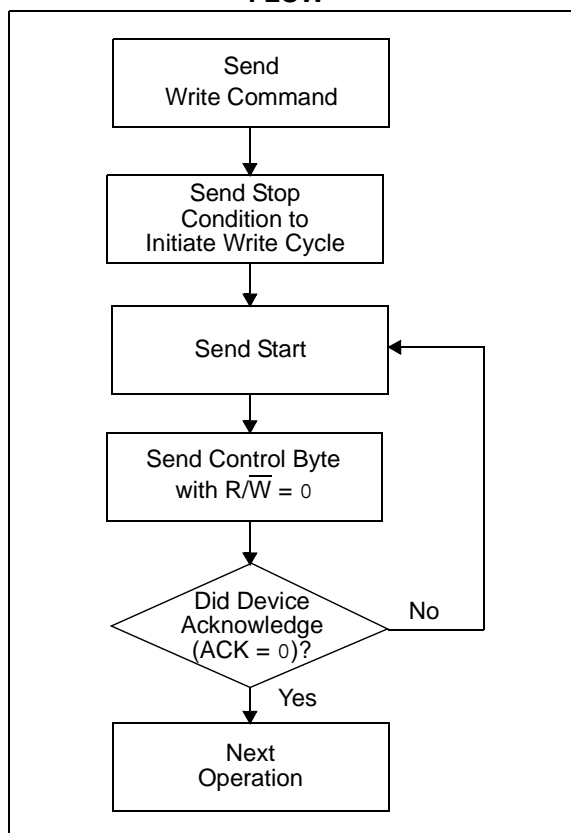
8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24AA014/24LC014 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to '1', the 24AA014/24LC014 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24AA014/24LC014 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24AA014/24LC014 as part of a write operation.

Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The 24AA014/24LC014 will then issue an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24AA014/24LC014 discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA014/24LC014 transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24AA014/24LC014 to transmit the next sequentially addressed 8-bit word (Figure 8-3).
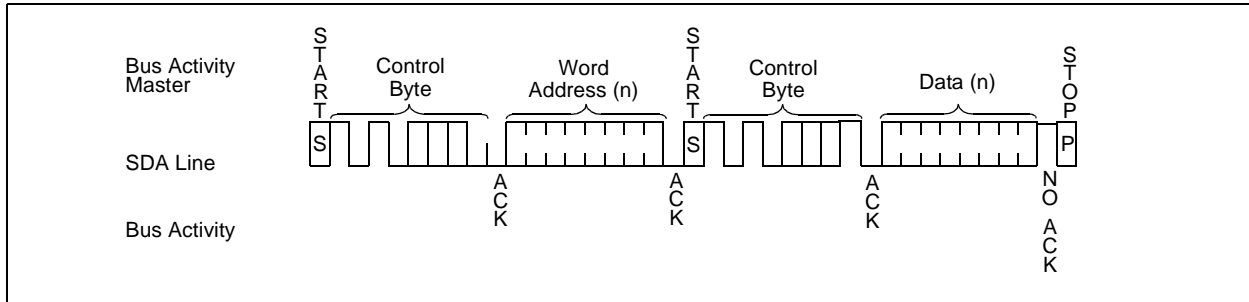
To provide sequential reads the 24AA014/24LC014 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address 0FFh to address 000h.
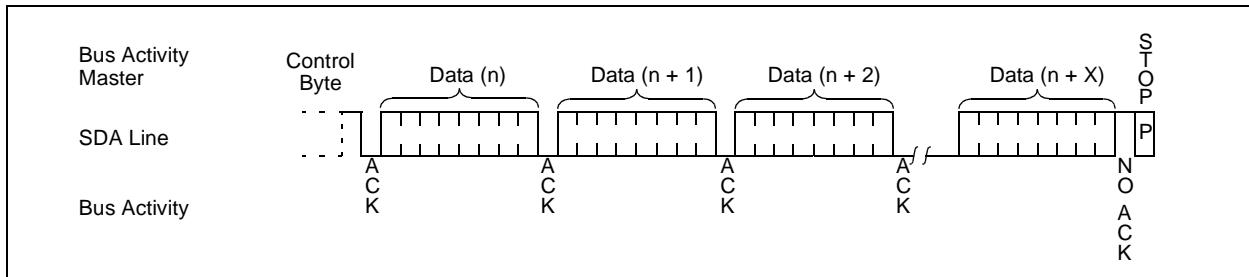
FIGURE 8-1: CURRENT ADDRESS READ
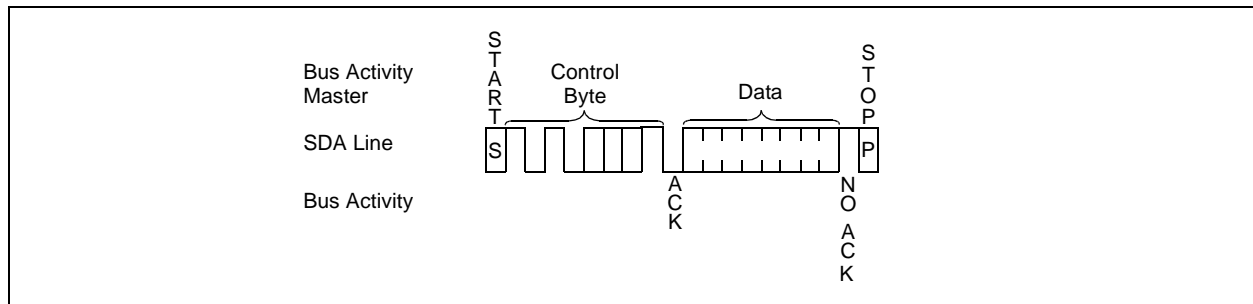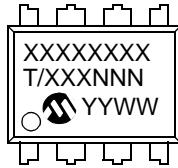
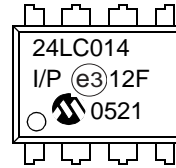**FIGURE 8-2:** **RANDOM READ**

FIGURE 8-3: **SEQUENTIAL READ**

9.0 PACKAGING INFORMATION

9.1 Package Marking Information

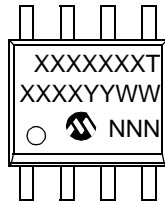8-Lead PDIP (300 mil)

```
XXXXXXXX
T/XXXNNN
  ⊙  Ⓜ YYWW
```
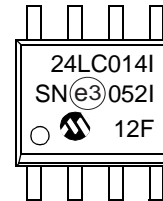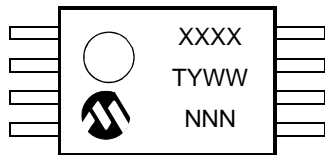
Example:

```
24LC014
I/P (e3)12F
  ⊙  Ⓜ 0521
```

8-Lead SOIC (150 mil)

```
XXXXXXXT
XXXXYYWW
  ○  Ⓜ NNN
```

Example:

```
24LC014I
SN(e3)052I
  ○  Ⓜ 12F
```

8-Lead TSSOP

```
  ◯      XXXX
         TYWW
  Ⓜ      NNN
```

Example:

```
  ◯      4L14
         I521
  Ⓜ      12F
```

8-Lead MSOP

```
XXXXT
YWWNNN

○  Ⓜ
```

Example:

```
4L14I
52112F

○  Ⓜ
```

8-Lead 2x3 DFN

```
  XXX
  YWW
  NN
•
```

Example:

```
  2N4
  521
  12
•
```
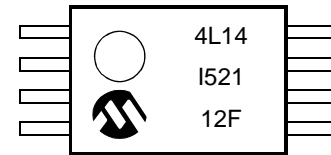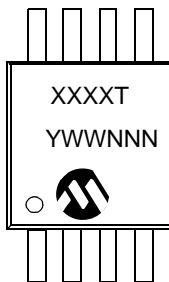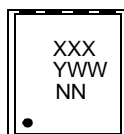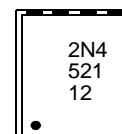
24AA014/24LC014

Part Number	1st Line Marking Codes		
	TSSOP	MSOP	DFN
24AA014	4A14	4A14T	2N1
24LC014	4L14	4L14T	2N4

Note: T = Temperature grade (I, E)

|		
Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3) , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

© 2005 Microchip Technology Inc.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)
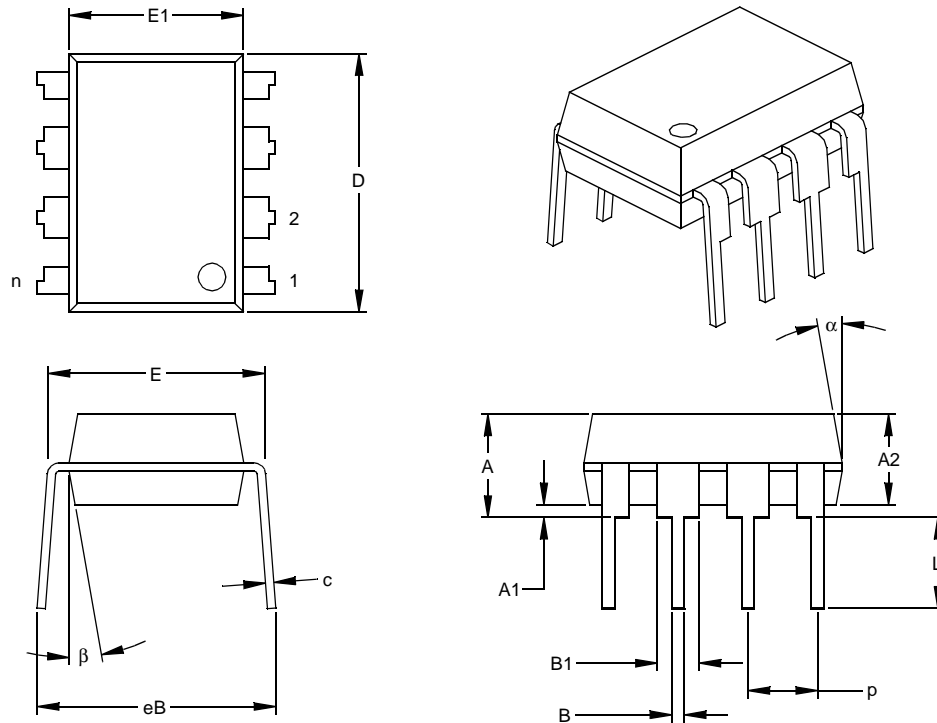
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
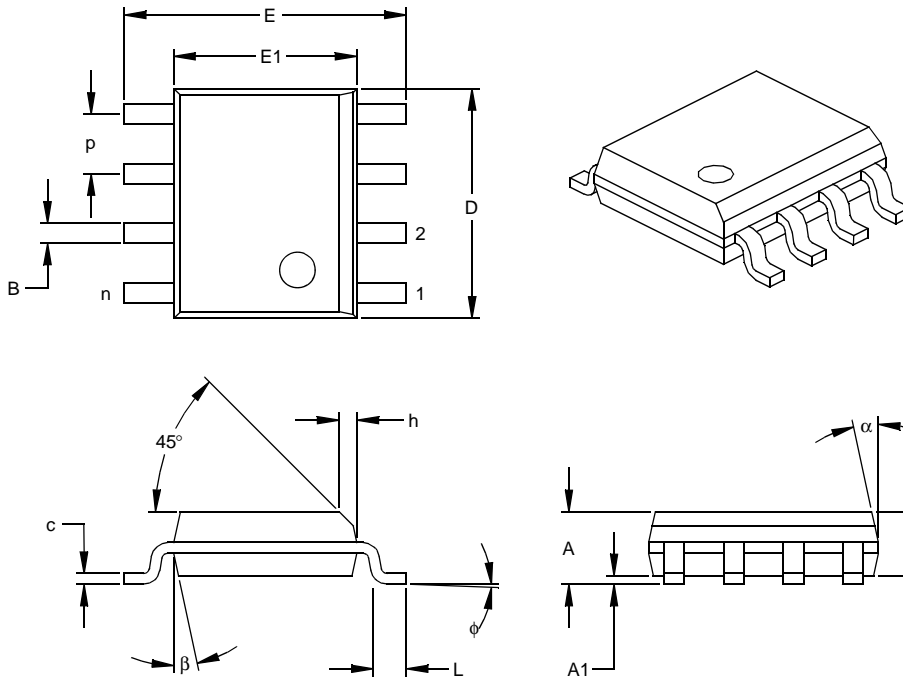§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

24AA014/24LC014

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

© 2005 Microchip Technology Inc.

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)
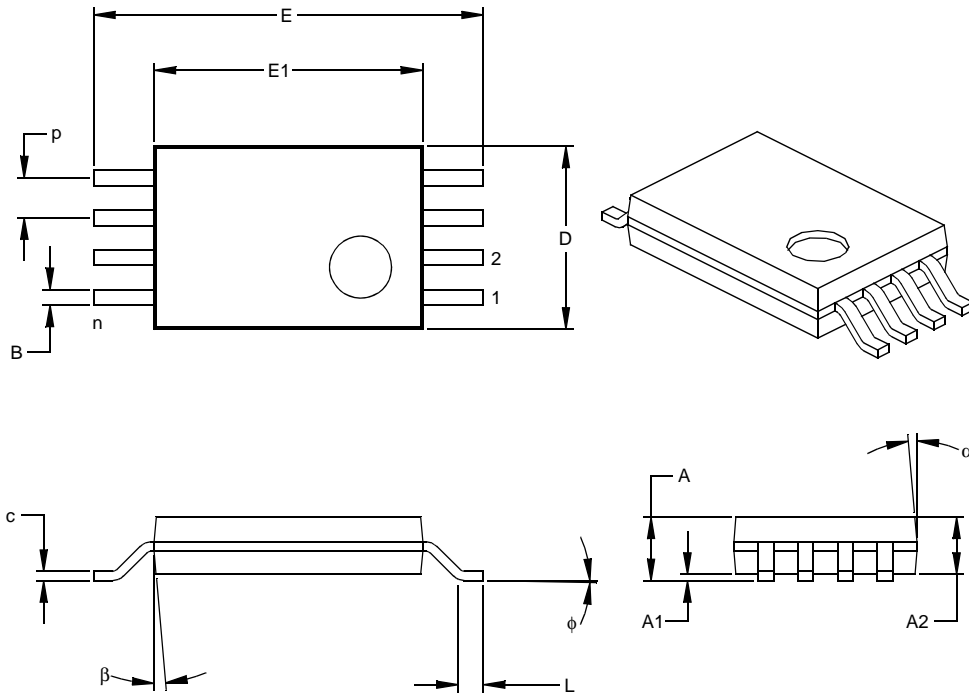
	Units	INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.
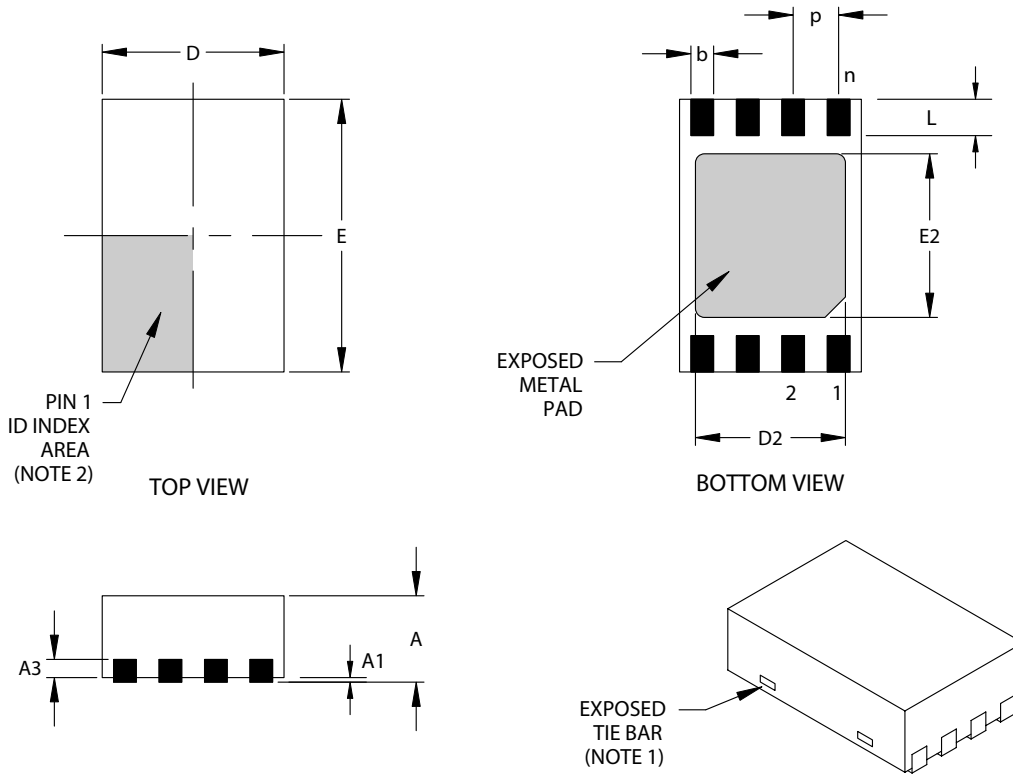JEDEC Equivalent: MO-153
Drawing No. C04-086

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)
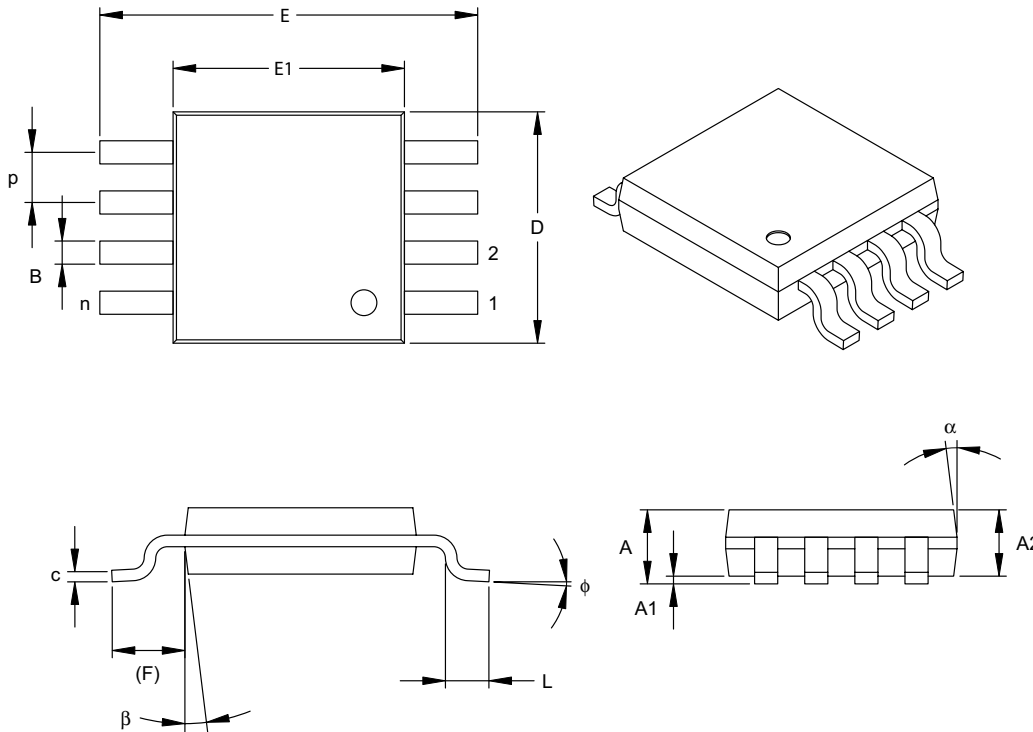
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

8-Lead Plastic Dual Flat No Lead Package (MC) 2x3x0.9 mm Body (DFN) – Saw Singulated

TOP VIEW

PIN 1
ID INDEX
AREA
(NOTE 2)

BOTTOM VIEW

EXPOSED
METAL
PAD

EXPOSED
TIE BAR
(NOTE 1)

Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.020 BSC			0.50 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008 REF.			0.20 REF.	
Overall Length	D		.079 BSC			2.00 BSC	
Exposed Pad Length (Note 3)	D2	.055	--	.064	1.39	--	1.62
Overall Width	E		.118 BSC			3.00 BSC	
Exposed Pad Width (Note 3)	E2	.047	--	.071	1.20	--	1.80
Contact Width	b	.008	.010	.012	0.20	0.25	0.30
Contact Length	L	.012	.016	.020	0.30	0.40	0.50

*Controlling Parameter

Notes:
1. Package may have one or more exposed tie bars at ends.
2. Pin 1 visual index feature may vary, but must be located within the hatched area.
3. Exposed pad dimensions vary with paddle size.
4. JEDEC equivalent: MO-229

Drawing No. C04-123

Revised 05/24/04

24AA014/24LC014

REVISION HISTORY

Revision B

Corrections to Section 1.0, Electrical Characteristics.

Revision C

Added DFN package.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

In addition, there is a Development Systems Information Line which lists the latest versions of Microchip's development systems software products. This line also provides information on how customers can receive currently available upgrade kits.

The Development Systems Information Line numbers are:

1-800-755-2345 – United States and most of Canada

1-480-792-7302 – Other International Locations

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager   Total Pages Sent _____

RE: Reader Response

From: Name _____

        Company _____

        Address _____

        City / State / ZIP / Country _____

        Telephone: (_____) _____ - _____   FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ____ Y ____ N

Device: 24AA014/24LC014   Literature Number: DS21809C

Questions:

1. What are the best features of this document?

    _____

    _____

2. How does this document meet your hardware and software development needs?

    _____

    _____

3. Do you find the organization of this document easy to follow? If not, why?

    _____

    _____

4. What additions to the document do you think would enhance the structure and subject?

    _____

    _____

5. What deletions from the document could be made without affecting the overall usefulness?

    _____

    _____

6. Is there any incorrect or misleading information (what and where)?

    _____

    _____

7. How would you improve this document?

    _____

    _____

© 2005 Microchip Technology Inc.

NOTES:

Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

• Microchip is willing to work with the customer who is concerned about the integrity of their code.

• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AmpLab, FilterLab, Migratable Memory, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rfLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel, Total Endurance and WiperLock are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2005, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

♻ Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═══ ISO/TS 16949:2002 ═══

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose
Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Qingdao
Tel: 86-532-502-7355
Fax: 86-532-502-7205

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-2229-0061
Fax: 91-80-2229-0062

India - New Delhi
Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

Japan - Kanagawa
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Taiwan - Hsinchu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

EUROPE

Austria - Weis
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Ballerup
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Massy
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Ismaning
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

England - Berkshire
Tel: 44-118-921-5869
Fax: 44-118-921-5820

03/01/05

© 2005 Microchip Technology Inc.