# DATA SHEET

## 74AVC16334A

16-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

Product specification
Supersedes data of 2000 May 02

2000 Aug 03

Philips Semiconductors

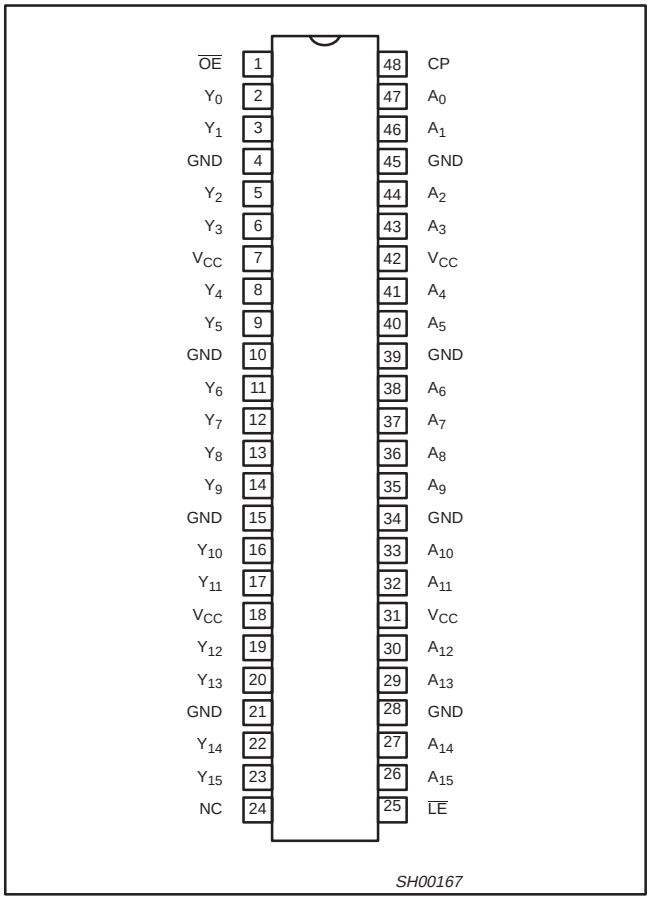
# 16-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

# 74AVC16334A

## FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A/5/7.
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- DCO (Dynamic Controlled Output) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple $V_{CC}$ and GND pins for minimum noise and ground bounce
- Power off disables 74AVC16334A outputs, permitting Live Insertion
- Integrated input diodes to minimize input overshoot and undershoot
- Full PC133 solution provided when used with PCK2509S or PCK2510S and CBT16292

## PIN CONFIGURATION




## DESCRIPTION

The 74AVC16334A is a 16-bit universal bus driver. Data flow is controlled by output enable ($\overline{OE}$), latch enable ($\overline{LE}$) and clock inputs (CP).

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient. See the graphs on page 8 for typical curves.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.0$ ns; $C_L$ = 30 pF.

| SYMBOL | PARAMETER | CONDITIONS | | TYPICAL | UNIT |
|---|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay An to Yn | $V_{CC}$ = 1.8 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ = 3.3 V | | 2.5<br>1.7<br>1.5 | ns |
| $t_{PHL}/t_{PLH}$ | Propagation delay $\overline{LE}$ to Yn;<br>CP to Yn | $V_{CC}$ = 1.8 V<br>$V_{CC}$ = 2.5 V<br>$V_{CC}$ = 3.3 V | | 2.7<br>2.0<br>1.6 | ns |
| $C_I$ | Input capacitance | | | 3.8 | pF |
| $C_{PD}$ | Power dissipation capacitance per buffer | $V_I$ = GND to $V_{CC}$[1] | Outputs enabled | 25 | pF |
| | | | Output disabled | 6 | |

**NOTE:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i$ = input frequency in MHz; $C_L$ = output load capacitance in pF; $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

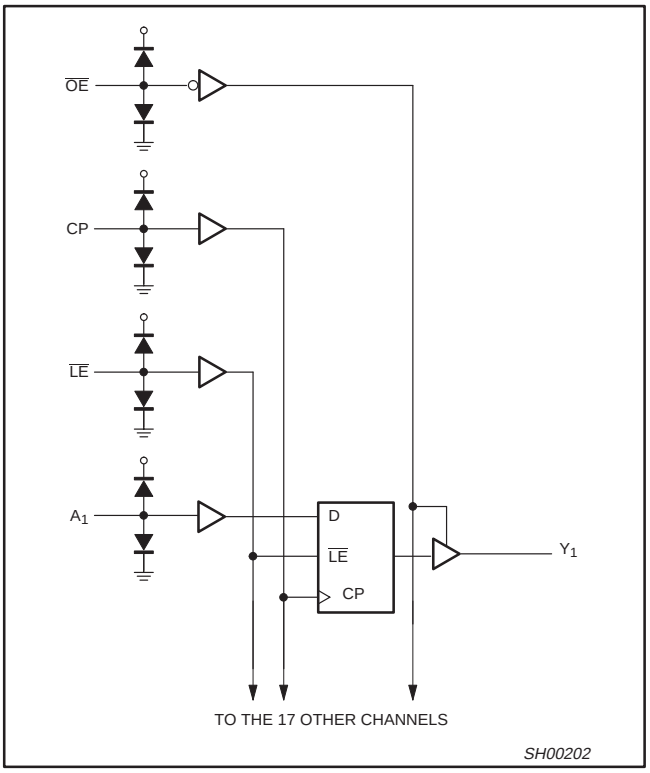
## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DRAWING NUMBER |
|---|---|---|---|---|
| 48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II | –40°C to +85°C | AVC16334A DGG | | SOT362-1 |

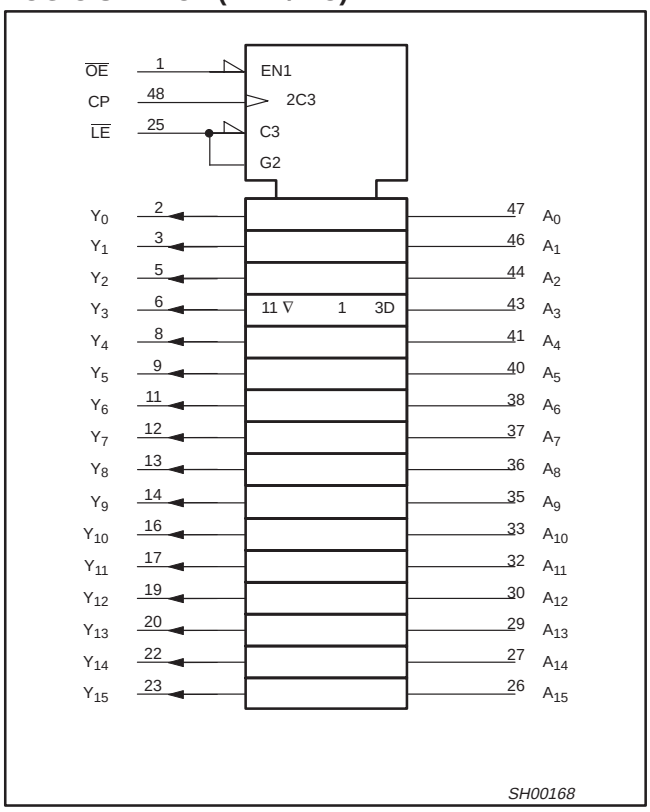
## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 24 | NC | No connection |
| 2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23 | $Y_0$ to $Y_{15}$ | Data outputs |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | Ground (0 V) |
| 7, 18, 31, 42 | $V_{CC}$ | Positive supply voltage |
| 1 | $\overline{OE}$ | Output enable input (active LOW) |
| 25 | $\overline{LE}$ | Latch enable input (active LOW) |
| 48 | CLK | Clock input |
| 47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26 | $A_0$ to $A_{15}$ | Data inputs |

## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)

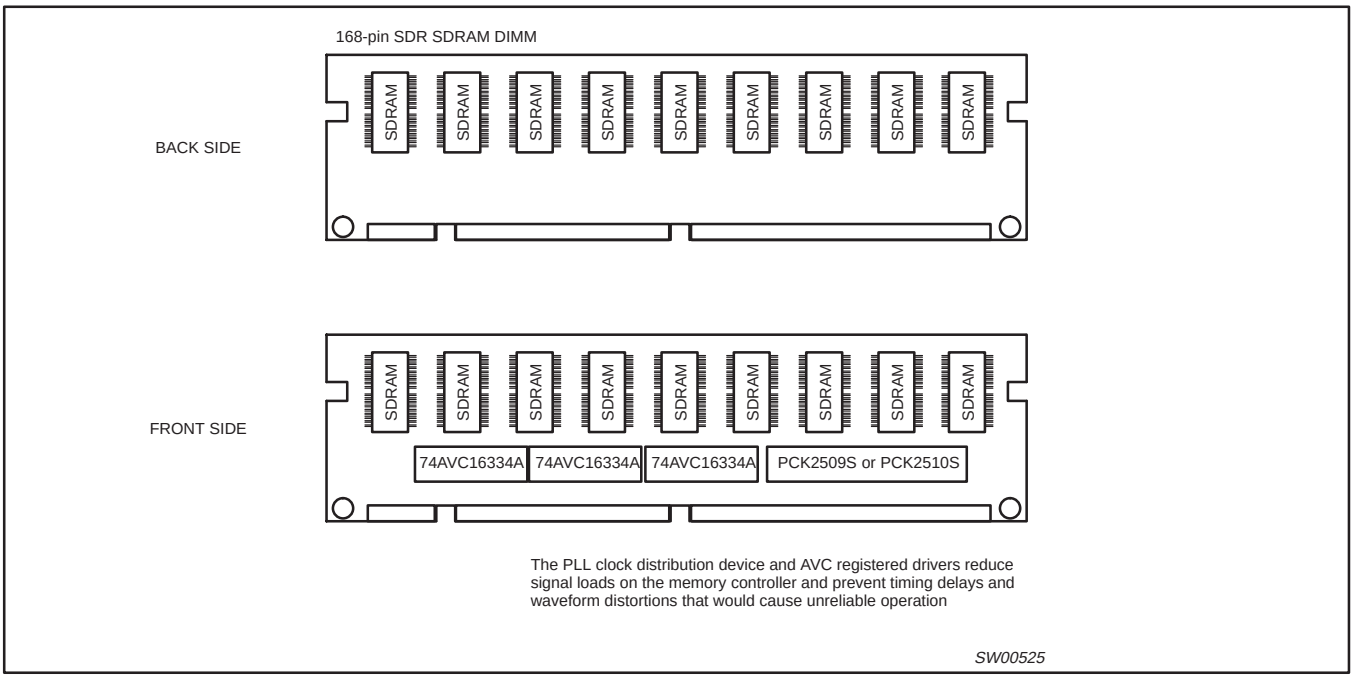



## FUNCTION TABLE

| INPUTS | | | | OUTPUTS |
|---|---|---|---|---|
| $\overline{OE}$ | $\overline{LE}$ | CLK | A | |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | L or H | X | $Y_0$[1] |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH level transition

**NOTE:**
1. Output level before the indicated steady-state input conditions were established.




## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage (according to JEDEC Low Voltage Standards) | | 1.65<br>2.3<br>3.0 | 1.95<br>2.7<br>3.6 | V |
| $V_{CC}$ | DC supply voltage (for low voltage applications) | | 1.2 | 3.6 | V |
| $V_I$ | DC Input voltage range | | 0 | 3.6 | V |
| $V_O$ | DC output voltage range; output 3-State | | 0 | 3.6 | V |
| | DC output voltage range; output HIGH or LOW state | | 0 | $V_{CC}$ | |
| $T_{amb}$ | Operating free-air temperature range | | –40 | +85 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 1.65 to 2.3 V<br>$V_{CC}$ = 2.3 to 3.0 V<br>$V_{CC}$ = 3.0 to 3.6 V | 0<br>0<br>0 | 30<br>20<br>10 | ns/V |

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +4.6 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –50 | mA |
| $V_I$ | DC input voltage | For data inputs[1] | –0.5 to 4.6 | V |
| $I_{OK}$ | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ±50 | mA |
| $V_O$ | DC output voltage; output 3-State | Note 1 | –0.5 to 4.6 | V |
| $V_O$ | DC output voltage; output HIGH or LOW state | Note 1 | –0.5 to $V_{CC}$ +0.5 | V |
| $I_O$ | DC output source or sink current | $V_O$ = 0 to $V_{CC}$ | ±50 | mA |
| $I_{GND}$, $I_{CC}$ | DC $V_{CC}$ or GND current | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package –plastic thin-medium-shrink (TSSOP) | For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K | 600 | mW |

**NOTE:**
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{CC}$ = 1.2 V | $V_{CC}$ | – | – | V |
| | | $V_{CC}$ = 1.65 to 1.95 V | 0.65 $V_{CC}$ | 0.9 | – | |
| | | $V_{CC}$ = 2.3 to 2.7 V | 1.7 | 1.2 | – | |
| | | $V_{CC}$ = 3.0 to 3.6 V | 2.0 | 1.5 | – | |
| $V_{IL}$ | LOW level Input voltage | $V_{CC}$ = 1.2 V | – | – | GND | V |
| | | $V_{CC}$ = 1.65 to 1.95 V | – | 0.9 | 0.35 $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 to 2.7 V | – | 1.2 | 0.7 | |
| | | $V_{CC}$ = 3.0 to 3.6 V | – | 1.5 | 0.8 | |
| $V_{OH}$ | HIGH level output voltage | $V_{CC}$ = 1.65 to 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –100 µA | $V_{CC}$ – 0.20 | $V_{CC}$ | – | V |
| | | $V_{CC}$ = 1.65 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –4 mA | $V_{CC}$ – 0.45 | $V_{CC}$ – 0.10 | – | |
| | | $V_{CC}$ = 2.3 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –8 mA | $V_{CC}$ – 0.55 | $V_{CC}$ – 0.28 | – | |
| | | $V_{CC}$ = 3.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –12 mA | $V_{CC}$ – 0.70 | $V_{CC}$ – 0.32 | – | |
| $V_{OL}$ | LOW level output voltage | $V_{CC}$ = 1.65 to 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100 µA | – | GND | 0.20 | V |
| | | $V_{CC}$ = 1.65 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 4 mA | – | 0.10 | 0.45 | |
| | | $V_{CC}$ = 2.3 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 8 mA | – | 0.26 | 0.55 | |
| | | $V_{CC}$ = 3.0 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 12 mA | – | 0.36 | 0.70 | |
| $I_I$ | Input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | – | 0.1 | 2.5 | µA |
| $I_{OFF}$ | 3-State output OFF-state current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 3.6 V | – | 0.1 | ±10 | µA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{CC}$ = 1.65 to 2.7 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND | – | 0.1 | 5 | µA |
| | | $V_{CC}$ = 3.0 to 3.6 V; $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND | – | 0.1 | 10 | |
| $I_{CC}$ | Quiescent supply current | $V_{CC}$ = 1.65 to 2.7 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | – | 0.1 | 20 | µA |
| | | $V_{CC}$ = 3.0 to 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | – | 0.2 | 40 | |

**NOTE:**

1. All typical values are at $T_{amb}$ = 25°C.

## AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L$ = 30 pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 ± 0.3 V | | | $V_{CC}$ = 2.5 ± 0.2 V | | | $V_{CC}$ = 1.8 ± 0.15 V | | | $V_{CC}$ = 1.5 ± 0.1 V | | $V_{CC}$ = 1.2 V | |
| | | | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | MIN | TYP[1] | MAX | MIN | MAX | TYP | |
| $t_{PHL}/t_{PLH}$ | Propagation delay An to Yn | 1 | 0.7 | 1.5 | 2.6 | 0.8 | 1.7 | 3.0 | 1.0 | 2.5 | 4.4 | 1.7 | 5.3 | 5.0 | ns |
| | Propagation delay $\overline{LE}$ to Yn | 2 | 0.7 | 1.6 | 3.2 | 1.0 | 2.0 | 3.3 | 1.2 | 2.7 | 4.8 | 1.7 | 6.0 | 5.3 | |
| | Propagation delay CP to Yn | 3 | 0.7 | 1.6 | 2.8 | 0.8 | 1.7 | 3.0 | 1.0 | 2.3 | 3.9 | 1.4 | 4.6 | 4.1 | |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $\overline{OE}$ to Yn | 6 | 0.7 | 1.7 | 3.4 | 1.0 | 2.2 | 3.8 | 1.5 | 3.1 | 5.3 | 2.0 | 6.7 | 6.0 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time $\overline{OE}$ to Yn | 6 | 1.0 | 2.1 | 3.7 | 0.9 | 2.0 | 3.9 | 1.5 | 3.7 | 6.5 | 1.7 | 7.1 | 6.1 | ns |
| $t_W$ | CP pulse width HIGH or LOW | 3 | 1.0 | – | – | 1.2 | – | – | 2.0 | – | – | – | – | – | ns |
| | $\overline{LE}$ pulse width LOW | 2 | 1.0 | – | – | 1.2 | – | – | 2.0 | – | – | – | – | – | |
| $t_{SU}$ | Set-up time An to CP | 5 | 0.2 | –0.1 | – | 0.1 | –0.1 | – | 0.1 | –0.1 | – | 0.1 | – | 0.0 | ns |
| | Set-up time An to $\overline{LE}$ | 4 | 0.4 | 0.1 | – | 0.5 | 0.1 | – | 0.8 | 0.3 | – | 1.2 | – | 1.0 | |
| $t_h$ | Hold time An to CP | 5 | 0.6 | 0.2 | – | 0.6 | 0.2 | – | 0.6 | 0.2 | – | 0.6 | – | 0.1 | ns |
| | Hold time An to $\overline{LE}$ | 4 | 0.4 | 0.1 | – | 0.4 | 0.1 | – | 0.3 | 0.1 | – | 0.3 | – | –0.4 | |
| $f_{max}$ | Maximum clock pulse frequency | 3 | 500 | – | – | 400 | – | – | 250 | – | – | – | – | – | MHz |

**NOTE:**

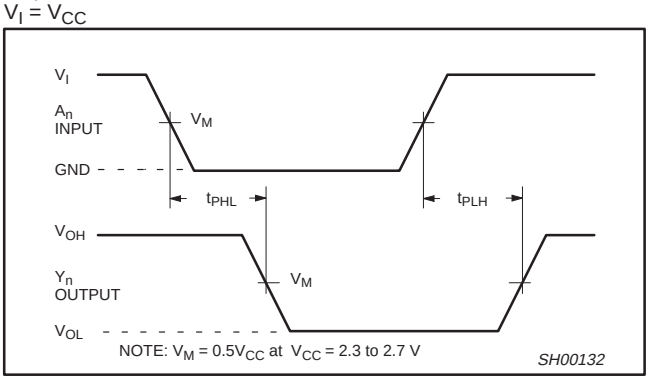
1. All typical values are measured at $T_{amb}$ = 25°C and at $V_{CC}$ = 1.8 V, 2.5 V, 3.3 V.

## AC WAVEFORMS FOR $V_{CC}$ = 3.0 V TO 3.6 V RANGE

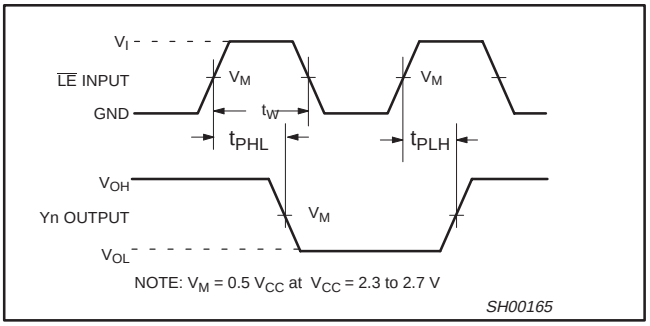
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.300\ V$
$V_Y = V_{OH} - 0.300\ V$
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

## AC WAVEFORMS FOR $V_{CC}$ = 2.3 V TO 2.7 V AND $V_{CC}$ < 2.3 V RANGE

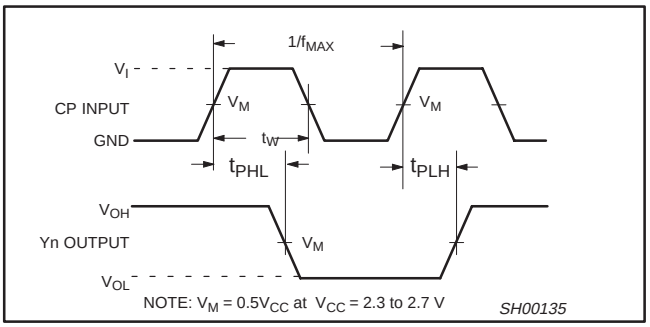
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15\ V$
$V_Y = V_{OH} - 0.15\ V$
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$



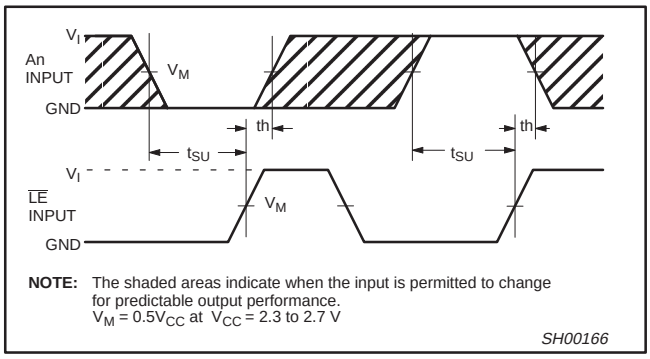

**Waveform 1. Input (An) to output (Yn) propagation delay**



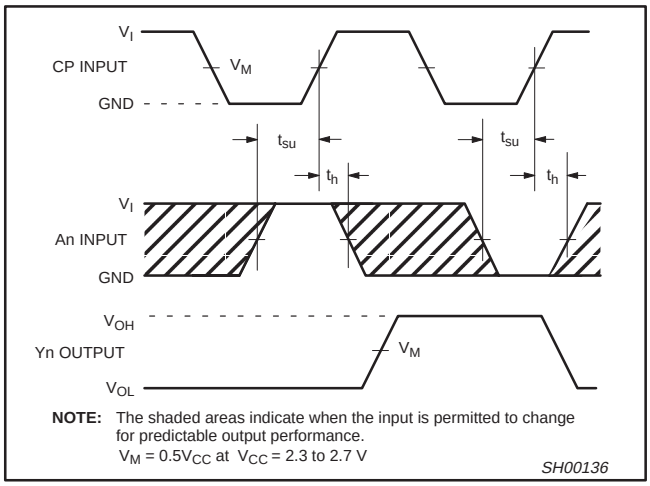

**Waveform 2. Latch enable input ($\overline{LE}$) pulse width, the latch enable input to output (Yn) propagation delays.**



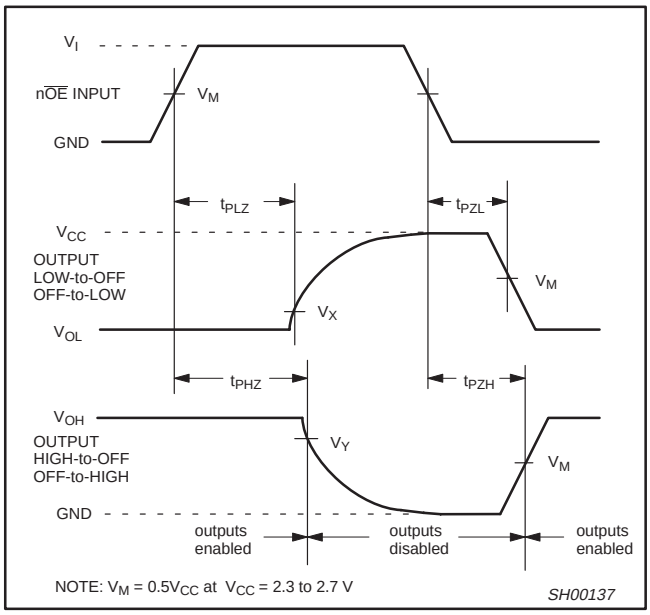

**Waveform 3. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.**




**Waveform 4. Data set-up and hold times for the An input to the $\overline{LE}$ input**

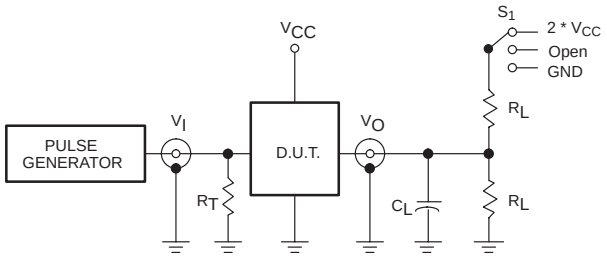



**Waveform 5. Data set-up and hold times for the An input to the clock CP input**




**Waveform 6. 3-State enable and disable times**

## TEST CIRCUIT




**Test Circuit for switching times**

**DEFINITIONS**

$R_L$ = Load resistor

$C_L$ = Load capacitance includes jig and probe capacitance

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

**SWITCH POSITION**

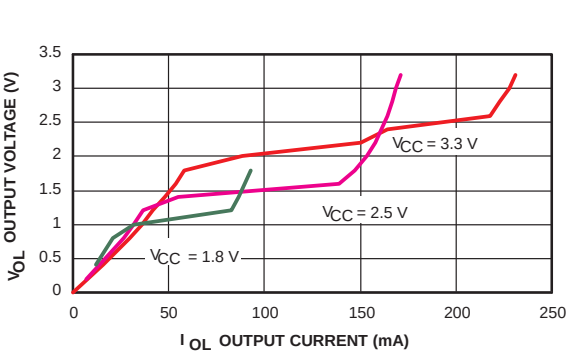
| TEST | $S_1$ |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 * $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $V_I$ | $R_L$ |
|---|---|---|
| < 2.3 V | $V_{CC}$ | 1000 Ω |
| 2.3–2.7 V | $V_{CC}$ | 500 Ω |
| 3.0 V | $V_{CC}$ | 500 Ω |

SV01018

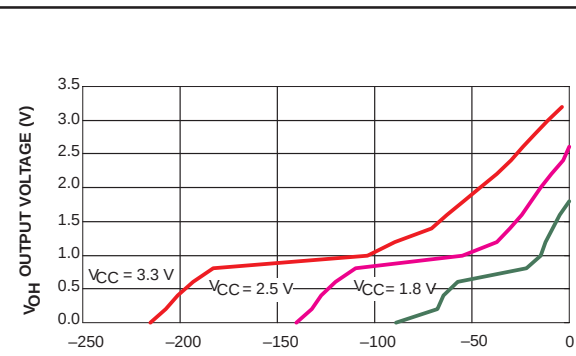
**Waveform 7. Load circuitry for switching times**

## GRAPHS




SH00204

**Figure 1. Output voltage ($V_{OL}$) vs. output current ($I_{OL}$)**

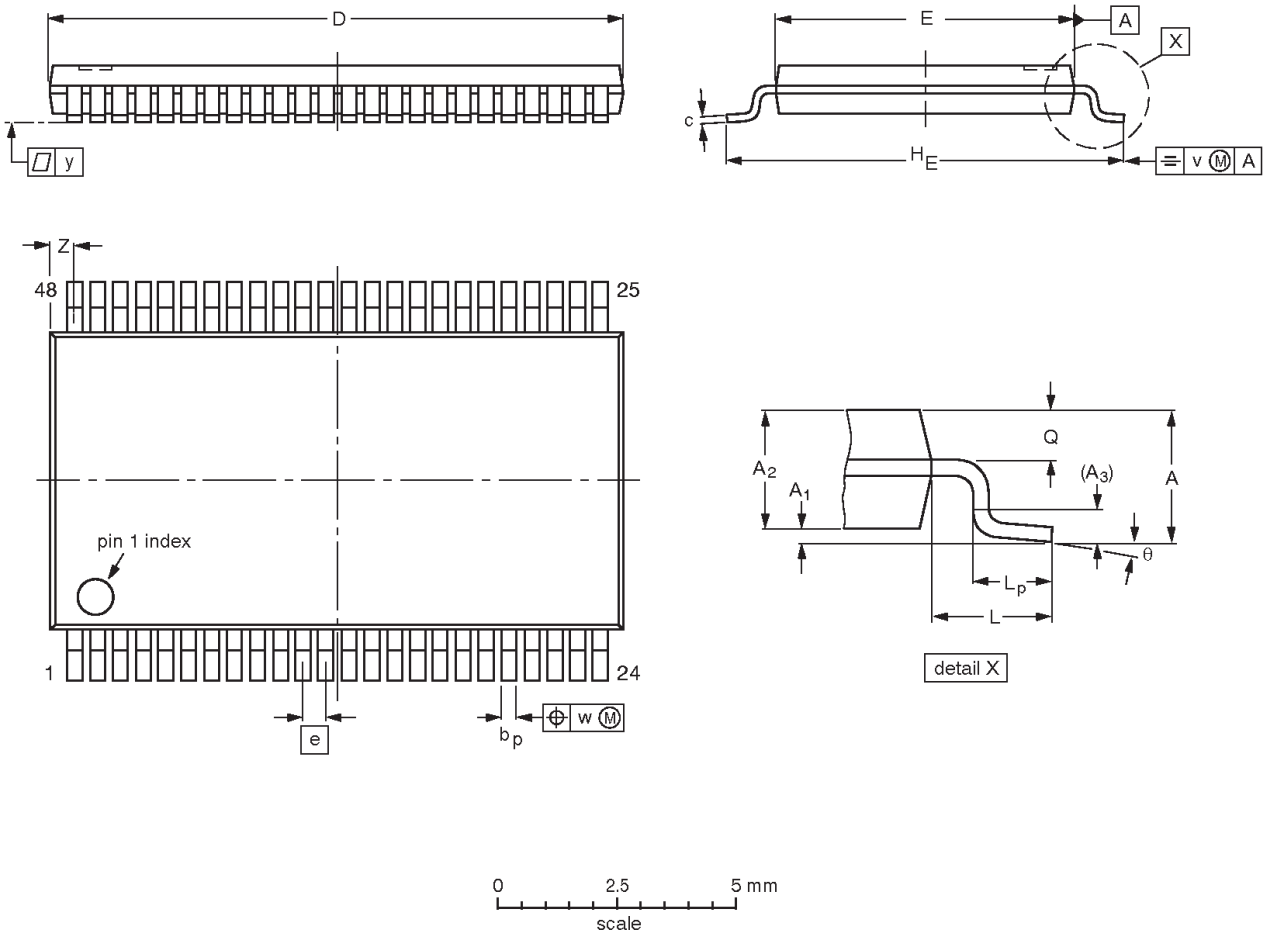



SH00205

**Figure 2. Output voltage ($V_{OH}$) vs. output current ($I_{OH}$)**

A Dynamic Controlled Output (DCO) circuit is designed in. During the transition, it initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figures 1 and 2 show $V_{OL}$ vs. $I_{OL}$ and $V_{OH}$ vs. $I_{OH}$ curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DCO circuit provides a maximum dynamic drive that is equivalent to a high drive standard output device.

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 12.6<br>12.4 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT362-1 | | MO-153ED | | | | | ~~93-02-03~~<br>95-02-10 |

# 16-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State) 74AVC16334A

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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