DATA SHEET

CBT6832D

16-bit controlled enable rate
1-of-2 multiplexer/demultiplexer
with precharged outputs and charge pump
undershoot protection for live insertion

Product specification
Supersedes data of 2000 May 18

2000 Sep 01

Philips
Semiconductors

16-bit controlled enable rate 1-of-2 multiplexer/demultiplexer with precharged outputs and charge pump undershoot protection for live insertion

CBT6832D

FEATURES

- 5 Ω typical r_{on}
- Pull-up on B port
- Undershoot protection on A port only: –2.0 V
- Near zero propagation delay
- Controlled enable rate
- V_{CC} operating range: +4.5 V to +5.5 V
- > 100 MHz bandwidth (or clock rate) at 20 pF load capacitance
- 56-pin TSSOP package
- Bias voltage pre-charges the B output when the channel is disabled
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

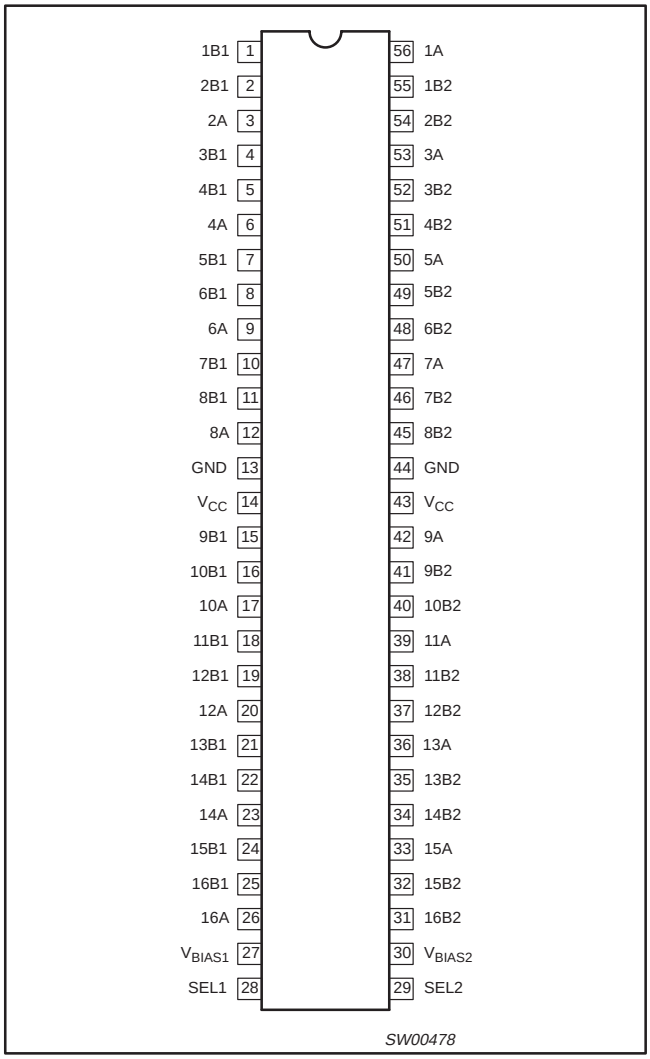
APPLICATION

- Provides PCI-X hot-plugging

DESCRIPTION

The CBT6832D is a 16-bit controlled enable rate 1-of-2 multiplexer/demultiplexer with precharged outputs and charge pump undershoot protection for live insertion. Advantages of the CBT6832 include a propagation delay of 250 ps, resulting from 5 Ω channel resistance, and low I/O capacitance. A port demultiplexes to either 1B and 2B, or to both. The switch is bi-directional.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	0.25	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4.5	pF
$C_{OFF\ B}$	B capacitance, switch off	Outputs disabled; V_O = 0 V	8	pF
$C_{OFF\ A}$	A capacitance, switch off	Outputs disabled; V_O = 0 V	13	pF
$C_{ON\ 1}$	One channel enabled capacitance	One B enabled; V_O = 0 V	21	pF
$C_{ON\ 2}$	Both channels enabled capacitance	Both B channels enabled; V_O = 0 V	34	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic TSSOP Type II	0°C to +70°C	CBT6832D DGG	SOT364-1

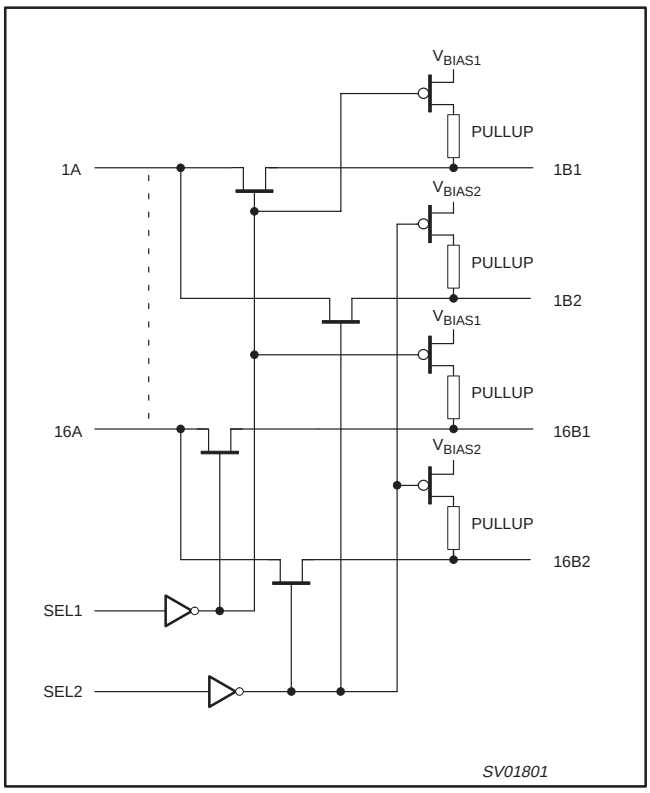
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3, 6, 9, 12, 17, 20, 23, 26, 33, 36, 39, 42, 47, 50, 53, 56	1A1–16A1	Inputs
1, 2, 4, 5, 7, 8, 10, 11, 15, 16, 18, 19, 21, 22, 24, 25	1B1–16B1	Outputs
31, 32, 34, 35, 37, 38, 40, 41, 45, 46, 48, 49, 51, 52, 54, 55	1B2–16B2	Outputs
27, 30	V_{BIAS1}, V_{BIAS2}	Precharge bias voltage inputs
28, 29	SEL1, SEL2	Select-control inputs
13, 44	GND	Ground (0 V)
14, 43	V_{CC}	Positive supply voltage

FUNCTION TABLE

SEL1	SEL2	FUNCTION
L	H	nA to nB1
H	L	nA to nB2
L	L	nA to nB1 and nB2
H	H	nB1, nB2 = V_{BIAS}

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	output in Low state	120	mA
T_{stg}	Storage temperature range		–65 to +150	°C
Θ_{JA}	Power dissipation		95	°C/W

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
T_{amb}	Operating free-air temperature range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS

Over operating temperature range T_{amb} = 0°C to +70°C; V_{CC} = 5 V ±10%; V_{BIAS} = 1.3 V to V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IH}	Input HIGH voltage	Guaranteed logic HIGH level	2.0			V
V_{IL}	Input LOW voltage	Guaranteed logic LOW level	–0.5		0.8	V
I_{IH}	Input HIGH current	V_{CC} = 5.5 V, V_{IN} = V_{CC}			±5	µA
I_{IL}	Input LOW current	V_{CC} = 5.5 V, V_{IN} = GND			±5	µA
I_{OZH}	High impedance output current	A = 0 V or V_{CC} MAX, V_{BIAS1} = V_{BIAS2} = V_{CC} MAX			±1	µA
I_{OZL}	Low impedance output current	B = 0 V or V_{CC} MAX, V_{BIAS1} = V_{BIAS2} = V_{CC} MAX	–0.2		–2	mA
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = –18 mA		–0.7	–1.8	V
r_{on}	Switch on resistance[2]	V_{CC} = 4.5 V; V_I = 0 V; I_I = 48 mA		5	8	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = –15 mA		10	15	Ω
Capacitance[3] (T_{amb} = +25°C; f = 1 MHz)						
C_{IN}	Input capacitance	V_I = 0 V		4.5		pF
$C_{OFF\ B}$	B capacitance, switch off	V_I = 0 V		8		pF
$C_{OFF\ A}$	A capacitance, switch off	V_I = 0 V		13		pF
$C_{ON\ 1}$	Capacitance, switch on (one B)	V_I = 0 V		21		pF
$C_{ON\ 2}$	Capacitance, both B channels enabled	V_I = 0 V		34		pF
Power supply						
I_{CC}	Quiescent supply current enabled	V_{CC} = 5.5 V; V_I = V_{CC} or GND			200	µA
ΔI_{CC}	Additional supply current per input pin[5]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND			2.5	mA

NOTES:

1. All typical values are at V_{CC} = 5 V, T_{amb} = +25°C ambient and maximum loading.
2. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.
3. These parameters are determined by device characterization, but is not production tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. Per TTL driven input (V_I = 3.4 V, control inputs only); A and B pins do not contribute to I_{CC}.
6. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. this parameter is not tested, but is guaranteed by design.

AC CHARACTERISTICS

V_{CC} = 5.0 V ±0.5 V; GND = 0 V; C_L = 50 pF, R_L = 500 Ω

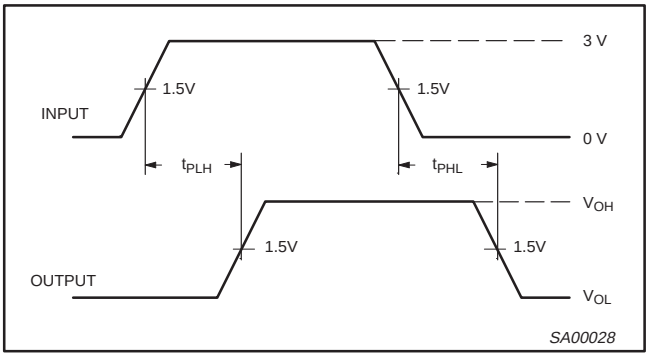
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay[1] A to B			0.25		ns
t_{PZH} t_{PZL}	Bus enable time SEL to A, B		10 5		30 25	ns
t_{PHZ} t_{PLZ}	Bus disable time SEL to A, B		0.5 0.5		6 7	ns

NOTE:

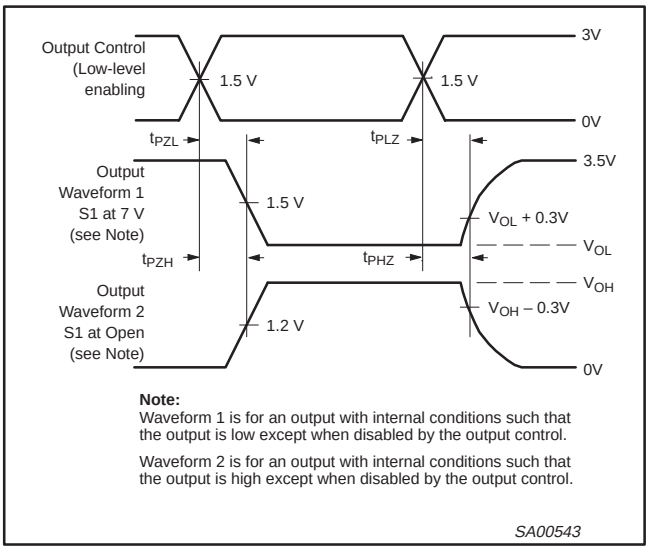
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V

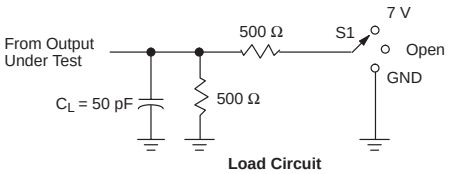


Waveform 1. Input (An) to Output (Bn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Load Circuit

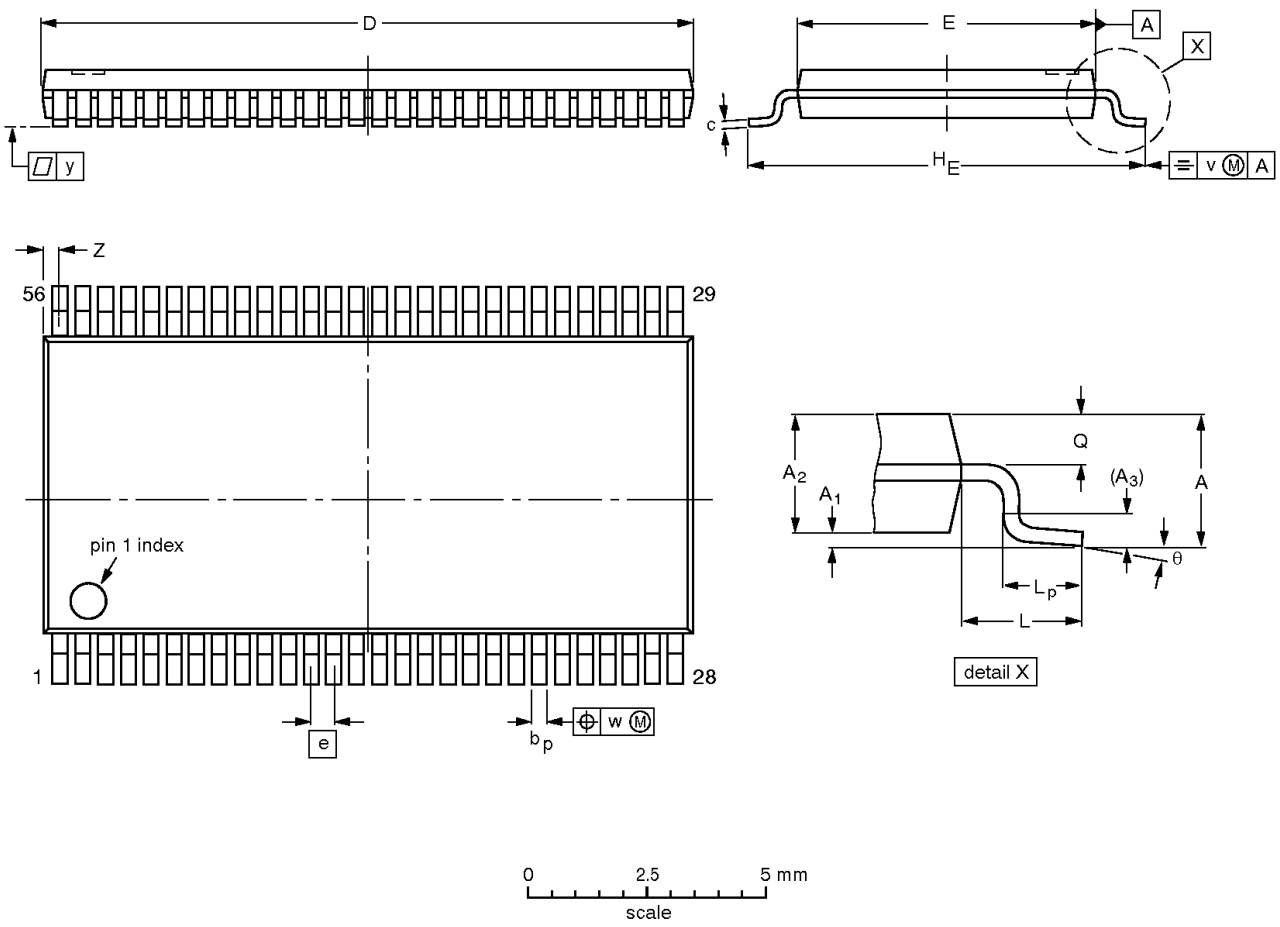
TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

NOTES

16-bit controlled enable rate 1-of-2 multiplexer/demultiplexer with precharged outputs and charge pump undershoot protection for live insertion

CBT6832D

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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