

October 2010

# FSLV16211 — 24-Bit Bus Switch

### **Features**

- $5\Omega$  Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low I<sub>CC</sub>
- Zero Bounce in Flow-Through Mode
- Packaged in Thin-Shrink Small Outline Package (TSSOP)

### **Description**

The FSLV16211 is a 24-bit, high-speed, low-voltage bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

This design can be used as a 12- or 24-bit bus switch. When /OE1 is LOW, port 1A is connected to Port 1B. When /OE2 is LOW, port 2A is connected to Port 2B.

## **Ordering Information**

Part Number	Operating Temperature Range	Package	Packing Method
FSLV16211MTDX	-40°C to 85°C	56-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC M0-153, 6.1mm Wide	Tape and Reel

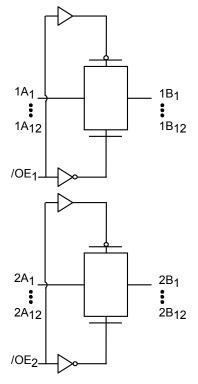


Figure 1. Logic Diagram

# **Connection Diagram**

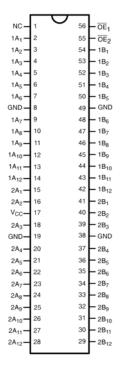


Figure 2. Pin Assignments for TSSOP (Top Through View)

# **Pin Description**

Pin Name	Description
OE <sub>1</sub> , OE <sub>2</sub> Bus Switch Enables	
1A, 2A	Bus A
1B, 2B	Bus B
NC	No Connect

### **Truth Table**

Inp	uts	Inputs/0	Outputs
OE <sub>1</sub>	OE <sub>2</sub>	1A,1B	2A, 2B
Low	Low	1A=1B	2A=2B
Low	High	1A=1B	Z
High	Low	Z	2A=2B
High	High	Z	Z

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	-0.5	4.6	V
Vs	DC Switch Voltage <sup>(1)</sup>	-0.5	4.6	V
V <sub>IN</sub>	DC Input Voltage	-0.5	4.6	V
I <sub>IK</sub>	DC Input Diode Current		-50	mA
I <sub>OUT</sub>	DC Output Sink Current		128	mA
I <sub>CC</sub> /I <sub>GNG</sub>	DC V <sub>CC</sub> /GND Current		±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C

### Note:

## **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.<sup>(2)</sup>

Symbol	Parameter		Min.	Max.	Unit
V <sub>CC</sub>	Power Supply Operating Voltage		2.3	3.6	V
V <sub>IN</sub>	Input Voltage		0	3.6	V
$V_{OUT}$	Output Voltage		0	3.6	V
+ +	Innut Disc and Fall Time	Switch Control Input	0	4.0	ns/V
t <sub>r</sub> , t <sub>f</sub> Input Rise and Fall Time	Switch I/O	0	DC	ns/V	
T <sub>A</sub>	Free Air Operating Temperature		-40	85	°C

#### Note:

2. Unused control inputs must be held HIGH or LOW. They may not float.

The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

### **DC Electrical Characteristics**

Not all conditions may appear on all switch types.

Symbol	Parameter	Conditions	V <sub>cc</sub>	T <sub>A</sub> = -40°C to +85°C			Unit
Symbol		Conditions	(V)	Min.	Тур.	Max.	Unit
V <sub>IK</sub>	Clamp Diode Voltage	I <sub>IN</sub> = -18mA	3.0			-1.2	V
V <sub>IH</sub>	HIGH Level Control Input Voltage		2.3-2.7 2.7-3.6	1.7 2.0			V
V <sub>IL</sub>	LOW Level Control Input Voltage		2.3-2.7 2.7-3.6			0.7	V
		Force V <sub>I</sub> = 3.6V, I <sub>OUT</sub> = 0.0A	2.3			10	_
IL	Input Leakage Current	Force V <sub>I</sub> = 3.6V	0.0			10	μΑ
		$0 \leq \ V_{IN} \leq \ 3.6 V$	3.6			1	
I <sub>CC</sub>	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0A$	3.6			10	μΑ
Δlcc	Increase in I <sub>CC</sub> per Input	One Input at 3V Other Inputs at V <sub>CC</sub> or GND	3.6			300	μΑ
l <sub>OZ</sub>	Off-State Leakage	0.0 ≤ A, B ≤ 3.6V	3.6	-1		1	μΑ
		I <sub>IN</sub> = 64mA, V <sub>I</sub> = 0.0V	3.0		5	7	
		$I_{IN} = 30 \text{mA}, V_I = 0.0 \text{V}$	3.0		5	7	
		$I_{IN} = 15mA, V_I = 2.4V$	3.0		10	15	1
Ron	Switch On Resistance	$I_{IN} = 15mA, V_I = 3.0V$	2.3			20	Ω
NON	Owiton On Nesistance	$I_{IN} = 64mA, V_I = 0.0V$	2.3		5	8	2.2
		$I_{IN} = 30 \text{mA}, V_I = 0.0 \text{V}$	2.3		5	8	
		$I_{IN} = 15 \text{mA}, V_I = 1.7 \text{V}$	2.3		10	15	
		$I_{IN} = 15mA, V_I = 2.0V$	2.3			20	

### **AC Electrical Characteristics**

Symbol		T <sub>A</sub> =-40°C to +85°C		T <sub>A</sub> =40°C	- Unit	
	Dovementor	C <sub>L</sub> =30pF, R <sub>L</sub> =500Ω		C <sub>L</sub> =50pF, R <sub>L</sub> =500Ω		
	Parameter	$V_{CC} = 2.5V \pm 0.20V$		$V_{CC} = 3.3V \pm 0.30V$		
		Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay <sup>(3)</sup>		0.15		0.25	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Enable Time	0.5	4.7	1.0	7.0	ns
$t_{PZH},t_{PZL}$	Disable Time	0.5	5.1	1.0	5.5	ns

### Note:

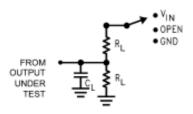
3. This parameter is guaranteed by design, but is not production tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the load capacitance when driven by an ideal voltage source (zero output impedance).

# Capacitance

T<sub>A</sub> = +25°C, f = 1MHz, unless otherwise noted. Capacitance is characterized, but not production tested.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> – 3.3V		4.5		pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> , /OE= 3.3V		18		pF

# **AC Loading Waveforms**



 TEST
 SWITCH

 t<sub>PD</sub>
 Open

 t<sub>PLZ</sub>/t<sub>PZL</sub>
 V<sub>IN</sub>

 t<sub>PHZ</sub>/t<sub>PZH</sub>
 GND

Note:  $C_L$  includes load and stray capacitance Note: Input PRR = 1.0 MHz,  $t_W$  = 500 ns

Figure 3. AC Test Circuit

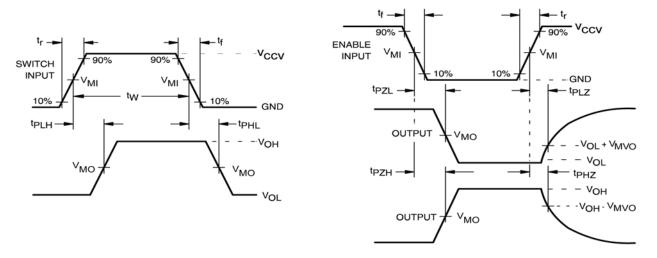


Figure 4. AC Waveforms

	V <sub>cc</sub>				
Symbol	3.3V ± 0.3V	2.5V ± 0.2V			
V <sub>MI</sub>	1.5V	V <sub>CC</sub> /2			
V <sub>MO</sub>	1.5V	V <sub>CC</sub> /2			
V <sub>MVO</sub>	0.3V	0.15V			
V <sub>IN</sub>	6.0V	2 x V <sub>CC</sub>			
V <sub>CCV</sub>	3.0V	Vcc			
t <sub>r</sub> /t <sub>f</sub>	2ns	2.5ns			

## **Physical Dimensions** 14.00±0.10 0.15 TYP В 8.10 4.05 28 0.2 C B A 23 28 ALL LEAD TIPS PIN #1 IDENT. 0.30 0.50 LAND PATTERN RECOMMENDATION REFERENCE TSSOP50P810X120-56N □ 0.1 C SEE DETAIL A 1.1 MAX ALL LEAD TIPS -C-0.09-0.20 0.10±0.05 0.17-0.27 0.50 ⊕ 0.10M A BS CS 12.00° TOP & BOTTOM NOTES: R0.16 GAGE PLANE A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EE, $_{\rm R0.31}$ REF NOTE 6, DATE 10/97. 0.25 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. 0.60±0.10 1.00 E. DRAWING FILE NAME: MTD56REV3 MTD56REV3 DETAIL A

Figure 5. 56-Lead Thin-Shrink Small Outline Package (TSSOP), JEDEC MO153, 6.1mm Wide

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Rev. 150

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