

## CBTD16212 24-bit level shifting bus exchange switch with 12-bit output enables

Product data
File under Integrated Ciruits ICL03

PHILIPS

## 24-bit level shifting bus exchange switch with 12-bit output enables

## FEATURES

- $5 \Omega$ switch connection between two ports
- TTL compatible control input levels
- Designed to be used in level shifting applications
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- ESD protection exceeds 1500 V HBM per JESD22-114A and 1000 V CDM per JESD22-C101


## DESCRIPTION

The CBTD16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

A diode to $\mathrm{V}_{\mathrm{CC}}$ is integrated into the circuit to allow for level shifting between 5 V inputs and 3.3 V outputs.

The CBTD16212 operates as 24 -bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0-S2) terminals.
The CBT16212 is characterized for operation from -40 to $+85^{\circ} \mathrm{C}$.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS <br> $T_{\text {amb }}=25{ }^{\circ} \mathbf{C} ; \mathbf{G N D}=\mathbf{0} \mathbf{V}$ | TYPICAL | UNIT |
| :---: | :--- | :--- | :---: | :---: |
| $\mathrm{t}_{\mathrm{pd}}$ | Propagation delay <br> An to n n | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} ; \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | 0.25 | ns |
| $\mathrm{C}_{\mathrm{IN}}$ | Input capacitance | $\mathrm{V}_{\mathrm{I}}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | 4.5 | pF |
| $\mathrm{C}_{\mathrm{OUT}}$ | Output capacitance | Outputs disabled; $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ or $\mathrm{V}_{\mathrm{CC}}$ | 11.5 | pF |
| $\mathrm{r}_{\mathrm{on}}$ | A1 to A 2 | $\mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=0 \mathrm{~V}$ | 5 | $\Omega$ |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DWG NUMBER |
| :--- | :---: | :---: | :---: |
| 56 -Pin Plastic SSOP | -40 to $+85^{\circ} \mathrm{C}$ | CBTD16212DL | SOT371-1 |
| $56-$ Pin Plastic TSSOP | -40 to $+85^{\circ} \mathrm{C}$ | CBTD16212DGG | SOT364-1 |

## NOTE

1. Standard packing quantities and other packaging data is available at www.philipslogic.com/support/packages.

## FUNCTION TABLE

| S2 | S1 | S0 | A1 | A2 | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L | L | L | Z | Z | Disconnect |
| L | L | H | B1 | Z | A1 = B1 |
| L | H | L | B2 | Z | A1 $=$ B2 |
| L | H | H | Z | B1 | A2 $=$ B1 |
| H | L | L | Z | B2 | A2 $=$ B2 |
| H | L | H | Z | Z | Disconnect |
| H | H | L | B1 | B2 | A1 $=$ B1, A2 $=$ B2 |
| H | H | H | B2 | B1 | A1 $=$ B2, A2 $=$ B1 |

$\mathrm{H}=$ High voltage level
L = Low voltage level
$Z=$ High impedance "off" state

## LOGIC SYMBOL



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## PIN CONFIGURATION



PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
| :---: | :---: | :--- |
| $1,56,55$ | S0, S1, S2 | Data select |
| $2,4,6,9,11,13,15$, <br> $18,21,23,25,27$ | 1A1-12A1 | A1 channel |
| $3,5,7,10,12,14,16$, <br> $20,22,24,26,28$ | 1A2-12A2 | A2 channel |
| $54,52,50,47,45,43$, <br> $41,39,36,34,32,30$ | 1B1, 12B1 | B1 channel |
| $53,51,48,46,44,42$, <br> $40,37,35,33,31,29$ | $1 \mathrm{~B} 2,12 \mathrm{~B} 2$ | B2 channel |
| $8,19,38,49$ | GND | Ground (0 V) |
| 17 | $\mathrm{~V}_{\mathrm{CC}}$ | Positive supply voltage |

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## ABSOLUTE MAXIMUM RATINGS ${ }^{1,2}$

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
| :---: | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC supply voltage |  | -0.5 to +7.0 | V |
| $\mathrm{I}_{\mathrm{IK}}$ | DC input diode current | $\mathrm{V}_{1}<0$ | -50 | mA |
| $\mathrm{~V}_{\mathrm{I}}$ | DC input voltage $^{3}$ |  | -0.5 to +7.0 | V |
| $\mathrm{~V}_{\text {OUT }}$ | DC output voltage $^{3}$ | output in Off or High state | -0.5 to +5.5 | V |
| $\mathrm{I}_{\text {OUT }}$ | DC output current | output in Low state | 128 | mA |
| $\mathrm{~T}_{\text {stg }}$ | Storage temperature range |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |

## NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed $150^{\circ} \mathrm{C}$.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS |  | UNIT |
| :---: | :--- | :---: | :---: | :---: |
|  |  | Min | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | DC supply voltage | 4.5 | 5.5 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | High-level input voltage | 2.0 | - | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level Input voltage | - | 0.8 | V |
| $\mathrm{~T}_{\mathrm{amb}}$ | Operating free-air temperature range | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{T}_{\text {amb }}=-40$ to $+85^{\circ} \mathrm{C}$ |  |  |  |
|  |  |  | Min | Typ ${ }^{1}$ | Max |  |
| $\mathrm{V}_{\mathrm{IK}}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ | - | - | -1.2 | V |
| $\mathrm{V}_{\mathrm{P}}$ | Output high pass voltage | See Figure 1, page 6 | - | - | -1.2 | V |
| 1 | Input leakage current | $\mathrm{V}_{\text {CC }}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$; $\mathrm{V}_{\mathrm{I}}=\mathrm{GND}$ or 5.5 V | - | - | $\pm 1$ |  |
| ICC | Quiescent supply current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} ; \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}}$ or GND | - | - | 3.5 | mA |
| $\Delta_{\text {l }}$ | Additional supply current per input pin ${ }^{2}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, one input at 3.4 V , other inputs at $\mathrm{V}_{\mathrm{CC}}$ or GND | - | - | 2.5 | mA |
| $\mathrm{C}_{1}$ | Control pins | $\mathrm{V}_{1}=3 \mathrm{~V}$ or 0 V | - | 4.5 | - | pF |
| $\mathrm{C}_{\text {IO(OFF) }}$ | Port OFF capacitance | $\mathrm{V}_{\mathrm{O}}=3 \mathrm{~V}$ or 0 V ; S0, S1, S2 $=0 \mathrm{~V}$ | - | 11.5 | - | pF |
| $\mathrm{ron}^{3}$ | A1 to A2 | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{V}_{1}=0 \mathrm{~V} ; \mathrm{I}_{\mathrm{I}}=64 \mathrm{~mA}$ | - | 5 | 8 | $\Omega$ |
|  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{V}_{1}=0 \mathrm{~V} ; \mathrm{I}_{\mathrm{I}}=30 \mathrm{~mA}$ | - | 5 | 8 |  |
|  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} ; \mathrm{V}_{1}=2.4 \mathrm{~V} ; \mathrm{I}_{\mathrm{I}}=15 \mathrm{~mA}$ | - | 16 | 35 |  |

## NOTES:

1. All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than $\mathrm{V}_{\mathrm{CC}}$ or GND.
3. Measured by the voltage drop between the $A$ and the $B$ terminals at the indicated current through the switch.

On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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## AC CHARACTERISTICS

GND $=0 \mathrm{~V} ; \mathrm{t}_{\mathrm{R}} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$

| SYMBOL | PARAMETER | FROM (INPUT) | $\begin{gathered} \text { TO } \\ \text { (OUTPUT) } \end{gathered}$ | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| $t_{\text {pd }}$ | Propagation delay ${ }^{1}$ | A or B | $B$ or $A$ | - | 0.25 | ns |
| $t_{\text {en }}$ | Output enable time to High and Low level | S | A or B | 2 | 11.5 | ns |
| $\mathrm{t}_{\text {dis }}$ | Output disable time from High and Low level | S | A or B | 1.5 | 8.5 | ns |

## NOTE

1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF , when driven by an ideal voltage source (zero output impedance).

## AC WAVEFORMS



Waveform 1. Input (An) to Output (Yn) Propagation Delays


Waveform 2. 3-State Output Enable and Disable Times

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Figure 1. Typical characteristics

## 24-bit level shifting bus exchange switch with 12-bit output enables



DIMENSIONS ( mm are the original dimensions)

| UNIT | $\mathbf{A}$ <br> max. | $\mathbf{A}_{\mathbf{1}}$ | $\mathbf{A}_{\mathbf{2}}$ | $\mathbf{A}_{\mathbf{3}}$ | $\mathbf{b}_{\mathbf{p}}$ | $\mathbf{c}$ | $\mathbf{D}^{(1)}$ | $\mathbf{E}^{(1)}$ | $\mathbf{e}$ | $\mathbf{H}_{\mathbf{E}}$ | $\mathbf{L}$ | $\mathbf{L}_{\mathbf{p}}$ | $\mathbf{Q}$ | $\mathbf{v}$ | $\mathbf{w}$ | $\mathbf{y}$ | $\mathbf{Z}^{(1)}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 2.8 | 0.4 | 2.35 | 0.25 | 0.3 | 0.22 | 18.55 | 7.6 | 0.635 | 10.4 | 1.4 | 1.0 | 1.2 | 0.25 | 0.18 | 0.1 | 0.85 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE <br> VERSION | REFERENCES |  |  | EUROPEAN | ISSUE DATE |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | PROJECTION | EIAJ |  |  |  |
| SOT371-1 |  | JEDEC | MO-118 |  |  |

## 24-bit level shifting bus exchange switch with 12-bit output enables


detail X


DIMENSIONS (mm are the original dimensions).

| UNIT | $\mathbf{A}$ <br> max. | $\mathbf{A}_{\mathbf{1}}$ | $\mathbf{A}_{\mathbf{2}}$ | $\mathbf{A}_{\mathbf{3}}$ | $\mathbf{b}_{\mathbf{p}}$ | $\mathbf{c}$ | $\mathbf{D}^{(1)}$ | $\mathbf{E}^{(2)}$ | $\mathbf{e}$ | $\mathbf{H}_{\mathbf{E}}$ | $\mathbf{L}$ | $\mathbf{L}_{\mathbf{p}}$ | $\mathbf{Q}$ | $\mathbf{v}$ | $\mathbf{w}$ | $\mathbf{y}$ | $\mathbf{Z}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| mm | 1.2 | 0.15 | 1.05 | 0.25 | 0.28 <br> 0.17 | 0.2 <br> 0.1 | 14.1 <br> 13.9 | 6.2 <br> 6.0 | 0.5 | 8.3 <br> 7.9 | 1.0 | 0.8 <br> 0.4 | 0.50 <br> 0.35 | 0.25 | 0.08 | 0.1 | 0.5 |
| 0.1 | $8^{0}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0.0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE <br> VERSION | REFERENCES |  |  | EUROPEAN PROJECTION | ISSUE DATE |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | IEC | JEDEC | EIAJ |  |  |
| SOT364-1 |  | MO-153 |  | - ¢ | $\begin{aligned} & -95-02-10 \\ & 99-12-27 \end{aligned}$ |

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CBTD16212

NOTES

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## Data sheet status

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