N a t i o n a l   S e m i c o n d u c t o r

May 1995

54F/74F398 • 54F/74F399
Quad 2-Port Register

General Description

The 'F398 and 'F399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

Features

■ Select inputs from two data sources
■ Fully positive edge-triggered operation
■ Both true and complement outputs—'F398
■ Guaranteed 4000V minimum ESD protection—'F399

Commercial	Military	Package Number	Package Description
74F398PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F398DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F398SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
	54F398FM (Note 2)	W20A	20-Lead Cerpack
	54F398LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74F399PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F399DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F399SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F399SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F399FM (Note 2)	W20A	20-Lead Cerpack
	54F399LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.
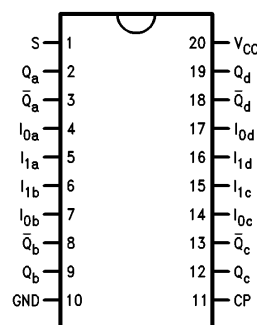
Connection Diagrams

'F398
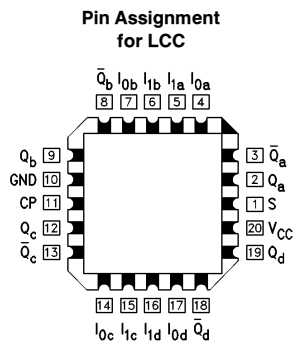
Pin Assignment for LCC
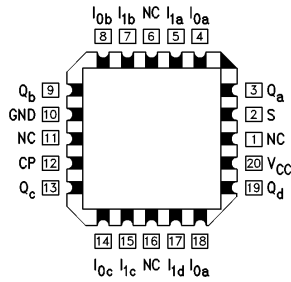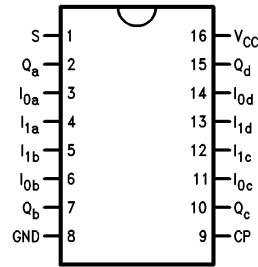
Pin Assignment for DIP, SOIC and Flatpak

TL/F/9533–5

TL/F/9533–6

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
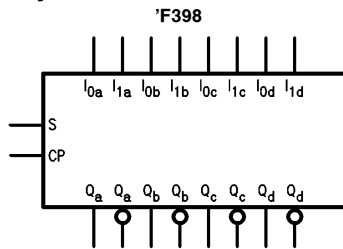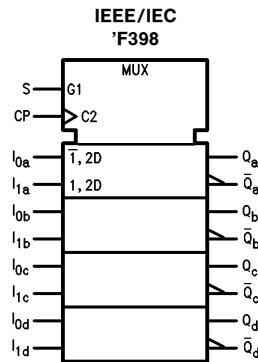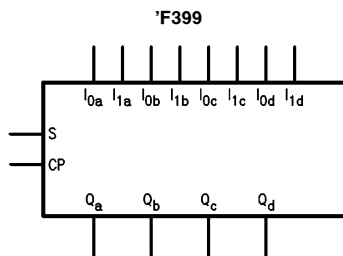
Connection Diagrams (Continued)

'F399

```
        I0b I1b NC I1a I0a
         8   7   6   5   4
Qb   9                     3  Qa
GND 10                     2  S
NC  11                     1  NC
CP  12                    20  VCC
Qc  13                    19  Qd
        14  15  16  17  18
        I0c I1c NC I1d I0a
```
TL/F/9533–7

```
S    — 1        16 — VCC
Qa   — 2        15 — Qd
I0a  — 3        14 — I0d
I1a  — 4        13 — I1d
I1b  — 5        12 — I1c
I0b  — 6        11 — I0c
Qb   — 7        10 — Qc
GND  — 8         9 — CP
```
TL/F/9533–8

Logic Symbols

'F398

```
        I0a I1a I0b I1b I0c I1c I0d I1d
   S
   CP
        Qa Qa Qb Qb Qc Qc Qd Qd
```
TL/F/9533–2

IEEE/IEC 'F398

```
              MUX
S  — G1
CP — ▷C2
I0a — 1, 2D          Qa
I1a — 1, 2D          Qa̅
I0b                  Qb
I1b                  Qb̅
I0c                  Qc
I1c                  Qc̅
I0d                  Qd
I1d                  Qd̅
```
TL/F/9533–1

'F399

```
        I0a I1a I0b I1b I0c I1c I0d I1d
   S
   CP
        Qa   Qb   Qc   Qd
```
TL/F/9533–4

'F399
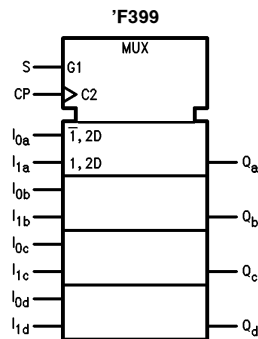
```
              MUX
S  — G1
CP — ▷C2
I0a — 1, 2D
I1a — 1, 2D          Qa
I0b
I1b                  Qb
I0c
I1c                  Qc
I0d
I1d                  Qd
```
TL/F/9533–3

Unit Loading/Fan Out

| Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S	Common Select Input	1.0/1.0	20 μA/−0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
I_{0a}–I_{0d}	Data Inputs from Source 0	1.0/1.0	20 μA/−0.6 mA
I_{1a}–I_{1d}	Data Inputs from Source 1	1.0/1.0	20 μA/−0.6 mA
Q_a–Q_d	Register True Outputs	50/33.3	−1 mA/20 mA
$\overline{Q}_a$–$\overline{Q}_d$	Register Complementary Outputs ('F398)	50/33.3	−1 mA/20 mA

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Functional Description

The 'F398 and 'F399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

Function Table

Inputs			Outputs	
S	I_0	I_1	Q	$\overline{Q}*$
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Immaterial
*'F398 only

Logic Diagram
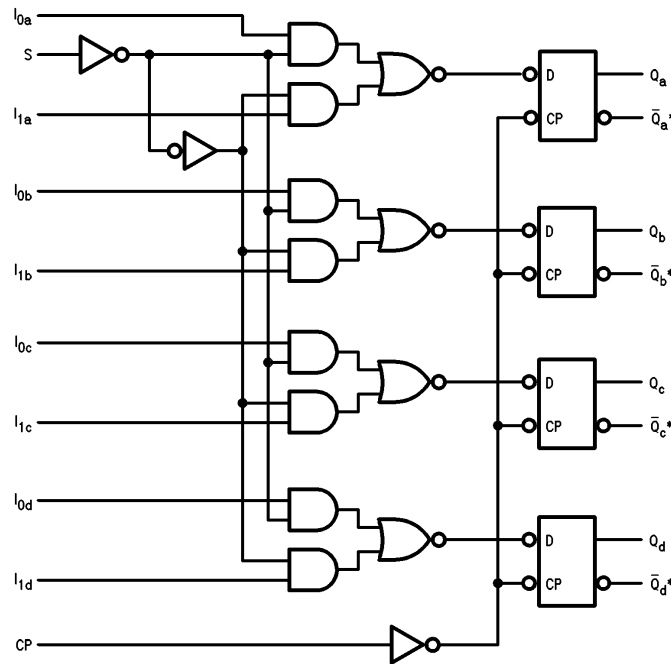
TL/F/9533–9

*'F398 Only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	$-0.5V$ to V_{CC}
TRI-STATE® Output	$-0.5V$ to $+5.5V$
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)—'F399	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9 \mu A$ All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CCH}	Power Supply Current ('F398)			25	38	mA	Max	$V_O = $ HIGH
I_{CCL}	Power Supply Current ('F398)			25	38	mA	Max	$V_O = $ LOW
I_{CCH}	Power Supply Current ('F399)			22	34	mA	Max	$V_O = $ HIGH
I_{CCL}	Power Supply Current ('F399)			22	34	mA	Max	$V_O = $ LOW

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AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			54F $T_A, V_{CC} = $ Mil $C_L = 50$ pF		74F $T_A, V_{CC} = $ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Input Clock Frequency	100	140		80		100		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$	3.0* 3.0	5.7 6.8	7.5 9.0	3.0 3.0	9.5 11.5	3.0 3.0	8.5 10.0	ns

*'F398 3.3 ns

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = $ Mil		74F $T_A, V_{CC} = $ Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I_n to CP	3.0 3.0		4.5 4.5		3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I_n to CP	1.0 1.0		1.5 1.5		1.0 1.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S to CP ('F398)	7.5 7.5		10.5 10.5		8.5 8.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW S to CP ('F399)	7.5 7.5		9.5 9.5		8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW S to CP	0 0		0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 5.0		4.0 7.0		4.0 5.0		ns

5

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

```
        74F    398/399    S    C    X
```

Temperature Range Family
    74F = Commercial
    54F = Military

Device Type

Package Code
    P = Plastic DIP
    D = Ceramic DIP
    F = Flatpak
    L = Leadless Chip Carrier (LCC)
    S = Small Outline SOIC JEDEC
    SJ = Small Outline SOIC EIAJ (74F399 only)

Special Variations
    QB = Military grade device with
           environmental and burn-in
           processing
    X = Devices shipped in 13″ reel

Temperature Range
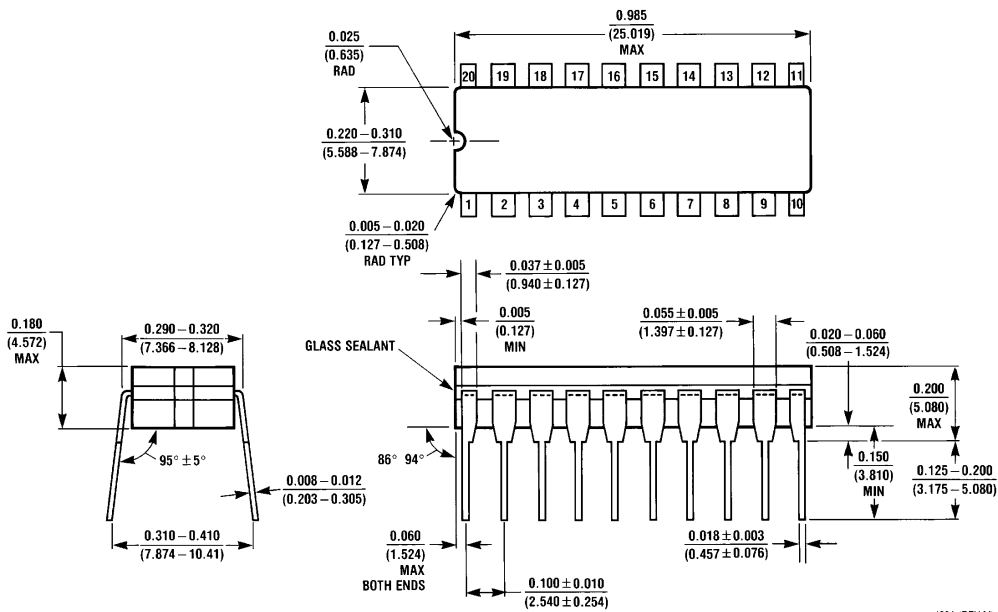   C = Commercial (0°C to +70°C)
    M = Military (−55°C to +125°C)

6

Physical Dimensions inches (millimeters)
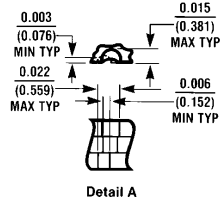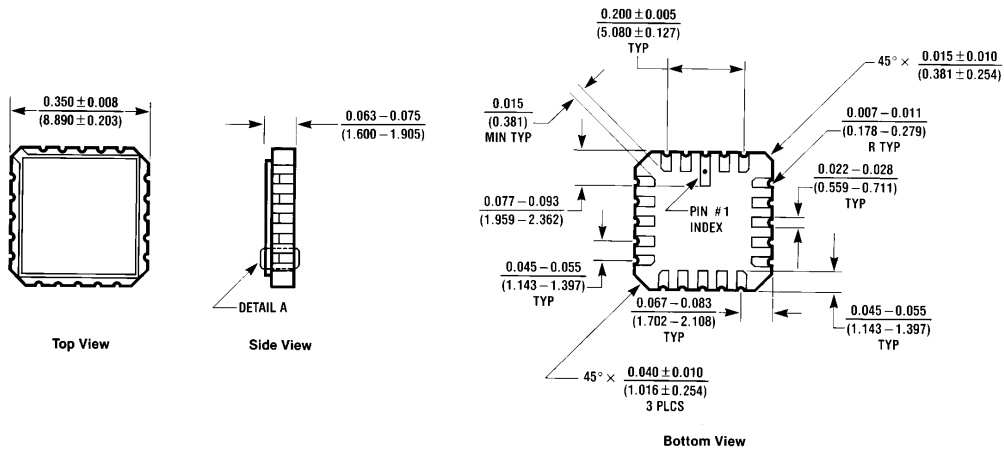
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Top View

0.350 ± 0.008
(8.890 ± 0.203)

Side View

$0.063 - 0.075$
$(1.600 - 1.905)$

DETAIL A

0.200 ± 0.005
(5.080 ± 0.127)
TYP

$45° \times \dfrac{0.015 \pm 0.010}{(0.381 \pm 0.254)}$

0.015
(0.381)
MIN TYP

$0.007 - 0.011$
$(0.178 - 0.279)$
R TYP

$0.077 - 0.093$
$(1.959 - 2.362)$

$0.022 - 0.028$
$(0.559 - 0.711)$
TYP

PIN #1
INDEX

$0.045 - 0.055$
$(1.143 - 1.397)$
TYP

$0.067 - 0.083$
$(1.702 - 2.108)$
TYP

$0.045 - 0.055$
$(1.143 - 1.397)$
TYP

$45° \times \dfrac{0.040 \pm 0.010}{(1.016 \pm 0.254)}$
3 PLCS

Bottom View

Detail A

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
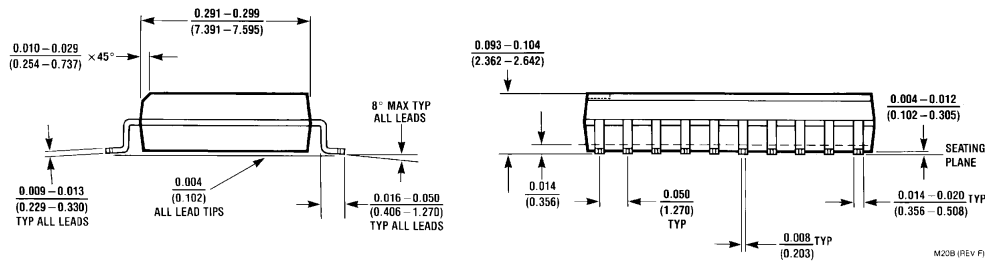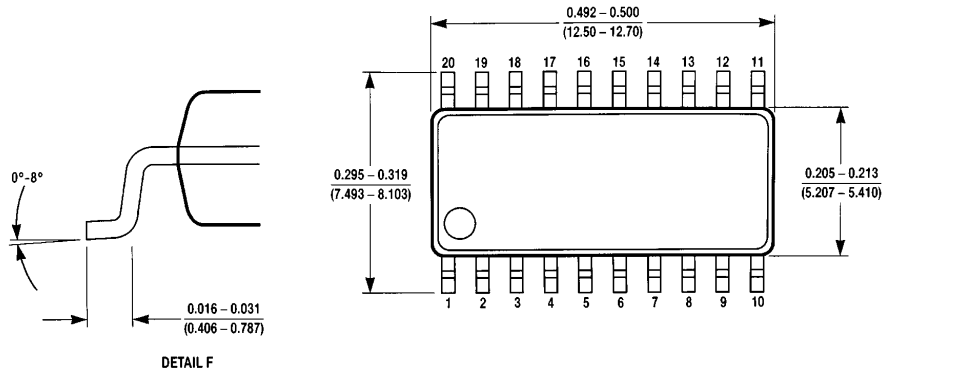(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

E20A (REV D)

20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

0.985
(25.019)
MAX

0.025
(0.635)
RAD

| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |

$0.220 - 0.310$
$(5.588 - 7.874)$

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

$0.005 - 0.020$
$(0.127 - 0.508)$
RAD TYP

0.037 ± 0.005
(0.940 ± 0.127)

0.180
(4.572)
MAX

$0.290 - 0.320$
$(7.366 - 8.128)$

GLASS SEALANT

0.005
(0.127)
MIN

0.055 ± 0.005
(1.397 ± 0.127)

$0.020 - 0.060$
$(0.508 - 1.524)$

0.200
(5.080)
MAX

$95° \pm 5°$

$86°$ $94°$

$0.008 - 0.012$
$(0.203 - 0.305)$

0.150
(3.810)
MIN

$0.125 - 0.200$
$(3.175 - 5.080)$

$0.310 - 0.410$
$(7.874 - 10.41)$

0.060
(1.524)
MAX
BOTH ENDS

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

J20A (REV M)

7

Physical Dimensions inches (millimeters) (Continued)

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

30° TYP

0.010
(0.254) MAX

1 2 3 4 5 6 7 8 9 10

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.014
(0.356)

0.050
(1.270)
TYP

0.014 − 0.020
(0.356 − 0.508) TYP

0.008
(0.203) TYP

M20B (REV F)

20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

0.492 − 0.500
(12.50 − 12.70)

20 19 18 17 16 15 14 13 12 11

0.295 − 0.319
(7.493 − 8.103)

0.205 − 0.213
(5.207 − 5.410)

1 2 3 4 5 6 7 8 9 10

0°-8°

0.016 − 0.031
(0.406 − 0.787)

DETAIL F

0.071
(1.803) REF

0.067 − 0.083
(1.702 − 2.108)

0.006 − 0.010
(0.152 − 0.254)

SEATING PLANE

0.049
(1.245) REF

0.050
(1.270)

0.000 − 0.010
(0.000 − 0.254)

SEE DETAIL F

0.014 − 0.020
(0.356 − 0.508)

M20D (REV A)
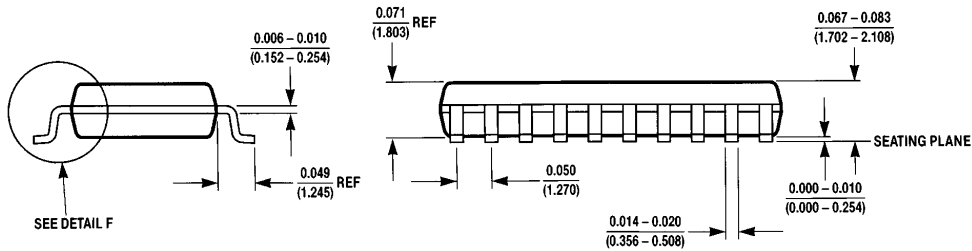
20-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D

8

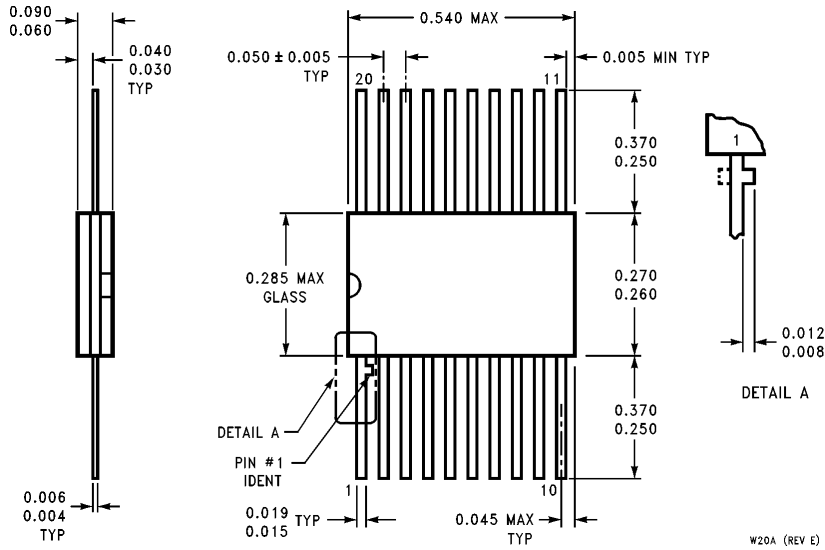# Physical Dimensions inches (millimeters) (Continued)
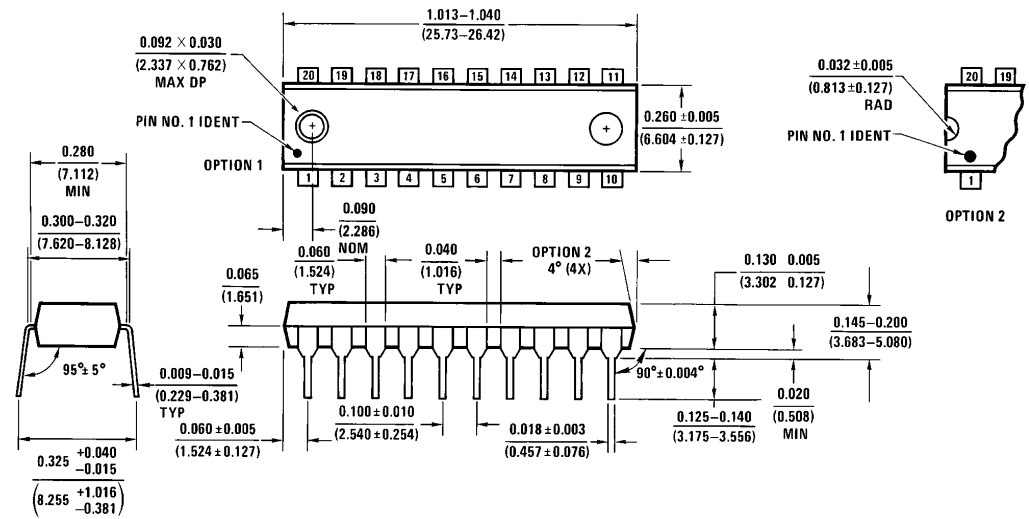
20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

N20A (REV G)

Physical Dimensions inches (millimeters) (Continued)

0.090
0.060

0.040
0.030
TYP

0.540 MAX

0.050 ± 0.005
TYP

0.005 MIN TYP

20   11

0.370
0.250

0.285 MAX
GLASS

0.270
0.260

0.006
0.004
TYP

DETAIL A

PIN #1
IDENT

0.370
0.250

1   10

0.019
0.015
TYP

0.045 MAX
TYP

0.012
0.008

DETAIL A

W20A (REV E)

20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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