19-2075; Rev 2; 10/02

Integrated Cellular RF-Section Power-Management IC

General Description

The MAX8890 is a power-management IC intended for cellular handsets using a single lithium-ion (Li+) cell battery with input voltages from +2.5V to +5.5V. The IC contains three identical, low-noise, low-dropout (LDO) linear regulators to provide all of the supply voltage requirements for the RF portion of the handset.

The first LDO is intended to power the transmitter, receiver, and synthesizer. The second LDO is intended to power the TCXO, and high-power voltage-controlled oscillators (VCOs). The third LDO is intended to power the UHF offset VCO.

Each LDO has its own individual enable (ON/$\overline{\text{OFF}}$) control to maximize design flexibility. The reference is powered on if any of the enable inputs (EN1, EN2, EN3) are logic high. The high-accuracy output voltage of each LDO is preset at an internally trimmed voltage (1.8V to 3.3V in 50mV increments). Each LDO is capable of supplying 100mA with a low 50mV dropout and is optimized for low noise and high crosstalk-isolation. Designed with internal P-channel MOSFET pass transistors, the MAX8890's low 180µA operating supply current is independent of load.

Other features include short-circuit and thermal-overload protection. The MAX8890 is available in a compact, high-power, 12-pin 4mm × 4mm QFN package with a metal pad on the underside.

Applications

Cellular Handsets

Single-Cell Li+ Systems

3-Cell NiMH, NiCD, or Alkaline Systems

Personal Digital Assistants (PDAs)

Standard Preset Output Voltage Suffixes

SUFFIX	OUTPUT VOLTAGE (V)	SUFFIX	OUTPUT VOLTAGE (V)
A	3.30	H	2.75
B	3.00	J	2.70
D	2.90	K	2.50
F	2.85	L	2.00
G	2.80	M	1.80

**Nonstandard output voltages between 1.80V and 3.30V are available in 50mV increments.*

Standard Versions table and Pin Configuration appear at end of data sheet.

Features

- ♦ **Three 100mA Low-Dropout Linear Regulators**
- ♦ **Low 50mV Dropout Voltage at 100mA**
- ♦ **±1% Output Voltage Accuracy Over Temperature**
- ♦ **Preset 1.8V to 3.3V Output Voltages (in 50mV Increments)**
- ♦ **Low $45\mu V_{RMS}$ Output Voltage Noise**
- ♦ **Low 180µA Operating Supply Current**
- ♦ **2.5V to 5.5V Input Voltage Range**
- ♦ **67dB PSRR**
- ♦ **$10\mu V_{P-P}$ Channel-to-Channel Crosstalk**
- ♦ **Short-Circuit Protection**
- ♦ **Thermal-Overload Protection**
- ♦ **0.01µA Shutdown Current**
- ♦ **Tiny 12-Pin 4mm x 4mm QFN Package**

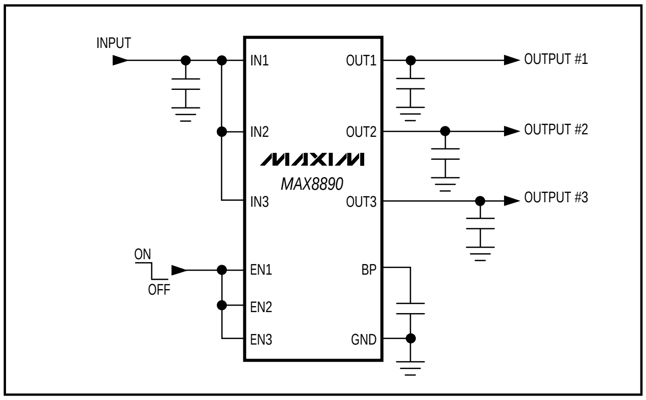
Ordering Information

PART	TEMP RANGE	PIN PACKAGE
MAX8890ETCxyz*	-40°C to +85°C	12 (4mm x 4mm) QFN

**Each preset output voltage of these devices is factory trimmed to one of ten voltages. Replace "xyz" with the letters corresponding to the desired output voltages (see Standard Preset Output Voltage Suffixes table), where the three letter suffix corresponds to the following output voltages: "x" = V_{OUT1}, "y" = V_{OUT2}, and "z" = V_{OUT3}.*

***Note:** There are five standard versions available (see Standard Versions table). Sample stock is generally held on standard versions only. Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact the factory for availability of nonstandard versions.*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

IN_, EN_ to GND	-0.3V to +6V
OUT_, BP to GND	-0.3V to ($V_{IN\_}$ + 0.3V)
Output Short-Circuit Protection (Note A)	indefinite
Continuous Power Dissipation (T_A = +70°C)	
12-Pin 4 x 4 QFN (derate 16.9mW/°C above +70°C)	1349mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note A: As long as the maximum continuous power dissipation rating is not exceeded, the output can be shorted indefinitely.

ELECTRICAL CHARACTERISTICS

($V_{IN\_}$ = 3.6V, EN_ = IN_, C_{IN} = 6.8µF, $C_{OUT\_}$ = 2.2µF, C_{BP} = 0.01µF, all ceramic capacitors **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Input Voltage	$V_{IN\_}$			2.5		5.5	V
Input Undervoltage Lockout Threshold	V_{UVLO}	Rising and falling edge		2.10	2.25	2.45	V
Input Undervoltage Hysteresis					45		mV
SUPPLY CURRENT							
Quiescent Supply Current	I_Q	$I_{OUT\_}$ = 0			180	330	µA
Shutdown Supply Current		EN_ = OUT_ = GND			0.01	10	µA
LINEAR REGULATORS							
Output Voltage Accuracy	$V_{OUT\_}$	$V_{IN\_}$ = 0.5V + the highest of (V_{OUT1}, V_{OUT2}, or V_{OUT3}), $I_{OUT\_}$ = 1mA to 100mA	T_A = +85°C	-1		+1	%
			T_A = 0°C +85°C	-2		+2	
Current Limit	I_{LIM}	OUT_ = GND		120	250	500	mA
Output Pulldown Resistance	$R_{OUT\_}$	EN_ = GND		3	5	8	kΩ
Dropout Voltage (Note 1)	$V_{IN\_}$ - $V_{OUT\_}$	$I_{OUT\_}$ = 1mA			1		mV
		$I_{OUT\_}$ = 50mA			25		
		$I_{OUT\_}$ = 100mA			50	100	
Line Regulation		$V_{IN\_}$ = ($V_{OUT\_}$+ 0.1V) to 5.5V for $V_{OUT\_} \geq$ 2.4V, or $V_{IN\_}$ = 2.5V to 5.5V for $V_{OUT\_}$ < 2.4V, I_{OUT} = 1mA		-0.15		+0.15	%/V
Output Voltage Noise		10Hz to 100kHz, $C_{OUT\_}$ = 10µF ceramic, $V_{OUT\_}$ = 2.8V, $I_{OUT\_}$ = 10mA			45		μV_{RMS}
Output Voltage PSRR		100Hz, $C_{OUT\_}$ = 2.2µF ceramic, $I_{OUT\_}$ = 10mA			67		dB
Channel-to-Channel Isolation		10kHz, $C_{OUT\_}$ = 2.2µF ceramic, $I_{OUT\_}$ = 10mA			64		dB

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = 3.6V, EN_ = IN_, C_{IN} = 6.8µF, $C_{OUT\_}$ = 2.2µF, C_{BP} = 0.01µF, all ceramic capacitors **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE LOGIC CONTROL						
EN_ Input Threshold	$V_{EN\_}$	2.5V ≤ $V_{IN\_}$ ≤ 5.5V	0.4		1.6	V
EN_ Input Bias Current	$I_{EN\_}$	$V_{EN\_}$ = 5.5V or 0, T_A = +85°C	-1		+1	µA
THERMAL PROTECTION						
Thermal-Shutdown Temperature	T_{SHDN}	Rising temperature		160		°C
Thermal-Shutdown Hysteresis	ΔT_{SHDN}			15		°C

ELECTRICAL CHARACTERISTICS

($V_{IN\_}$ = 3.6V, EN_ = IN_, C_{IN} = 6.8µF, $C_{OUT\_}$ = 2.2µF, C_{BP} = 0.01µF, all ceramic capacitors **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
GENERAL					
Input Voltage	$V_{IN\_}$		2.5	5.5	V
Input Undervoltage Lockout Threshold	V_{UVLO}	Rising and falling edge	2.10	2.45	V
SUPPLY CURRENT					
Quiescent Supply Current	I_Q	$I_{OUT\_}$ = 0		330	µA
Shutdown Supply Current		EN_ = OUT_ = GND		10	µA
LINEAR REGULATORS					
Output Voltage Accuracy	$V_{OUT\_}$	$V_{IN\_}$ = 0.5V + the highest of (V_{OUT1}, V_{OUT2}, or V_{OUT3}), $I_{OUT\_}$ = 1mA to 100mA	-2	+2	%
Current Limit	I_{LIM}	OUT_ = GND	110	500	mA
Output Pulldown Resistance	$R_{OUT\_}$	EN_ = GND	3	8	kΩ
Dropout Voltage	$V_{IN\_}$ - $V_{OUT\_}$	$I_{OUT\_}$ = 100mA (Note 1)		100	mV
Line Regulation		$V_{IN\_}$ = ($V_{OUT\_}$+ 0.1V) to 5.5V for $V_{OUT\_}$ ≥ 2.4V, or $V_{IN\_}$ = 2.5V to 5.5V for $V_{OUT\_}$ < 2.4V, I_{OUT} = 1mA	-0.15	+0.15	%/V
ENABLE LOGIC CONTROL					
EN_ Input Threshold	$V_{EN\_}$	2.5V ≤ $V_{IN\_}$ ≤ 5.5V	0.4	1.6	V
EN_ Input Bias Current	$I_{EN\_}$	$V_{EN\_}$ = 5.5V or 0, T_A = +85°C	-1	+1	µA

Note 1: The dropout voltage is defined as $V_{IN\_}$ - $V_{OUT\_}$, when $V_{OUT\_}$ is 100mV below the set output voltage (the value of $V_{OUT\_}$ for $V_{IN\_}$ = $V_{OUT\_}$ + 500mV). Since the minimum input voltage range is 2.5V, this specification is only meaningful when the set output voltage exceeds 2.7V ($V_{OUT\_(NOM)}$ ≥ 2.7V).

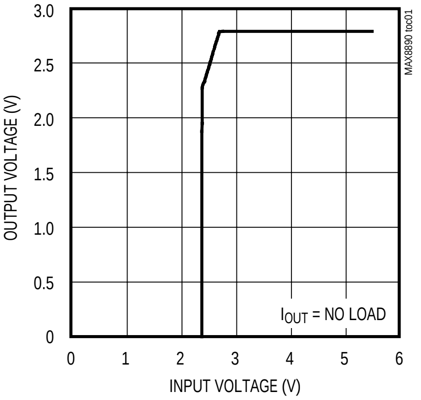
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Integrated Cellular RF-Section Power-Management IC

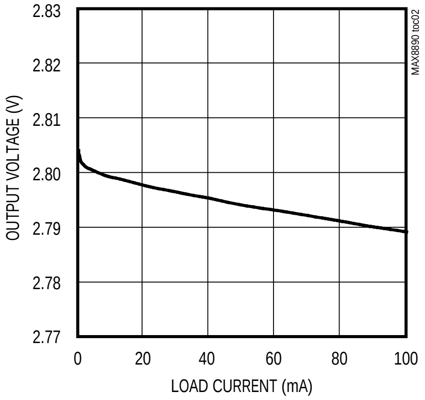
Typical Operating Characteristics

(Circuit of Figure 1, MAX8890ETCGGG, V_{IN} = 3.3V, EN_ = IN_, T_A = +25°C, unless otherwise noted.)

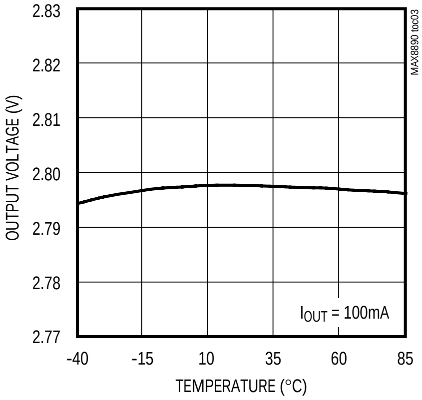
OUTPUT VOLTAGE vs. INPUT VOLTAGE



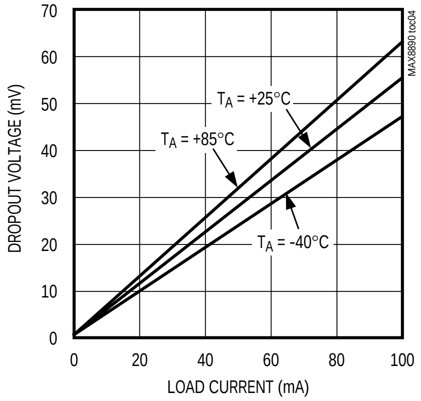
OUTPUT VOLTAGE vs. LOAD CURRENT



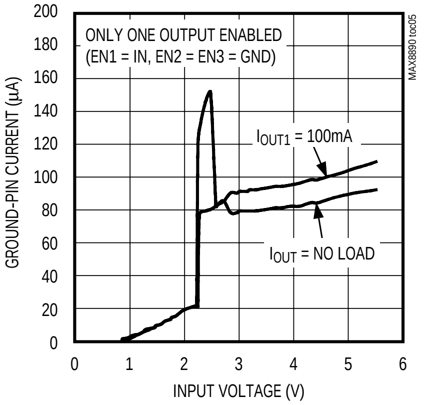
OUTPUT VOLTAGE vs. TEMPERATURE



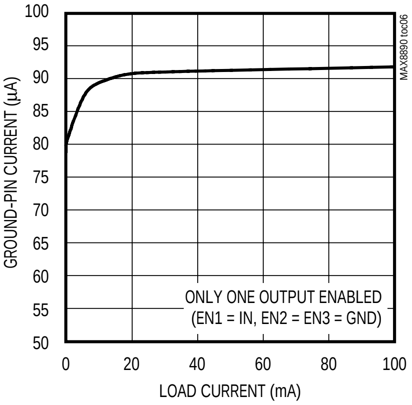
DROPOUT VOLTAGE vs. LOAD CURRENT



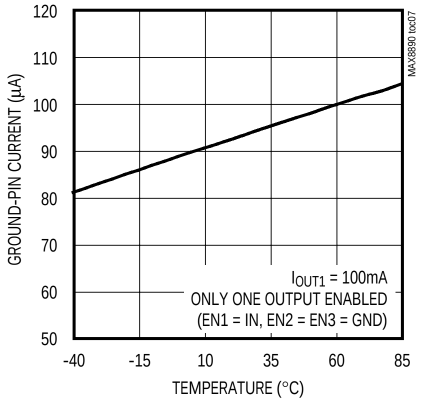
GROUND-PIN CURRENT vs. INPUT VOLTAGE



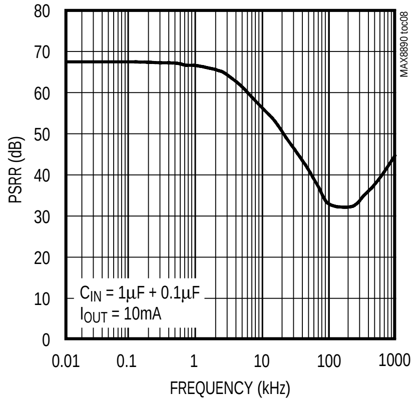
GROUND-PIN CURRENT vs. LOAD CURRENT



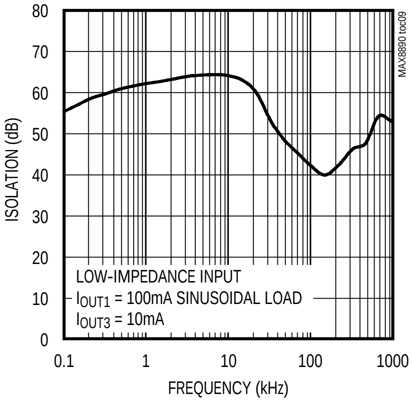
GROUND-PIN CURRENT vs. TEMPERATURE



POWER-SUPPLY REJECTION RATIO



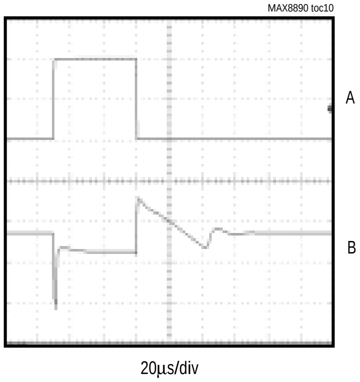
CHANNEL-TO-CHANNEL ISOLATION



Typical Operating Characteristics (continued)

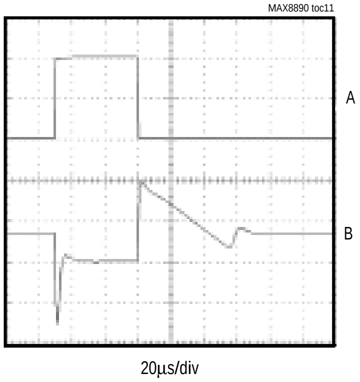
(Circuit of Figure 1, MAX8890ETCGGG, V_{IN} = 3.3V, EN_ = IN_, T_A = +25°C, unless otherwise noted.)

LOAD TRANSIENT



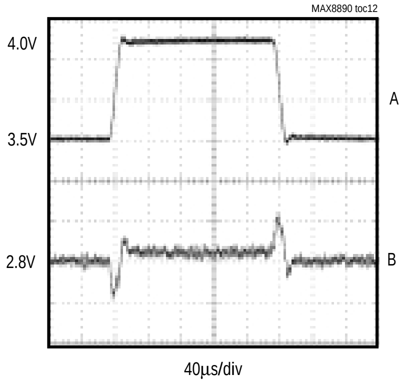
A. $I_{OUT\_}$ = 1mA to 100mA, 50mA/div
B. $V_{OUT\_}$ = 2.8V, 20mV/div
V_{IN} = 3.3V ($V_{OUT\_}$ +500mV)

LOAD TRANSIENT NEAR DROPOUT



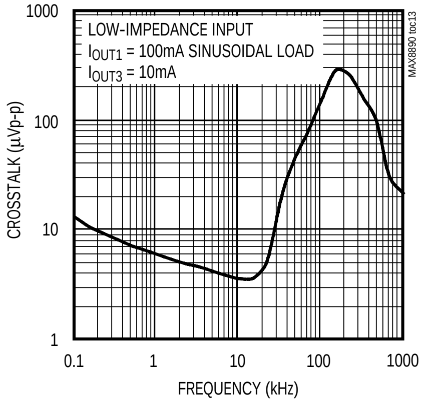
A. $I_{OUT\_}$ = 1mA to 100mA, 50mA/div
B. $V_{OUT\_}$ = 2.8V, 20mV/div
V_{IN} = 2.9V ($V_{OUT\_}$ + 100mV)

LINE TRANSIENT RESPONSE

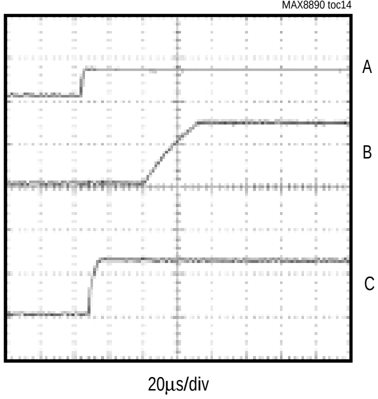


A. V_{IN} = 3.5V to 4.0V, 200mV/div
B. $V_{OUT\_}$ = 2.8V, 2mV/div
I_{OUT} = 100mA

CROSSTALK VOLTAGE

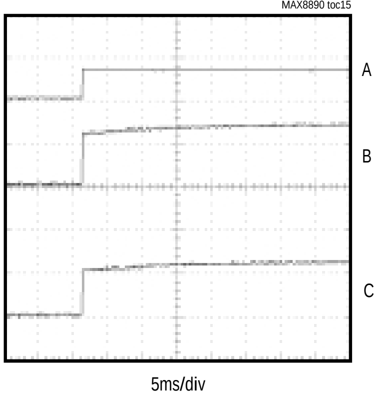


STARTUP WAVEFORM (C_{BP} = 0.01µF)



A. V_{IN} = 0 to 3.3V, 5V/div
B. $V_{OUT\_}$ = 2.8V, 2V/div
C. V_{BP} = 1.25V, 1V/div
$R_{OUT\_}$ = 28Ω (100mA)

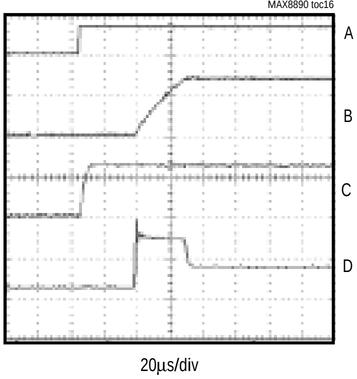
STARTUP WAVEFORM (C_{BP} = 0.1µF)



A. V_{IN} = 0 to 3.3V, 5V/div
B. $V_{OUT\_}$ = 2.8V, 2V/div
C. V_{BP} = 1.25V, 1V/div
$R_{OUT\_}$ = 28Ω (100mA)

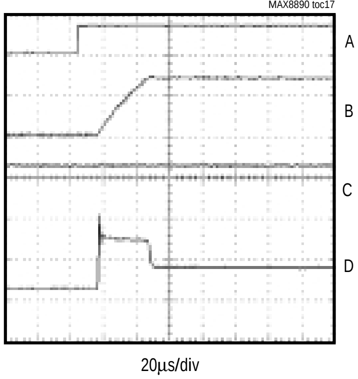
Typical Operating Characteristics (continued)

(Circuit of Figure 1, MAX8890ETCGGG, V_{IN} = 3.3V, EN_ = IN_, T_A = +25°C, unless otherwise noted.)



ENABLE WAVEFORM (1ST OUTPUT)

A. V_{EN1} = 0 to 3.3V, 5V/div
B. V_{OUT1} = 2.8V, R_{OUT1} = 28Ω (100mA), 2V/div
C. V_{BP} = 1.25V, 1V/div
D. I_{IN}, 200mA/div
V_{IN} = 3.3V, EN2 = EN3 = GND, C_{BP} = 0.01µF



ENABLE WAVEFORM (2ND OUTPUT)

A. V_{EN2} = 0 to 3.3V, 5V/div
B. V_{OUT2} = 2.8V, R_{OUT2} = 28Ω (100mA), 2V/div
C. V_{BP} = 1.25V, 1V/div
D. I_{IN}, 200mA/div
V_{IN} = 3.3V, EN1 = IN, EN3 = GND, C_{BP} = 0.01µF

Pin Description

PIN	NAME	FUNCTION
1	IN1	Regulator 1 Input. Supply voltage can range from 2.5V to 5.5V. Bypass with a capacitor to GND (see *Capacitor Selection and Regulator Stability* section).
2	IN2	Regulator 2 Input. Supply voltage can range from 2.5V to V_{IN1}. Bypass with a capacitor to GND (see *Capacitor Selection and Regulator Stability* section).
3	OUT2	Regulator 2 Output. Sources up to 100mA. Bypass with a 2.2µF ceramic capacitor to GND.
4	EN1	Active-High Enable Input for Regulator 1. A logic low shuts down the first linear regulator. In shutdown, OUT1 is pulled low through an internal 5kΩ resistor. Connect to IN1 for normal operation.
5	EN2	Active-High Enable Input for Regulator 2. A logic low shuts down the second linear regulator. In shutdown, OUT2 is pulled low through an internal 5kΩ resistor. Connect to IN2 for normal operation.
6	EN3	Active-High Enable Input for Regulator 3. A logic low shuts down the third linear regulator. In shutdown, OUT3 is pulled low through an internal 5kΩ resistor. Connect to IN3 for normal operation.
7	BP	1.25V Voltage Reference Bypass Pin. Connect a 0.01µF ceramic bypass capacitor from BP to GND to minimize the output noise. Make no other connection to this pin.
8	GND	Ground. Connect both ground pins together externally, as close to the IC as possible.
9	IN3	Regulator 3 Input. Supply voltage can range from 2.5V to V_{IN1}. Bypass with a capacitor to GND (see *Capacitor Selection and Regulator Stability* section).
10	OUT3	Regulator 3 Output. Sources up to 100mA. Bypass with a 2.2µF ceramic capacitor to GND.
11	GND	Ground. Connect both ground pins together externally, as close to the IC as possible.
12	OUT1	Regulator 1 Output. Sources up to 100mA. Bypass with a 2.2µF ceramic capacitor to GND.
EP	GND	Ground. **THE EXPOSED PAD AND ALL FOUR CORNER TABS ON THE QFN PACKAGE ARE INTERNALLY CONNECTED TO GROUND.** The exposed pad functions as a heatsink. Solder to a large pad or to the circuit board ground plane to maximize power dissipation. Do not use as device ground.

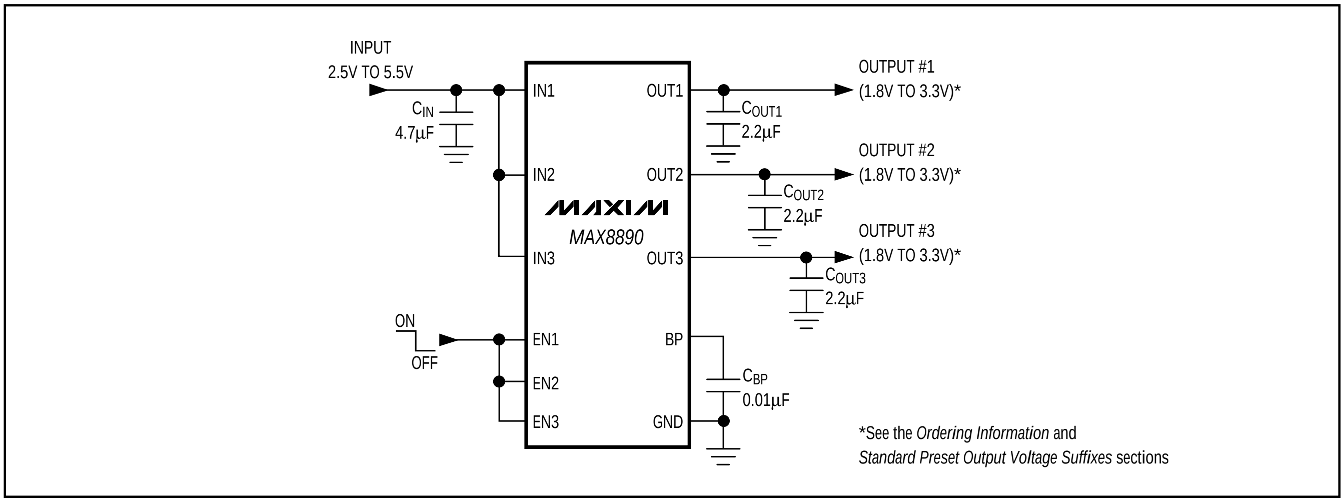


Figure 1. Typical Application Circuit

Detailed Description

The MAX8890 is an RF power-management IC for a cellular phone. The MAX8890 contains three low-noise, low quiescent current, low-dropout, linear regulators for powering the transmitter, receiver, synthesizer, TCXO, and voltage controlled oscillators (VCOs). Each low-dropout linear regulator (LDO) supplies loads up to 100mA and is available with preset output voltages from 1.8V to 3.3V in 50mV increments. Furthermore, the MAX8890's input voltage range of 2.5V to 5.5V is perfect for single-cell Li+ battery or 3-cell NiMH battery applications.

As illustrated in Figure 2, each regulator consists of an error amplifier, internal feedback resistive-divider, and P-channel MOSFET pass transistor. The output voltage feeds back through the internal resistive-divider connected to OUT_. This feedback voltage connects to the error amplifier, which compares the feedback voltage with the internal 1.25V reference voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, which allows more current to flow to the output and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to flow to the output.

Clear transmission and reception in a cellular phone can only be achieved with a low-noise power supply. Therefore, all three LDOs on the MAX8890 feature low output voltage noise, high power-supply rejection ratios, and excellent load and line regulation characteristics. Designed for single-cell Li+ battery applications where a pulsed current demand is required from the battery, each LDO is designed with $45\mu V_{RMS}$ noise from 10Hz to 100kHz and PSRR of 67dB.

The MAX8890 also features output current limiting (short-circuit protection), a low-power shutdown mode, and thermal overload protection.

Internal P-Channel Pass MOSFET

Each linear regulator features a 0.5Ω P-channel MOSFET pass transistor. Unlike similar designs using PNP pass transistors, P-channel MOSFETs require no base drive, which reduces the quiescent current. PNP based regulators also waste considerable current in dropout when the pass transistor saturates and use high base-drive currents under large loads. The MAX8890 does not suffer from these problems and consumes only 180µA of quiescent current (all three regulators enabled).

Current Limit (Short-Circuit Protection)

The MAX8890 contains separate current-limit circuitry for each linear regulator. The device monitors and controls the gate voltage of each pass transistor, limiting the regulator's output current to 250mA (typ). The output can be shorted to ground for an indefinite period of time without damage to the part as long as the maximum continuous power dissipation rating is not exceeded.

Output Voltage Selection

The MAX8890 is supplied with factory-set output voltages from 1.8V to 3.3V in 50mV increments. The three-letter part number suffix identifies the output voltage for each regulator. For example, the MAX8890ETCAKM's output voltages are preset to 3.3V (V_{OUT1}), 2.5V (V_{OUT2}), and 1.8V (V_{OUT3}).

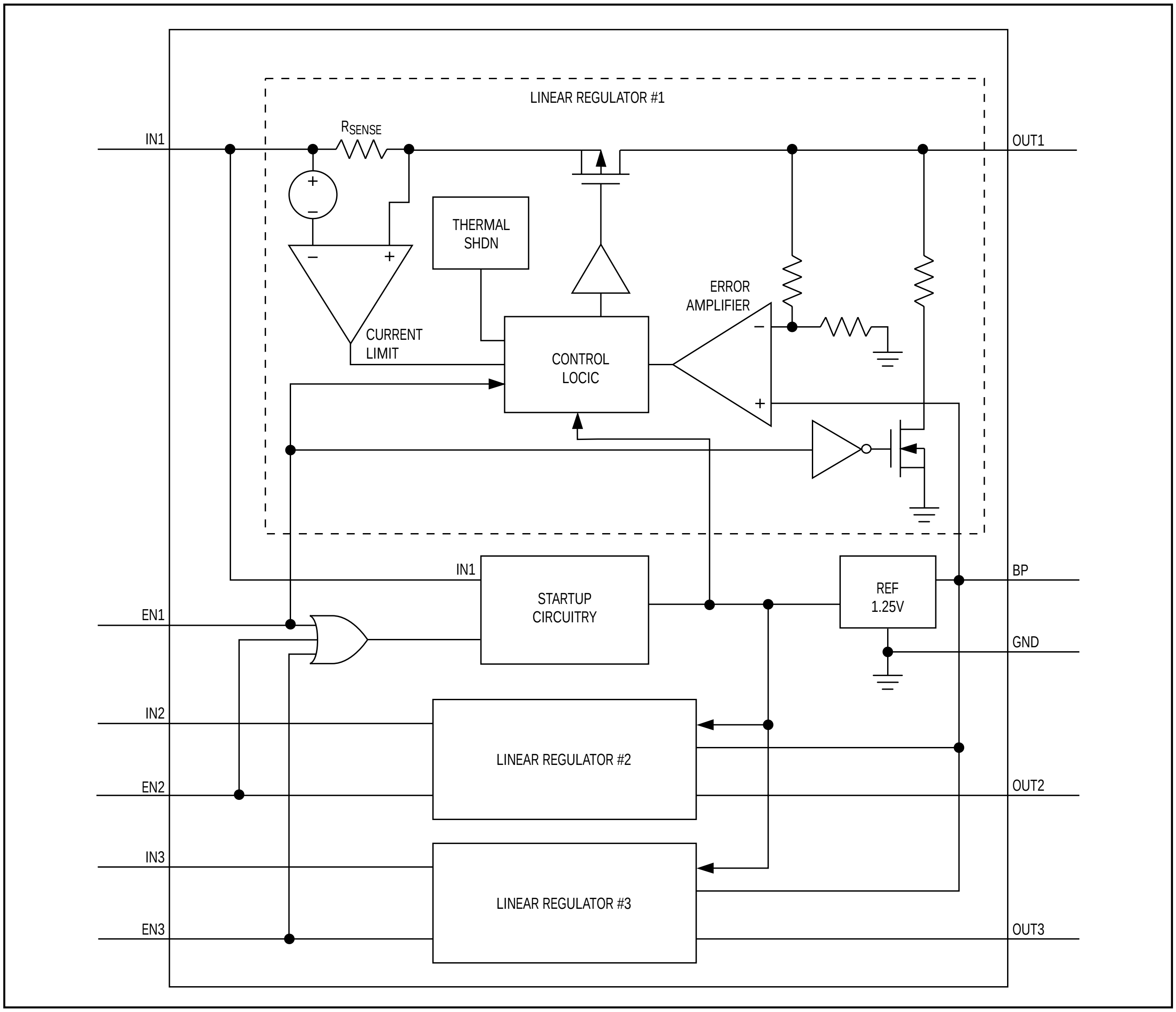


Figure 2. Functional Diagram

Enable

If any one of the three low-dropout linear regulators (LDOs) is enabled, the internal 1.25V reference powers up. Therefore, all three LDOs must be disabled to shut down the internal reference, reducing the supply current to 0.01µA.

Pull EN_ low to enter shutdown. When any one of the linear regulators is shutdown, the corresponding MAX8890 output disconnects from the corresponding input, and the output discharges through an internal 5kΩ resistor. The capacitance and load determine the rate at which $V_{OUT\_}$ decays. Do not leave EN_ floating. Connect EN_ to IN_ for normal operation. EN_ can be pulled as high as 6V, regardless of the input and output voltages.

Thermal-Overload Protection

Thermal-overload protection limits the MAX8890's total power dissipation in the event of fault conditions. Each linear regulator has its own thermal-shutdown circuitry.

When the junction temperature exceeds T_J = 160°C, a thermal sensor activates the shutdown logic, disabling the overheated regulator. The thermal sensor turns the linear regulator on again after the regulator's junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = 150°C.

Applications Information

Capacitor Selection and Regulator Stability

Capacitors are required at each input and each output of the MAX8890 for stable operation over the full load range and full temperature range. Connect a minimum 2.2µF ceramic capacitor between OUT_ and ground to ensure stability and optimum transient response. Use larger 10µF ceramic output capacitors for lower noise requirements.

The input capacitor ($C_{IN\_}$) lowers the source impedance of the input supply, thereby reducing the input noise and improving transient response. Connect a minimum 1µF ceramic capacitance between each IN_ and ground. Place all input and output capacitors as close to the MAX8890 as possible to minimize the impact of PC board trace impedance. Because IN1 and IN2 are next to each other, they may easily share a single 2.2µF or larger ceramic capacitor.

Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. However, note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. Z5U and Y5V dielectrics may require a minimum 3.3µF nominal output capacitance, especially with low temperature operation.

Reference Bypass Capacitor

An external bypass capacitor is connected to BP to reduce the inherent reference noise. The capacitor forms a lowpass filter in conjunction with an internal network. Use a 0.01µF or greater ceramic capacitor connected as close to BP as possible. Capacitance values greater than 0.01µF will increase the startup time. (See *Typical Operating Characteristics* for startup waveforms.) For the lowest noise, increase the bypass capacitor to 0.1µF. Values above 0.1µF provide no performance improvement and are therefore not recommended. Do not place any additional loading on this reference bypass pin.

Noise, PSRR, and Transient Response

The MAX8890 is designed to operate with low dropout voltages and low quiescent currents in battery-powered systems while providing low noise, fast transient response, and high AC rejection. See the *Typical Operating Characteristics* for a plot of Power-Supply Rejection Ratio (PSRR) vs. Frequency. When operating from noisy sources, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques.

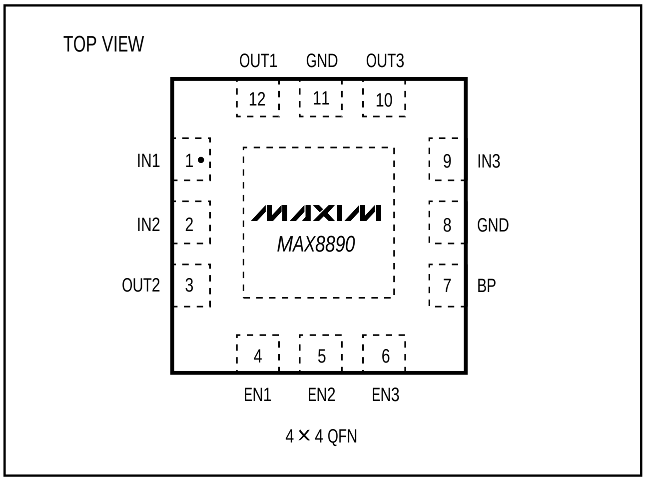
The MAX8890 load-transient response graphs (see *Typical Operating Characteristics*) show two components of the output response: a DC shift from the output impedance due to the load current change and the transient response. Increasing the output capacitor's value and decreasing the ESR reduces the transient under/overshoot.

Input-Output (Dropout) Voltage

A regulator's minimum input-to-output voltage differential (dropout voltage) determines the lowest useable input supply voltage. Once the linear regulator reaches dropout, the series pass transistor is fully on and regulation ceases. The output voltage tracks the input voltage as the input voltage drops lower. Because the MAX8890 uses P-channel MOSFET pass transistors, its dropout voltage is a function of the MOSFET's drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current (see *Typical Operating Characteristics*):

$$V_{DROPOUT} = V_{IN\_} - V_{OUT\_} = R_{DS(ON)} \times I_{OUT\_}$$

Pin Configuration



Standard Versions

VERSION	TOP MARK
MAX8890ETCAAA	AABG
MAX8890ETCDDD	AABH
MAX8890ETCGGG	AABI
MAX8890ETCMMM	AABJ
MAX8890ETCAKM	AABK
MAX8890ETCABK	AABN

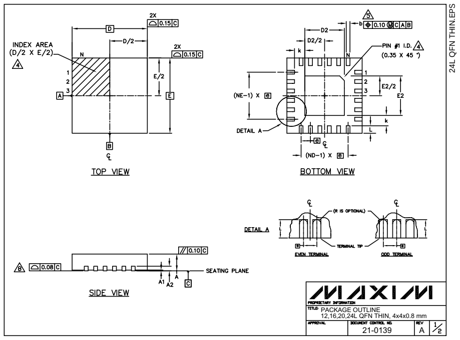
Chip Information

TRANSISTOR COUNT: 1472

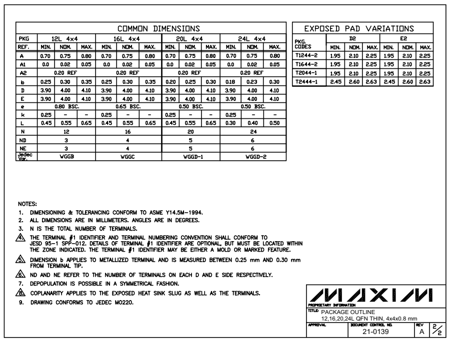
PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV A | 1/2



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV A | 2/2

Package Information (continued)

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