

General Description

The MXB7846 is an industry-standard 4-wire touchscreen controller. It contains a 12-bit sampling analogto-digital converter (ADC) with a synchronous serial interface and low on-resistance switches for driving resistive touch screens. The MXB7846 uses an internal +2.5V reference or an external reference. The MXB7846 can make absolute or ratiometric measurements. In addition, this device has an on-chip temperature sensor, a battery-monitoring channel, and has the ability to perform touch-pressure measurements without external components. The MXB7846 has one auxiliary ADC input. All analog inputs are fully ESD protected, eliminating the need for external TransZorb™ devices.

The MXB7846 is guaranteed to operate with a supply voltage down to +2.375V when used with an external reference or +2.7V with an internal reference. In shutdown mode, the typical power consumption is reduced to under 0.5µW, while the typical power consumption at 125ksps throughput and a +2.7V supply is 650µW.

Low-power operation makes the MXB7846 ideal for battery-operated systems, such as personal digital assistants with resistive touch screens and other portable equipment. The MXB7846 is available in 16-pin QSOP and TSSOP packages, and is guaranteed over the -40°C to +85°C temperature range.

Applications

Personal Digital Assistants Portable Instruments Point-of-Sales Terminals **Pagers Touch-Screen Monitors** Cellular Phones

Typical Application Circuit appears at end of data sheet.

TransZorb is a trademark of Vishay Intertechnology, Inc. SPI/QSPI are trademarks of Motorola, Inc.

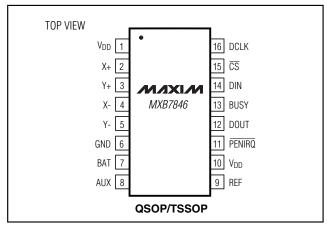
Features

- **♦ ESD-Protected ADC Inputs** ±15kV IEC 61000-4-2 Air-Gap Discharge ±8kV IEC 61000-4-2 Contact Discharge
- ♦ Pin Compatible with MXB7843
- ♦ +2.375V to +5.25V Single Supply
- ♦ Internal +2.5V Reference
- ♦ Direct Battery Measurement (0 to 6V)
- **♦ On-Chip Temperature Measurement**
- **♦ Touch-Pressure Measurement**
- ♦ 4-Wire Touch-Screen Interface
- **♦** Ratiometric Conversion
- ♦ SPI™/QSPI™, 3-Wire Serial Interface
- ♦ Programmable 8-/12-Bit Resolution
- ♦ Auxiliary Analog Input
- **♦ Automatic Shutdown Between Conversions**
- **♦** Low Power (External Reference) 270µA at 125ksps 115µA at 50ksps 25µA at 10ksps 5µA at 1ksps 2µA Shutdown Current

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MXB7846EEE	-40°C to +85°C	16 QSOP
MXB7846EUE	-40°C to +85°C	16 TSSOP

Pin Configuration



MIXIM

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V _{DD} , VBAT, DIN, $\overline{\text{CS}}$, DCLK to GND	0.3V to +6V
Digital Outputs to GND	
V _{REF} , X+, X-, Y+, Y-, AUX to GND	$0.3V$ to $(V_{DD} + 0.3V)$
Maximum Current into Any Pin	±50mA
Maximum ESD per IEC-61000-4-2 (per MI	L STD-883 HBM)
X+, X-, Y+, Y-, VBAT, AUX	15kV (4kV)
All Other Pins	2kV (500V)

Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
16-Pin QSOP (derate 8.30mW/°C above +70°C)	667mW
16-Pin TSSOP (derate 5.70mW/°C above +70°C)	456mW
Operating Temperature Range40°C	C to +85°C
Junction Temperature	+150°C
Storage Temperature Range65°C	
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{DD} = 2.7V \text{ to } 3.6V, V_{REF} = 2.5V, f_{DCLK} = 2MHz (50\% \text{ duty cycle}), f_{SAMPLE} = 125kHz, 12-bit mode, 0.1 \mu F capacitor at REF, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)	•		•			
Resolution					12	Bits
No Missing Codes			11	12		Bits
Relative Accuracy	INL	(Note 2)		±1	±2	LSB
Differential Nonlinearity	DNL			±1		LSB
Offset Error					±6	LSB
Gain Error		(Note 3)			±4	LSB
Noise		Including internal reference		70		μV _{RMS}
CONVERSION RATE	•					
Conversion Time	tconv	12 clock cycles (Note 4)			6	μs
Track/Hold Acquisition Time	tACQ	3 clock cycles	1.5			μs
Throughput Rate	fSAMPLE	16 clock conversion			125	kHz
Multiplexer Settling Time				500		ns
Aperture Delay				30		ns
Aperture Jitter				100		ps
Channel-to-Channel Isolation		V _{IN} = 2.5V _{P-P} at 50kHz		100		dB
Serial Clock Frequency	fDCLK		0.1		2.0	MHz
Duty Cycle			40		60	%
ANALOG INPUT (X+, X-, Y+, Y-,	AUX)		·			
Input Voltage Range			0		V _{REF}	V
Input Capacitance				25		рF
Input Leakage Current		On/off leakage, V _{IN} = 0 to V _{DD}		±0.1	±1	μΑ
SWITCH DRIVERS			•			
O. D (N 5)		Y+, X+		7		
On-Resistance (Note 5)		Y-, X-		9		Ω
INTERNAL REFERENCE	•		•			
Reference Output Voltage	V _{REF}	V _{DD} = 2.7V to 5.25V, T _A = +25°C	2.45	2.50	2.55	V
REF Output Tempco	TCV _{REF}			50		ppm°/C
REF Short-Circuit Current				18		mA
REF Output Impedance				250		Ω

2 ______ /N/XI/M

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD}=2.7V\ to\ 3.6V,\ V_{REF}=2.5V,\ f_{DCLK}=2MHz\ (50\%\ duty\ cycle),\ f_{SAMPLE}=125kHz,\ 12-bit\ mode,\ 0.1\mu F\ capacitor\ at\ REF,\ T_{A}=T_{MIN}\ to\ T_{MAX},\ unless\ otherwise\ noted.$ Typical values are at $T_{A}=+25^{\circ}C.)$

Reference input Voltage Range Note 7 1	PARAMETER	SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS	
Input Resistance	EXTERNAL REFERENCE (Interna	al reference c	lisabled, referenc	ce applied to REF)					
Input Current Input Curre	Reference Input Voltage Range		(Note 7)		1		V_{DD}	V	
SMMPLE = 12.5kHz	Input Resistance					1		GΩ	
Input Current Input Voltage Range Differential method (Note 8)			f _{SAMPLE} = 125k	кНz		13	40		
PATTERY MONITOR (BAT) Input Voltage Range During acquisition 10 Rac Raccuracy VREF = 2.5V 10 3.0 Raccuracy VREF = 2.5V Single-conversion method 0.3 Raccuracy Raccuracy VREF = 2.5V Single-conversion method 0.3 Raccuracy Raccuracy VREF VREF VREF Raccuracy Raccuracy VREF	Input Current		fSAMPLE = 12.5	kHz		2.5		μΑ	
Input Voltage Range			f _{DCLK} = 0				±3		
During acquisition 10 KΩ CREF = 2.5V	BATTERY MONITOR (BAT)								
VREF = 2.5V	Input Voltage Range				0		6	V	
Internal reference ±3 % TEMPERATURE MEASUREMENT	Input Resistance		During acquisit	ion		10		kΩ	
Internal reference	Acquirect		V _{REF} = 2.5V				±2	9/	
Differential method (Note 8) 1.6 °C Single-conversion method 0.3 °C Accuracy Differential method (Note 8) ±2 °C Single-conversion method ±3 °C Single-conversion method ±3 °C Single-conversion method ±3 °C DIGITAL INPUTS (DCLK, CS, DIN) Input High Voltage V _{IH} V _{DD} × 0.7 V Input Low Voltage V _{IL} 0.8 V Input Low Voltage V _{IH} 0.8 V Input Low Voltage V _{IH} 0.8 V Input Leakage Current In 0.8 V Input Capacitance C _{IN} 15 pF DIGITAL OUTPUT (DOUT, BUSY) Output Voltage Low V _{OL} IsiNK = 250μA V _{DD} × 0.5 V PENIRO Output Low Voltage V _{OL} SokΩ pullup to V _{DD} 0.8 V Three-State Leakage Current I _L CS = V _{DD} 1 ±10 μA Three-State Output Capacitance C _{OUT} CS = V _{DD} 15 pF POWER REQUIREMENTS External reference 2.375 5.250 V Supply Voltage V _{OL} SokΩ pullup to reference 1.5 SokΩ V Internal reference 1.5	Accuracy		Internal referen	ce			±3	70	
Single-conversion method 0.3 °C	TEMPERATURE MEASUREMENT	-							
Single-conversion method 0.3 °C Differential method (Note 8) ±2 °C Single-conversion method ±3 °C Single-conversion method (Note 8) ±2 °C Single-conversion method ±3 °C Single-conversion method (Note 8) ±2 °C Single-conversion method ±3 °C VDD Single-conversion method ±3 °C VDD VIDD	Decolution		Differential met	hod (Note 8)		1.6		°C	
Single-conversion method ±3 °C	Resolution		Single-conversi	ion method		0.3		°C	
Single-conversion method ±3 °C	Accuracy		Differential met	hod (Note 8)		±2		°C	
Input High Voltage	Accuracy		Single-conversi	ion method		±3		°C	
Input Low Voltage	DIGITAL INPUTS (DCLK, CS, DIN	l)							
Input Hysteresis	Input High Voltage	VIH			$V_{DD} \times 0.$	7		V	
Input Leakage Current	Input Low Voltage	VIL					0.8	V	
Digital Output (Dout, Busy) Digital Output (Dout, Busy) Sunk = 250μA Output Voltage Low Voltage High Voh Isource = 250μA Voltout Voltage High Voh SokΩ pullup to Vod	Input Hysteresis	VHYST				100		mV	
DIGITAL OUTPUT (DOUT, BUSY) Output Voltage Low VOL $I_{SINIK} = 250\mu A$ 0.4 V Output Voltage High VOH $I_{SOURCE} = 250\mu A$ VDD - 0.5 V PENIRQ Output Low Voltage VOL $50k\Omega$ pullup to VDD 0.8 V Three-State Leakage Current IL $\overline{CS} = VDD$ 1 ±10 μA POWER REQUIREMENTS External reference 2.375 5.250 V Internal reference 2.70 5.25 V External reference 2.375 5.250 V Fisample = 125ksps 270 650 μA Internal reference 150 μA Internal reference </td <td>Input Leakage Current</td> <td>I_{IN}</td> <td></td> <td></td> <td></td> <td></td> <td>±1</td> <td>μΑ</td>	Input Leakage Current	I _{IN}					±1	μΑ	
Output Voltage LowVolIsiNK = 250μA0.4VOutput Voltage HighVOHIsource = 250μAVDD - 0.5VPENIRQ Output Low VoltageVOL $50k\Omega$ pullup to VDD0.8VThree-State Leakage CurrentIL $\overline{CS} = VDD$ 1 ± 10 μ AThree-State Output Capacitance $COUT$ $\overline{CS} = VDD$ 15 pF POWER REQUIREMENTSSupply Voltage VDD External reference2.3755.250VInternal reference2.705.25VExternal reference2.705.25V $INTERNAL PLE = 125ksps$ 270650 $INTERNAL PLE = 125ksps$ 150 $INTERNAL PLE = 125ksps$ 780950 $INTERNAL PLE = 125ksps$ 780950 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ 720 $INTERNAL PLE = 125ksps$ $INTERNAL PLE = 125ksps$ 720 <t< td=""><td>Input Capacitance</td><td>CIN</td><td></td><td></td><td></td><td>15</td><td></td><td>рF</td></t<>	Input Capacitance	CIN				15		рF	
Output Voltage HighVOHIsource = 250μAVDD - 0.5VPENIRQ Output Low VoltageVOL $50k\Omega$ pullup to VDD0.8VThree-State Leakage CurrentIL $\overline{CS} = VDD$ 1 ± 10 μA Three-State Output Capacitance $COUT$ $\overline{CS} = VDD$ 15 pF POWER REQUIREMENTSSupply Voltage VDD $External\ reference$ 2.3755.250VInternal reference2.705.25V $External\ reference$ $fsAMPLE = 125ksps$ 270650 μA $fsAMPLE = 12.5ksps$ 220 μA $fsAMPLE = 12.5ksps$ 780950 μA $fsAMPLE = 12.5ksps$ 780950 μA $fsAMPLE = 12.5ksps$ 720 μA	DIGITAL OUTPUT (DOUT, BUSY))	•						
PENIRQ Output Low VoltageVOL50kΩ pullup to VDD0.8VThree-State Leakage CurrentIL $\overline{CS} = VDD$ 1±10μAThree-State Output Capacitance $COUT$ $\overline{CS} = VDD$ 15pFPOWER REQUIREMENTSSupply VoltageExternal reference2.3755.250VInternal reference2.705.25VExternal referencefSAMPLE = 125ksps270650μAfSAMPLE = 12.5ksps220μAfSAMPLE = 0150μAInternal referencefSAMPLE = 12.5ksps780950μAfSAMPLE = 12.5ksps720μAfSAMPLE = 12.5ksps720μAShutdown Supply CurrentISHDNDCLK = $\overline{CS} = VDD$ 3μA	Output Voltage Low	V _{OL}	I _{SINK} = 250µA				0.4	V	
Three-State Leakage Current IL $\overline{CS} = V_{DD}$ 1 ±10 μA Three-State Output Capacitance C_{OUT} $\overline{CS} = V_{DD}$ 15 pF POWER REQUIREMENTS Supply Voltage V_{DD} $External\ reference$ 2.375 5.250 V_{DD} 10 5.25 $External\ reference$ 10 5.25 $External\ reference$ 10 5.25 $External\ reference$ 10 650 $External\ reference$ 10 650 $External\ reference$ 11 ±10 $External\ reference$ 12 6.375 6.250 $External\ reference$ 12 6.375 6.250 $External\ reference$ 12 6.375 6.250 $External\ reference$ 12 6.370 6.50 $External\ reference$ 13 6.34 $External\ reference$ 15 6.34 $External\ reference$ 16 6.34 $External\ reference$ 16 6.34 $External\ reference$ 16 6.34 $External\ reference$ 17 6.34 $External\ reference$ 18 6.34 $External\ reference$ 18 6.35 $External\ reference$ 18 6.34 $External\ reference$ 18 6.34 $External\ reference$ 18 6.34 $External\ reference$ 18 6.34 $External\ reference$ 19 6.35 $External\ reference$ 19 6.36 $External\ reference$ 19 6.36 $External\ reference$ 19 6.37 $External\ reference$ 10 $External\ reference$ 10 $External\ reference$ 10 $External\ ref$	Output Voltage High	Voh	ISOURCE = 250	μA	V _{DD} - 0.5	5		V	
Three-State Output Capacitance COUT $\overline{\text{CS}} = \text{V}_{DD}$ 15 pF POWER REQUIREMENTS Supply Voltage VDD External reference 2.375 5.250 V Supply Current Internal reference 2.70 5.25 V External reference fsample = 125ksps 270 650 μA fsample = 12.5ksps 220 μΑ μΑ fsample = 12.5ksps 780 950 μΑ fsample = 12.5ksps 720 μΑ fsample = 12.5ksps 720 μΑ Shutdown Supply Current Ishdown DCLK = $\overline{\text{CS}} = \text{VDD}$ 3 μΑ	PENIRQ Output Low Voltage	V _{OL}	$50k\Omega$ pullup to	V _{DD}			0.8	V	
POWER REQUIREMENTS Supply Voltage VDD External reference 2.375 5.250 V Supply Current IDD External reference fSAMPLE = 125ksps 270 650 μA External reference fSAMPLE = 12.5ksps 220 μA fSAMPLE = 0 150 150 150 fSAMPLE = 12.5ksps 780 950 μA fSAMPLE = 12.5ksps 720 μA fSAMPLE = 12.5ksps 720 μA Shutdown Supply Current ISHDN DCLK = CS = VDD 3 μA	Three-State Leakage Current	ΙL	$\overline{\text{CS}} = V_{\text{DD}}$			1	±10	μΑ	
Supply Voltage External reference 2.375 5.250 V Internal reference 2.70 5.25 V External reference fSAMPLE = 125ksps 270 650 4 fSAMPLE = 12.5ksps 220 μΑ μΑ Supply Current Internal reference fSAMPLE = 12.5ksps 780 950 4 fSAMPLE = 12.5ksps 720 μΑ 4 5 Shutdown Supply Current ISHDN DCLK = CS = VDD 3 μΑ	Three-State Output Capacitance	Cout	$\overline{\text{CS}} = V_{\text{DD}}$			15		рF	
Supply Voltage VDD Internal reference 2.70 5.25 V Supply Current External reference fSAMPLE = 125ksps 270 650 μA fSAMPLE = 12.5ksps 220 μA μA fSAMPLE = 125ksps 780 950 μA Internal reference fSAMPLE = 12.5ksps 720 μA μA Shutdown Supply Current ISHDN DCLK = CS = VDD 3 μA	POWER REQUIREMENTS								
Internal reference 2.70 5.25	Cupply Voltage	\/==	External referer	nce	2.375		5.250	\/	
External reference External reference fSAMPLE = 12.5ksps 220 μA Supply Current IDD fSAMPLE = 12.5ksps 780 950 Internal reference fSAMPLE = 12.5ksps 720 μA Shutdown Supply Current ISHDN DCLK = CS = VDD 3 μA	Supply voltage	VDD	Internal referen	се	2.70		5.25	T v	
Supply Current $IDD = \begin{bmatrix} ISAMPLE = 12.5ksps & 220 & \mu A \\ ISAMPLE = 0 & 150 & 150 \\ Internal reference & ISAMPLE = 125ksps & 780 & 950 \\ \hline ISAMPLE = 12.5ksps & 780 & 950 \\ \hline ISAMPLE = 12.5ksps & 720 & \mu A \\ \hline ISAMPLE = 0 & 650 & 3 & \mu A \end{bmatrix}$ Shutdown Supply Current $ISHDN = \begin{bmatrix} ISAMPLE = 12.5ksps & 780 & 950 \\ ISAMPLE = 0 & 650 & 3 & \mu A \\ \hline ISAMPLE = 0 & 3 $				fsample = 125ksps		270	650		
				f _{SAMPLE} = 12.5ksps		220		μΑ	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Supply Current	loo	Telefelice			150		1	
		IDD		f _{SAMPLE} = 125ksps		780	950		
				f _{SAMPLE} = 12.5ksps		720		μΑ	
			Telefelice	fsample = 0		650			
	Shutdown Supply Current	ISHDN					3	μΑ	
	Power-Supply Rejection Ratio		$V_{DD} = 2.7V \text{ to } 3$	3.6V full scale		70		dB	



TIMING CHARACTERISTICS (Figure 1)

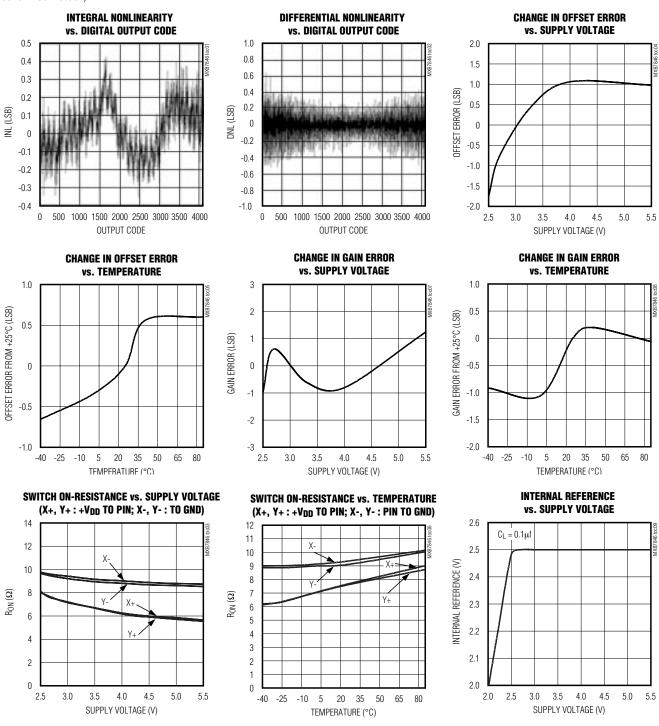
 $(V_{DD}=2.7V\ to\ 3.6V,\ V_{REF}=2.5V,\ f_{DCLK}=2MHz\ (50\%\ duty\ cycle),\ f_{SAMPLE}=125kHz,\ 12-bit\ mode,\ 0.1\mu F$ capacitor at REF, $T_A=T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A=+25^{\circ}C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Fig	ure 1)		•			•
Acquisition Time	tACQ		1.5			μs
DCLK Clock Period	tcp		500			ns
DCLK Pulse Width High	tch		200			ns
DCLK Pulse Width Low	tCL		200			ns
DIN-to-DCLK Setup Time	tDS		100			ns
DIN-to-DCLK Hold Time	t _{DH}		0			ns
CS Fall-to-DCLK Rise Setup Time	tcss		100			ns
CS Rise-to-DCLK Rise Ignore	tcsh		0			ns
DCLK Falling-to-DOUT Valid	t _{DO}	C _{LOAD} = 50pF			200	ns
CS Rise-to-DOUT Disable	t _{TR}	C _{LOAD} = 50pF			200	ns
CS Fall-to-DOUT Enable	t _{DV}	C _{LOAD} = 50pF			200	ns
DCLK Falling-to-BUSY Rising	t _{BD}				200	ns
CS Falling-to-BUSY Enable	t _{BDV}				200	ns
CS Rise-to-BUSY Disable	tBTR				200	ns

- **Note 1:** Tested at $V_{DD} = 2.7V$.
- **Note 2:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
- Note 3: Offset nulled.
- Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
- Note 5: Resistance measured from the source to drain of the switch.
- Note 6: External load should not change during conversion for specified accuracy.
- Note 7: ADC performance is limited by the conversion noise floor, typically 300µVp.p. An external reference below 2.5V can compromise the ADC performance.
- Note 8: Difference between Temp0 and Temp1. No calibration necessary.

Typical Operating Characteristics

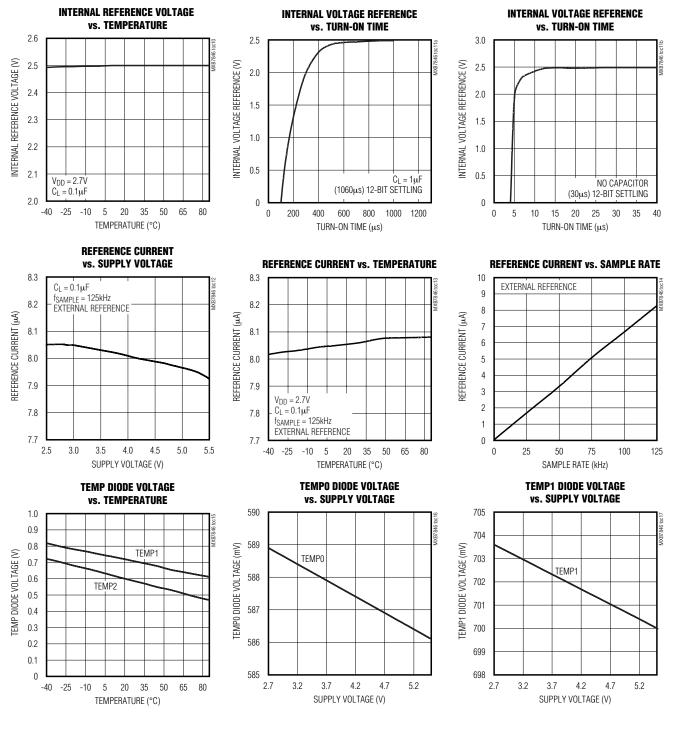
 $(V_{DD} = 2.7V, V_{REF} = 2.5V_{EXTERNAL}, f_{DCLK} = 2MHz, f_{SAMPLE} = 125kHz, C_{LOAD} = 50pF, 0.1\mu F capacitor at REF, T_A = +25^{\circ}C, unless otherwise noted.)$



NIXIN

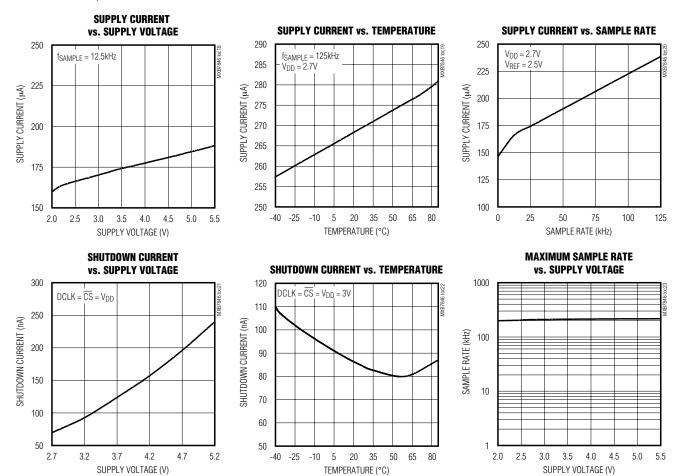
Typical Operating Characteristics (continued)

 $(V_{DD} = 2.7V, V_{REF} = 2.5V_{EXTERNAL}, f_{DCLK} = 2MHz, f_{SAMPLE} = 125kHz, C_{LOAD} = 50pF, 0.1\mu F capacitor at REF, T_A = +25^{\circ}C, unless otherwise noted.)$



Typical Operating Characteristics (continued)

 $(V_{DD} = 2.7V, V_{REF} = 2.5V_{EXTERNAL}, f_{DCLK} = 2MHz, f_{SAMPLE} = 125kHz, C_{LOAD} = 50pF, 0.1\mu F capacitor at REF, T_A = +25°C, unless otherwise noted.)$



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage. Connect to pin 10.
2	X+	X+ Position Input, ADC Input Channel 1
3	Y+	Y+ Position Input, ADC Input Channel 2
4	X-	X- Position Input
5	Y-	Y- Position Input
6	GND	Ground
7	BAT	Battery Monitoring Inputs; ADC Input Channel 3
8	AUX	Auxiliary Input to ADC; ADC Input Channel 4
9	REF	Voltage Reference Output/Input. Reference voltage for analog-to-digital conversion. In internal reference mode, the reference buffer provides a 2.50V nominal output. In external reference mode, apply a reference voltage between 1V and V _{DD} . Bypass REF to GND with a 0.1µF capacitor.
10	V _{DD}	Positive Supply Voltage, +2.375V (2.70V) to +5.25V. External (internal) reference. Bypass with a 1µF capacitor. Connect to pin 1.
11	PENIRQ	Pen Interrupt Output. Open anode output. $10k\Omega$ to $100k\Omega$ pullup resistor required to V_{DD} .
12	DOUT	Serial Data Output. Data changes state on the falling edge of DCLK. High impedance when $\overline{\text{CS}}$ is HIGH.
13	BUSY	Busy Output. BUSY pulses high for one clock period before the MSB decision. High impedance when $\overline{\text{CS}}$ is HIGH.
14	DIN	Serial Data Input. Data clocked in on the rising edge of DCLK.
15	CS	Active-Low Chip Select. Data is only clocked into DIN when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is HIGH, DOUT and BUSY are high impedance.
16	DCLK	Serial Clock Input. Clocks data in and out of the serial interface and sets the conversion speed (duty cycle must be 40% to 60%).

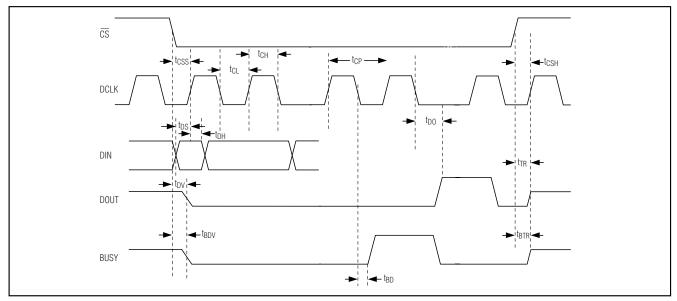


Figure 1. Detailed Serial Interface Timing

3 ______*NIXI/*N

Detailed Description

The MXB7846 uses a successive-approximation conversion technique to convert analog signals to a 12-bit digital output. An SPI/QSPI/MICROWIRE™-compatible serial interface provides easy communication to a microprocessor (µP). It features an internal 2.5V reference, an on-chip temperature sensor, a battery monitor, and a 4-wire touch-screen interface (*Functional Diagram*).

Analog Inputs

Figure 2 shows a block diagram of the analog input section that includes the input multiplexer of the MXB7846, the differential signal inputs of the ADC, and the differential reference inputs of the ADC. The input multiplexer switches between X+, X-, Y+, Y-, AUX, BAT, and the internal temperature sensor.

In single-ended mode, conversions are performed using REF as the reference. In differential mode, ratiometric conversions are performed with REF+ connected to X+ or Y+, and REF- connected to X- or Y-. Configure the reference and switching matrix according to Tables 1 and 2.

During the acquisition interval, the selected channel charges the sampling capacitance. The acquisition interval starts on the fifth falling clock edge and ends on the eighth falling clock edge.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time (tacq) is the maximum time the device takes to acquire the input signal to 12-bit accuracy. Calculate tacq with the following equation:

$$t_{ACQ} = 8.4 \times (R_S + R_{IN}) \times 25pF$$

where $R_{IN} = 2k\Omega$ and Rs is the source impedance of the input signal.

Source impedances below $1k\Omega$ do not significantly affect the ADC's performance. Accommodate higher source impedances by either slowing down DCLK or by placing a $1\mu\text{F}$ capacitor between the analog input and GND.

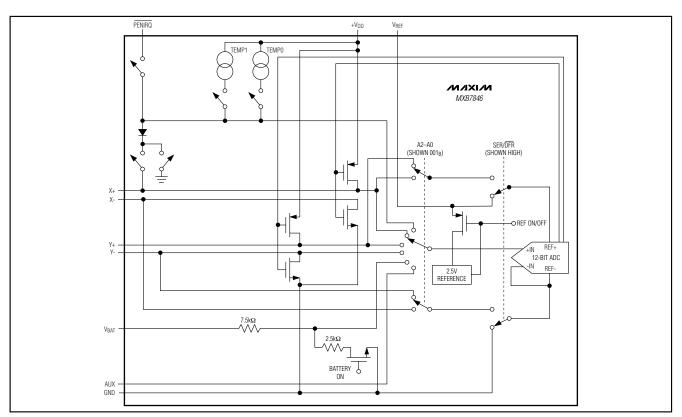


Figure 2. Equivalent Input Circuit

MICROWIRE is a trademark of National Semiconductor Corp.



Functional Diagram

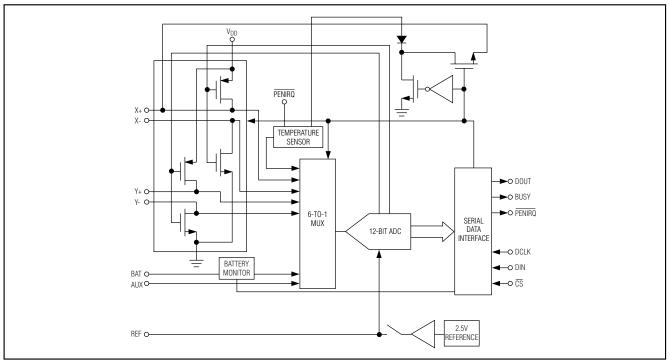


Table 1. Input Configuration, Single-Ended Reference Mode (SER/DFR HIGH)

A2	A1	A0	MEASUREMENT	ADC INPUT CONNECTION	DRIVERS ON
0	0	0	Temp0	Temp0	_
0	0	1	Y position	X+	Y+, Y-
0	1	0	ВАТ	BAT	_
0	1	1	Z1	X+	X-, Y+
1	0	0	Z2	Y-	X-, Y+
1	0	1	X- position	Y+	X-, X+
1	1	0	AUX	AUX	_
1	1	1	Temp1	Temp1	_

Table 2. Input Configuration, Differential Reference Mode (SER/DFR LOW)

A2	A1	A0	ADC +REF CONNECTION TO	ADC -REF CONNECTION TO	ADC INPUT CONNECTION TO	MEASUREMENT PERFORMED	DRIVER ON
0	0	1	Y+	Y-	X+	Y position	Y+, Y-
0	1	1	Y+	Y-	X+	Z1 position	Y+, X-
0	1	0	X+	X-	Y-	Z2 position	Y+, X-
1	0	1	X+	X-	Y+	X position	X+, X-

Input Bandwidth and Anti-Aliasing

The ADCs input tracking circuitry has a 25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the analog input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. Analog inputs must not exceed V_{DD} by more than 50mV or be lower than GND by more than 50mV for accurate conversion. If an off-channel analog input voltage exceeds the supplies, limit the input current to 50mA. The analog input pins are ESD protected to ± 8 kV using the Contact Discharge method and ± 15 kV using the Air-Gap method specified in IEC 61000-4-2.

Touch-Screen Conversion

The MXB7846 provides two conversion methods—differential and single ended. The SER/DFR bit in the control word selects either mode. A logic 1 selects a single-ended conversion, while a logic 0 selects a differential conversion.

Differential vs. Single Ended

Changes in operating conditions can degrade the accuracy and repeatability of touch-screen measurements. Therefore, the conversion results representing X and Y coordinates may be incorrect. For example, in single-ended measurement mode, variation in the touch-screen driver voltage drops results in incorrect input reading. Differential mode minimizes these errors.

Single-Ended Mode

Figure 3 shows the switching matrix configuration for Y-coordinate measurement in single-ended mode. The MXB7846 measures the position of the pointing device by connecting X+ to IN+ of the ADC, enabling Y+ and Y- drivers, and digitizing the voltage on X+. The ADC performs a conversion with REF+ = REF and REF- = GND. In single-ended measurement mode, the bias to the touch screen can be turned off after the acquisition to save power. The on-resistance of the X and Y drivers results in a gain error in single-ended measurement mode. Touch-screen resistance ranges from 200Ω to 900Ω (depending on the manufacturer), whereas the on-resistance of the X and Y drivers is 8Ω (typ). Limit the touch-screen current to less than 50mA by using a touch screen with a resistance higher than 100Ω . The

resistive-divider created by the touch screen and the on-resistance of the X and Y drivers result in both an offset and a gain shift. Also, the on-resistance of the X and Y drivers does not track the resistance of the touch screen over temperature and supply. This results in further measurement errors.

Differential Measurement Mode

Figure 4 shows the switching matrix configuration for Y-coordinate measurement. The REF+ and REF- inputs are connected directly to the Y+ and Y- pins, respectively. Differential mode uses the voltage at the Y+ pin as the REF+ voltage and voltage at the Y- pin as REF-voltage. This conversion is ratiometric and independent of the voltage drop across the drivers and variation in the touch-screen resistance. In differential mode, the touch screen remains biased during the acquisition and conversion process. This results in additional supply current and power dissipation during conversion when compared to the absolute measurement mode.

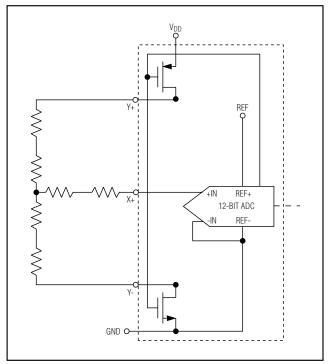
PEN Interrupt Request (PENIRQ)

Figure 5 shows the block diagram for the $\overline{\text{PENIRQ}}$ function. When used, $\overline{\text{PENIRQ}}$ requires a $10\text{k}\Omega$ to $100\text{k}\Omega$ pullup to $+\text{V}_{DD}$. If enabled, $\overline{\text{PENIRQ}}$ goes low whenever the touch screen is touched. The $\overline{\text{PENIRQ}}$ output can be used to initiate an interrupt to the microprocessor, which can write a control word to the MXB7846 to start a conversion.

Figure 6 shows the timing diagram for the PENIRQ pin function. The diagram shows that once the screen is touched while \overline{CS} is high, the PENIRQ output goes low after a time period indicated by tTOUCH. The tTOUCH value changes for different touch-screen parasitic capacitance and resistance. The microprocessor receives this interrupt and pulls \overline{CS} low to initiate a conversion. At this instant, the \overline{PENIRQ} pin should be masked, as transitions can occur due to a selected input channel or the conversion mode. The \overline{PENIRQ} pin functionality becomes valid when either the last data bit is clocked out, or \overline{CS} is pulled high.

Touch-Pressure Measurement

The MXB7846 provides two methods for measuring the pressure applied to the touch screen (Figure 7). By measuring R_{TOUCH}, it is possible to differentiate between a finger or stylus in contact with the touch screen. Although 8-bit resolution is typically sufficient, the following calculations use 12-bit resolution demonstrating the maximum precision of the MXB7846.



Y+

HIN REF+

12-BIT ADC

IN REF-

Figure 3. Single-Ended Y-Coordinate Measurement

Figure 4. Ratiometric Y-Coordinate Measurement

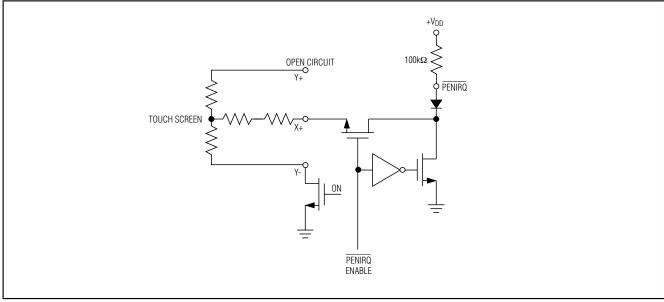


Figure 5. PENIRQ Functional Block Diagram

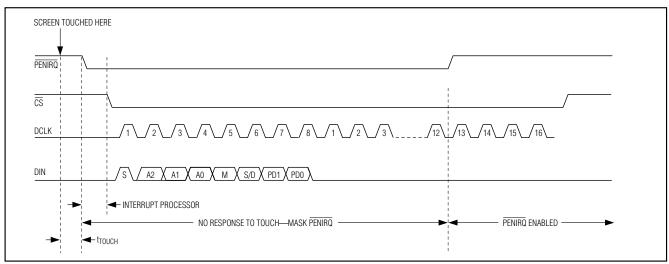


Figure 6. PENIRQ Timing Diagram

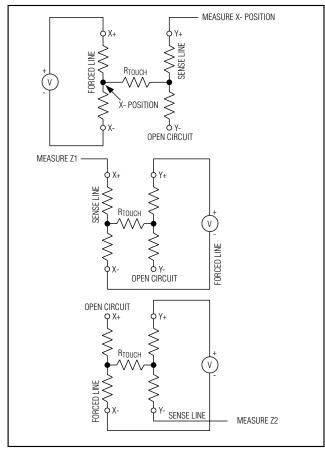


Figure 7. Pressure Measurement Block Diagram

The first method performs pressure measurements using a known X-plate resistance. After completing three conversions (X-position, Z1, and Z2), use the following equation to calculate RTOUCH:

$$R_{TOUCH} = (R_{XPLATE}) \times \left(\frac{X_{POSITION}}{4096}\right) \times \left[\left(\frac{Z_2}{Z_1}\right) - 1\right]$$

The second method requires knowing both the X-plate and Y-plate resistance. Three conversions are required in this method: the X-position, Y-position, and Z1-position. Use the following equation to calculate RTOUCH:

$$R_{TOUCH} = \left\{ \left(\frac{R_{XPLATE}}{Z_1} \right) \times \left(\frac{X_{POSITION}}{4096} \right) \times \left[\left(\frac{4096}{Z_1} \right) - 1 \right] \right.$$
$$\left. - \left\{ R_{YPLATE} \times \left(\frac{Y_{POSITION}}{4096} \right) \right\}$$

Internal Temperature Sensor

The MXB7846 provides two temperature measurement options: single-ended conversion and differential conversion. Both temperature measurement techniques rely on the semiconductor junction's temperature characteristics. The forward diode voltage (VBE) vs. temperature is a well-defined characteristic. The ambient temperature can be calculated by knowing the value of VBE at a fixed temperature and then monitoring the change in that voltage as the temperature changes. The single conversion method requires calibration at a known temperature, but only needs a single reading to calculate the ambient temperature. First, the PENIRQ diode for-

ward bias voltage is measured by the ADC with an address of A2 = 0, A1 = 0, and A0 = 0 at a known temperature. Subsequent diode measurements provide an estimate of the ambient temperature through extrapolation. This assumes a temperature coefficient of -2.1mV/°C. The single conversion method results in a resolution of 0.3°C/LSB and a typical accuracy of ±3°C.

The differential conversion method uses two measurement points. The first measurement ($\underline{\text{Temp0}}$) is performed with a fixed bias current into the $\underline{\text{PENIRQ}}$ diode. The second measurement ($\underline{\text{Temp1}}$) is performed with a fixed multiple of the original bias current with an address of A2 = 1, A1 = 1, and A0 = 1. The voltage difference between the first and second conversion is proportional to the absolute temperature and is expressed by the following formula:

$$T(^{\circ}C) = \left[2.60 \times (T1 - T0) \left(\frac{VREF}{4096}\right) \times 1000\right] - 273$$

where T0 (Temp0) and T1 (Temp1) are the conversion results.

This differential conversion method can provide much improved absolute temperature measurement; however, the resolution is reduced to 1.6°C/LSB.

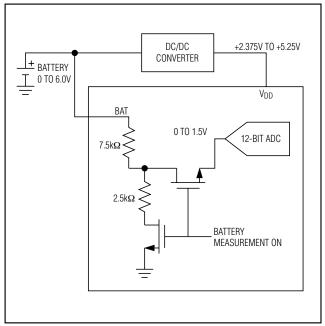


Figure 8. Battery Measurement Functional Block Diagram

Battery Voltage Monitor

A dedicated analog input (BAT) allows the MXB7846 to monitor the system battery voltage. Figure 8 shows the battery voltage monitoring circuitry. The MXB7846 monitors battery voltages from 0 to 6V. An internal resistor network divides down VBAT by 4 so that a 6.0V battery voltage results in 1.5V at the ADC input. To minimize power consumption, the divider is only enabled during the sampling of VBAT.

Internal Reference

Enable the internal 2.5V reference by setting PD1 in the control byte to a logic 1 (see Tables 3 and 4). The MXB7846 uses the internal reference for single-ended measurement mode, battery monitoring, temperature measurement, and for measurement on the auxiliary input. To minimize power consumption, disable the internal reference by setting PD1 to a logic 0 when performing ratiometric position measurements. The internal 2.5V reference typically requires 10ms to settle (with no external load). For optimum performance, connect a 0.1µF capacitor from REF to GND. This internal reference can be overdriven with an external reference. For best performance. the internal reference should be disabled when the external reference is applied. The internal reference of the MXB7846 must also be disabled to maintain compatibility with the MXB7843. To disable the internal reference of the MXB7846 after power-up, a control byte with PD1 = 0 is required. (See Typical Operating Characteristics for power-up time of the reference from power down.)

External Reference

Although the internal reference may be overdriven with an external reference, the internal reference should be disabled (PD1 = 0) for best performance when using an external reference. During conversion, an external reference at REF must deliver up to $40\mu A$ DC load current. If the reference has a higher output impedance or is noisy, bypass it close to the REF pin with a $0.1\mu F$ and a $4.7\mu F$ capacitor. Temperature measurements are always performed using the internal reference.

Digital Interface

Initialization After Power-Up and Starting a Conversion

The digital interface consists of three inputs, DIN, DCLK, $\overline{\text{CS}}$, and one output, DOUT. A logic-high on $\overline{\text{CS}}$ disables the MXB7846 digital interface and places DOUT in a high-impedance state. Pulling $\overline{\text{CS}}$ low enables the MXB7846 digital interface.

Table 3. Control Byte Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
START	A2	A1	A0	MODE	SER/DFR	PD1	PD0		
BIT	BIT NAME DESCRIPTION								
7	START	Start bit							
6	A2								
5	A1	Address (Tab	Address (Tables 1 and 2)						
4	A0								
3	MODE	Conversion re	onversion resolution: 1 = 8 bits, 0 = 12 bits						
2	SER/DFR	Conversion m	Conversion mode: 1 = single ended, 0 = differential						
1	PD1	Davier davis s	(Table 4)						
0	PD0	Power-down r	Power-down mode (Table 4)						

Start a conversion by clocking a control byte into DIN (Table 3) with $\overline{\text{CS}}$ low. Each rising edge on DCLK clocks a bit from DIN into the MXB7846's internal shift register. After $\overline{\text{CS}}$ falls, the first arriving logic 1 bit defines the control byte's START bit. Until the START bit arrives, any number of logic 0 bits can be clocked into DIN with no effect.

The MXB7846 is compatible with SPI/QSPI/MICROWIRE devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers of the microcontroller: set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI all transmit a byte and receive a byte at the same time. The simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to read the conversion result; Figure 9).

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 500kHz to 2MHz:

- 1) Set up the control byte and call it TB. TB should be in the format: 1XXXXXXX binary, where X denotes the particular channel, selected conversion mode, and power mode (Tables 3, 4).
- Use a general-purpose I/O line on the CPU to pull CS low.
- Transmit TB and simultaneously receive a byte; call it RB1.
- 4) Transmit a byte of all zeros (\$00 hex) and simultaneously receive byte RB2.
- Transmit a byte of all zeros (\$00 hex) and simultaneously receive byte RB3.
- 6) Pull CS high.

Figure 9 shows the timing for this sequence. Byte RB2 and RB3 contain the result of the conversion, padded with four trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle timing between 8-bit transfers.

Digital Output

The MXB7846 outputs data in straight binary format. Data is clocked out on the falling edge of the DCLK MSB first.

Serial Clock

The external clock not only shifts data in and out, but it also drives the analog-to-digital conversion steps. BUSY pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 DCLK falling edges. BUSY and DOUT go into a high-impedance state when $\overline{\text{CS}}$ goes high.

The conversion must complete in 500µs or less; if not, droop on the sample-and-hold capacitors can degrade conversion results.

Data Framing

The falling edge of $\overline{\text{CS}}$ does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on DCLK's falling edge, after the eighth bit of the control byte is clocked into DIN.

The first logic 1 clocked into DIN after bit 6 of a conversion in progress is clocked onto the DOUT pin and is treated as a START bit (Figure 10).

Once a start bit has been recognized, the current conversion must be completed.

Table 4. Power-Mode Selection

				SUPPLY CURRENT (typ) (μA)		
PD1	PD0	PENIRQ	STATUS	DURING CONVERSION	AFTER CONVERSION	
0	0	Enabled	ADC is ON during conversion, OFF between conversion	200	1	
0	1	Disabled	ADC is always ON, reference is always OFF	200	200	
1	0	Disabled	ADC is always OFF, reference is always ON	400	400	
1	1	Disabled	ADC is always ON, reference is always ON	600	600	

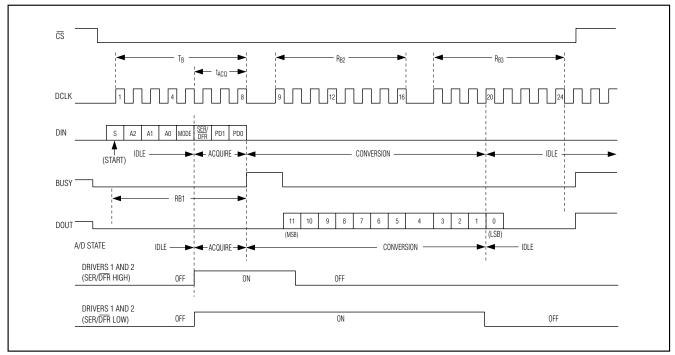


Figure 9. Conversion Timing, 24-Clock per Conversion, 8-Bit Bus Interface

The fastest the MXB7846 can run with $\overline{\text{CS}}$ held continuously low is 15 clock conversions. Figure 10 shows the serial-interface timing necessary to perform a conversion every 15 DCLK cycles. If $\overline{\text{CS}}$ is connected low and DCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (μ Cs) require that data transfers occur in multiples of eight DCLK cycles; 16 clocks per conversion is typically the fastest that a μ C can drive the MXB7846. Figure 11 shows the serial interface timing necessary to perform a conversion every 16 DCLK cycles.

8-Bit Conversion

The MXB7846 provides an 8-bit conversion mode selected by setting the MODE bit in the control byte high. In the 8-bit mode, conversions complete four clock cycles earlier than in the 12-bit output mode, resulting in 25% faster throughput. This can be used in conjunction with serial interfaces that provide 12-bit transfers, or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by 4 bits, but each conversion can also occur at a faster clock rate since settling to better than 8 bits is all that is required. The clock rate can be as much as 25% faster. The faster clock rate and fewer clock cycles combine to increase the conversion rate.

Data Format

The MXB7846 output data is in straight binary format as shown in Figure 12. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

_Applications Information

Basic Operation of the MXB7846

The 4-wire touch-screen controller works by creating a voltage gradient across the vertical or horizontal resistive network connected to the MXB7846, as shown in the *Typical Application Circuit*. The touch screen is biased through internal MOSFET switches that connect each resistive layer to V_{DD} and ground on an alternate basis. For example, to measure the Y position when a pointing device presses on the touch screen, the Y+

and Y- drivers are turned on, connecting one side of the vertical resistive layer to V_{DD} and the other side to ground. In this case, the horizontal resistive layer functions as a sense line. One side of this resistive layer gets connected to the X+ input, while the other side is left open or floating. The point where the touch screen is pressed brings the two resistive layers in contact and forms a voltage-divider at that point. The data converter senses the voltage at the point of contact through the X+ input and digitizes it. The horizontal layer resistance does not introduce any error in the conversion because no DC current is drawn.

The conversion process of the analog input voltage to digital output is controlled through the serial interface between the A/D converter and the μ P. The processor controls the MXB7846 configuration through a control byte (see Tables 3 and 4). Once the processor instructs

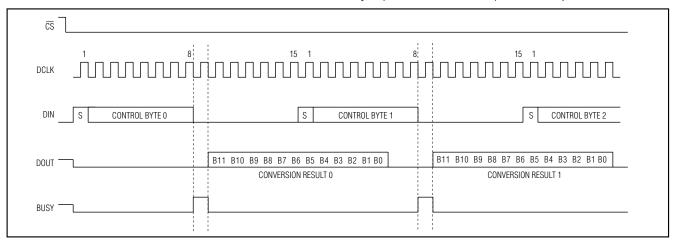


Figure 10. 15-Clock/Conversion Timing

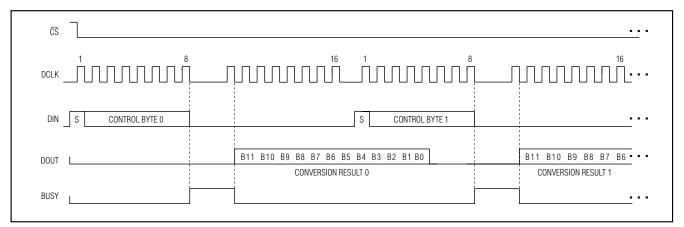


Figure 11. 16-Clock/Conversion Timing



the MXB7846 to initiate a conversion, the MXB7846 biases the touch screen through the internal switches at the beginning of the acquisition period. The voltage transient at the touch screen needs to settle down to a stable voltage before the acquisition period is over. After the acquisition period is over, the A/D converter goes into a conversion period with all internal switches turned off if the device is in single-ended mode. If the device is in differential mode, the internal switches remain on from the start of the acquisition period to the end of the conversion period.

Power-On Reset

When power is first applied, internal power-on circuitry resets the MXB7846. Allow 10µs for the first conversion after the power supplies stabilize. If \overline{CS} is low, the first logic 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. On power-up, allow time for the reference to stabilize.

Power Modes

Save power by placing the converter in one of two lowcurrent operating modes or in full power down between conversions. Select the power-down mode through PD1 and PD0 of the control byte (Tables 3 and 4).

The software power-down modes take effect after the conversion is completed. The serial interface remains active while waiting for a new control byte to start a conversion and switches to full-power mode. After completing its conversion, the MXB7846 enters the programmed power mode until a new control byte is received.

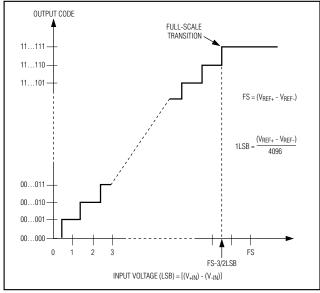


Figure 12. Ideal Input Voltages and Output Codes

The power-up wait before conversion period is dependent on the power-down state. When exiting software low-power modes, conversion can start immediately when running at decreased clock rates. Upon power-on reset, the MXB7846 is in power-down mode with PD1 = 0 and PD0 = 0. When exiting software shutdown, the MXB7846 is ready to perform a conversion in 10µs with an external reference. When using the internal reference, allow enough time for reference to settle to 12-bit accuracy when exiting full power-down mode, as shown in the *Typical Operating Characteristics*.

PD1 = 1, PD0 = 1

In this mode, the MXB7846 is always powered up and both the reference and the ADC are always on. The device remains fully powered after the current conversion completes.

PD1 = 0, PD0 = 0

In this mode, the MXB7846 powers down after the current conversion completes or on the next rising edge of \overline{CS} , whichever occurs first. The next control byte received on DIN powers up the MXB7846. At the start of a new conversion, it instantly powers up. When each conversion is finished, the part enters power-down mode, unless otherwise indicated. The first conversion after the ADC returns to full power is valid for differential conversions and single-ended measurement conversions when using an external reference.

When operating at full speed and 16 clocks per conversion, the difference in power consumption between PD1 = 0, PD0 = 1, and PD1 = 0, PD0 = 0 is negligible. Also, in the case where the conversion rate is decreased by slowing the frequency of the DCLK input, the power consumption between these two modes is not very different. When the DCLK frequency is kept at the maximum rate during a conversion, conversions are done less often. There is a significant difference in power consumption between these two modes.

PD1 = 1, PD0 = 0

In this mode, the MXB7846 is powered down. This mode becomes active after the current conversion completes or on the next rising edge of $\overline{\text{CS}}$, whichever occurs first. The next command byte received on the DIN returns the MXB7846 to full power. The first conversion after the ADC returns to full power is valid.

PD1 = 0, PD0 = 1

This mode turns the internal reference off and leaves the ADC on to perform conversions using an external reference.

Hardware Power-Down

 $\overline{\text{CS}}$ also places the MXB7846 into power-down. When $\overline{\text{CS}}$ goes HIGH, the MXB7846 immediately powers down and aborts the current conversion. The internal reference does not turn off when $\overline{\text{CS}}$ goes high. To disable the internal reference, an additional command byte is required before $\overline{\text{CS}}$ goes high (PD1 = 0). Set PD1 = 0 before $\overline{\text{CS}}$ goes high.

Touch-Screen Settling

There are two key touch-screen characteristics that can degrade accuracy. First, the parasitic capacitance between the top and bottom layers of the touch screen can result in electrical ringing. Second, vibration of the top layer of the touch screen can cause mechanical contact bouncing.

External filter capacitors may be required across the touch screen to filter noise induced by the LCD panel or backlight circuitry, etc. These capacitors lengthen the settling time required when the panel is touched and can result in a gain error, as the input signal may not settle to its final steady-state value before the ADC samples the inputs. Two methods to minimize or eliminate this issue are described below.

One option is to lengthen the acquisition time by stopping or slowing down DCLK, allowing for the required touch-screen settling time. This method solves the settling time problem for both single-ended and differential modes.

The second option is to operate the MXB7846 in the differential mode only for the touch screen, and perform additional conversions with the same address until the input signal settles. The MXB7846 can then be placed in the power-down state on the last measurement.

Connection to Standard Interface *MICROWIRE Interface*

When using the MICROWIRE- (Figure 13) or SPI-compatible interface (Figure 14), set the CPOL = CPHA = 0. Two consecutive 8-bit readings are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions occur on the serial clock's falling edge and are clocked into the μP on the DCLK's rising edge. The first 8-bit data stream contains the first 8 bits of the current conversion, starting with the MSB. The second 8-bit data stream contains the remaining 4 result bits followed by 4 trailing zeros. DOUT then goes high impedance when $\overline{\text{CS}}$ goes high.

QSPI/SPI Interface

The MXB7846 can be used with the QSPI/SPI interface using the circuit in Figure 14 with CPOL = 0 and CPHA = 0. This interface can be programmed to do a conversion on any analog input of the MXB7846.

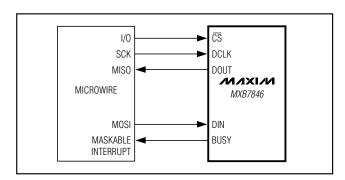


Figure 13. MICROWIRE Interface

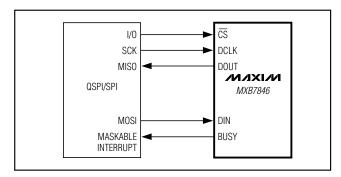


Figure 14. QSPI/SPI Interface

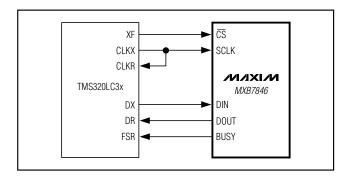


Figure 15. TMS320 Serial Interface

TMS320LC3x Interface

Figure 15 shows an example circuit to interface the MXB7846 to the TMS320. The timing diagram for this interface circuit is shown in Figure 16.

Use the following steps to initiate a conversion in the MXB7846 and to read the results:

The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are connected to the MXB7846 DCLK input.



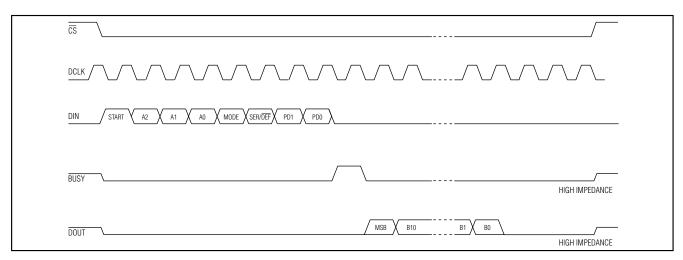


Figure 16. MXB7846-to-TMS320 Serial Interface Timing Diagram

- 2) The MXB7846's $\overline{\text{CS}}$ pin is driven low by the TMS320's XF I/O port to enable data to be clocked into the MXB7846's DIN pin.
- 3) An 8-bit word (1XXXXXXX) should be written to the MXB7846 to initiate a conversion and place the device into normal operating mode. See Table 3 to select the proper XXXXXXXX bit values for your specific applications.
- 4) The MXB7846's BUSY output is monitored through the TMS320's FSR input. A falling edge on the BUSY output indicates that the conversion is in progress and data is ready to be received from the device.
- 5) The TMS320 reads in 1 data bit on each of the next 16 rising edges of DCLK. These bits represent the 12-bit conversion result followed by 4 trailing bits.
- 6) Pull $\overline{\text{CS}}$ high to disable the MXB7846 until the next conversion is initiated.

Layout, Grounding, and Bypassing

For best performance, use printed circuit (PC) boards with good layouts; wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Establish a single-point analog ground (star ground point) at GND. Connect all analog grounds to the star ground. Connect the digital system ground to the star ground at this point only. For lowest noise operation, minimize the length of the ground return to the star ground's power supply.

Power-supply decoupling is also crucial for optimal device performance. A good way to decouple analog supplies is to place a 10µF tantalum capacitor in parallel with a 0.1µF capacitor bypassed to GND. To maximize performance, place these capacitors as close as possible to the supply pin of the device. Minimize capacitor lead length for best supply-noise rejection. If the supply is very noisy, a 10Ω resistor can be connected in series as a lowpass filter.

While using the MXB7846, the interconnection between the converter and the touch screen should be as short as possible. Since touch screens have low resistance, longer or loose connections may introduce error. Noise can also be a major source of error in touch-screen applications (e.g., applications that require a backlight LCD panel). EMI noise coupled through the LCD panel to the touch screen may cause flickering of the converted data. Utilizing a touch screen with a bottom-side metal layer connected to ground decouples the noise to ground. In addition, the filter capacitors from Y+, Y-, X+, and X- inputs to ground also help further reduce the noise. Caution should be observed for settling time of the touch screen, especially operating in the single-ended measurement mode and at high data rates.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MXB7846 are measured using the end-point method.

20 _______ /N/XI/VI

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

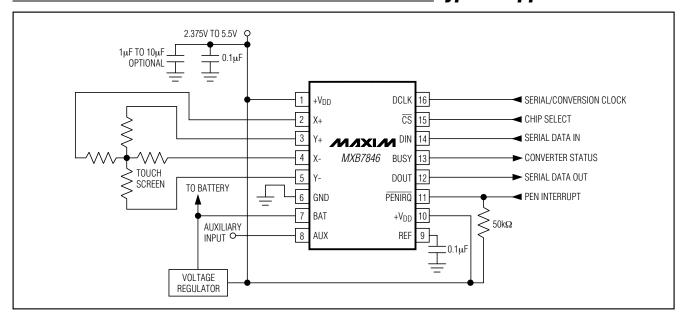
Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken.

Chip Information

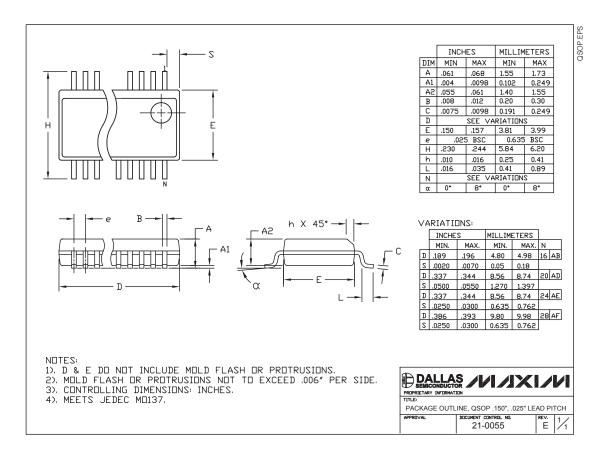
TRANSISTOR COUNT: 12,000 PROCESS: 0.6µm BiCMOS

Typical Application Circuit



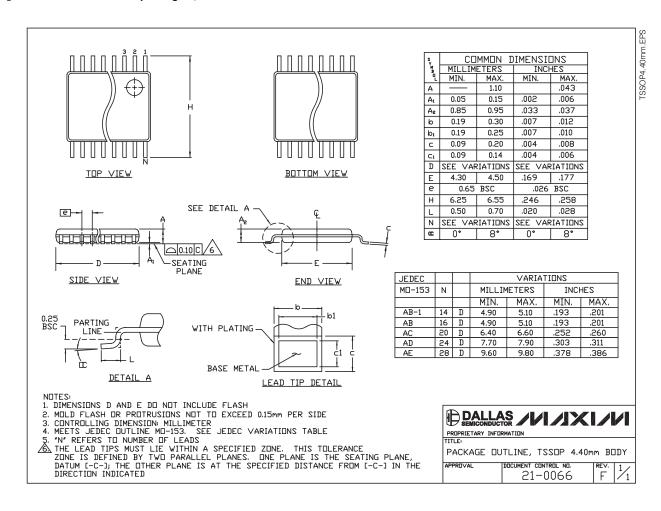
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600