RoHS

Touch Pad Controller

The MPR081 is a user interface controller which manages a 16-position rotary touch pad. The MPR081 uses an I^2C interface to communicate with the host, which configures the operation, and an interrupt to advise the host of status changes.

The interrupt output, $\overline{IRQ}$, indicates that rotary status has changed since the MPR081 was last read. The maximum interrupt frequency can be limited to sacrifice system response time in favor of power consumption for systems that wake up out of sleep to respond to interrupts.

Features

- 1.8 V to 3.6 V operation
- 150 µA average supply current (all touch pads being monitored)
- 1 µA standby current
- Supports a 16-position rotary interface
- Proprietary false touch rejection technology
- Ongoing pad analysis and detection not reset by EMI events
- Rotary data changes are delivered from a FIFO for shortest access time
- $\overline{IRQ}$ output advises when FIFO has data
- System can set interrupt behavior as immediate after event, or program a minimum time between successive interrupts
- Current rotary position is always available on demand for polling-based systems
- Sounder drive provides audible feedback to simulate mechanical key clicks
- Digital output (I^2C with custom addressing)
- 16-pin QFN and TSSOP packages
- -40°C to +85°C operating temperature range

Implementations

- Control Panels
- Switch Replacements
- Rotary and Linear Sliders
- Touch Pads

Typical Applications

- Appliances
- PC Peripherals
- Access Controls
- MP3 Players
- Remote Controls
- Mobile Phones

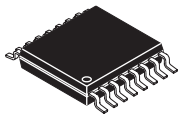
ORDERING INFORMATION			
Device Name	**Temperature Range**	**Case Number**	**Rotary Slider**
MPR081Q	-40°C to +85°C	1679 (16-Lead QFN)	16-Positions
MPR081EJ		948F (16-Lead TSSOP)	

MPR081

Touch Pad Controller

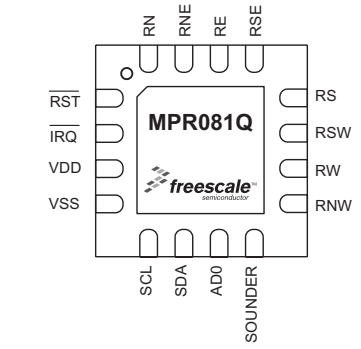
Bottom View

16-LEAD QFN
CASE 1679



16-LEAD TSSOP
CASE 948F

Top View



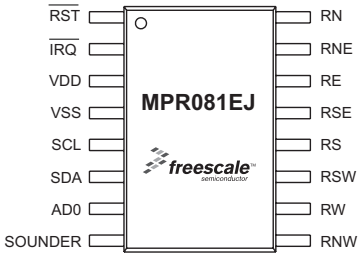


Figure 1. Pin Connections

freescale semiconductor

Table 1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage (with respect to VSS) VDD All other pins	—	 -0.3 to +3.8 VSS-0.3 to VDD+0.3	 V V
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

Table 2. ESD and Latch-Up Protection Characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latch-Up Current at T_A = 85°C	—	±100	mA

Table 3. DC Characteristics

(Typical Operating Circuit, V+ =1.8 V to 3.6 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3 V, T_A = +25°C.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Units
Operating Supply Voltage	V+	—	1.8		3.6	V
Standby Current (I^2C Interface idle)	I_+	SCL and SDA at V+ or GND	TBD			µA
Input High Voltage SDA, SCL	V_{IH}	—	0.7 x VDD	—	—	V
Input Low Voltage SDA, SCL	V_{IL}	—	—	—	0.35 x VDD	V
Input Leakage Current SDA, SCL	I_{IH}, I_{IL}	—	—	0.025	1	µA
Input Capacitance SDA, SCL	—	—	—	—	7	pF
Output Low Voltage SDA, $\overline{IRQ}$	V_{OL}	I_{OL} = 6 mA	—	—	0.5	V

Table 4. Interrupt $\overline{IRQ}$ Timing Characteristics

(Typical Operating Circuit, V+ = 1.8 V to 3.6 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3 V, T_A = +25°C.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Units
$\overline{IRQ}$ Reset delay time from STOP	t_{IP}	$C_L \leq 100$ pF	—	—	TBD	µs
$\overline{IRQ}$ Reset delay time from acknowledge	t_{IR}	$C_L \leq 100$ pF	—	—	TBD	µs

Table 5. I^2C AC Characteristics

(Typical Operating Circuit, V+ = 1.8 V to 3.6 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Units
Serial Clock Frequency	f_{SCL}	—	—	400	kHz
Bus Timeout	$F_{TIMEOUT}$	—	31.25	—	ms
Bus Free Time Between a STOP and a START Condition	t_{BUF}	1.3	—	—	µs
Hold Time, (Repeated) START Condition	$t_{HD, STA}$	0.6	—	—	µs
Repeated START Condition Setup Time	$t_{SU, STA}$	0.6	—	—	µs
STOP Condition Setup Time	$t_{SU, STO}$	0.6	—	—	µs
Data Hold Time	$t_{HD, DAT}$	—	—	0.9	µs
Data Setup Time	$t_{SU, DAT}$	100	—	—	ns
SCL Clock Low Period	t_{LOW}	1.3	—	—	µs
SCL Clock High Period	t_{HIGH}	0.7	—	—	µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	—	$20+0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	—	$20+0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F.TX}$	—	$20+0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	—	50	—	ns
Capacitive Load for Each Bus Line	C_b	—	—	400	pF

Table 6. Pin Description

Pin	Name	Function
1	$\overline{\text{RST}}$	Reset Input. Active low clears the 2-wire interface and puts the device in the same condition as power-up reset.
2	$\overline{\text{IRQ}}$	Interrupt Output. $\overline{\text{IRQ}}$ is the active-low open-drain interrupt output signalling new events.
3	VDD	Positive Supply Voltage Bypass VDD to VSS with a 0.1µF ceramic capacitor
4	VSS	Ground
5	SCL	I²C-Compatible Serial Clock Input
6	SDA	I²C-Compatible Serial Data I/O
7	AD0	Address input 0. Connect to VSS to select device slave address 0x4C. Connect to VDD to select device slave address 0x4D.
8	SOUNDER	Sounder driver output. Connect a piezo-ceramic sounder from this output to ground. Output is push-pull.
9 - 16	RNW, RW, RSW, RS, RSE, RE, RNE, RN	Rotary Touch Inputs. Connect the 8 inputs to a 16-position rotary sensor.
PAD	Exposed Pad	Exposed Pad on Package Underside (QFN only). Connect to VSS.

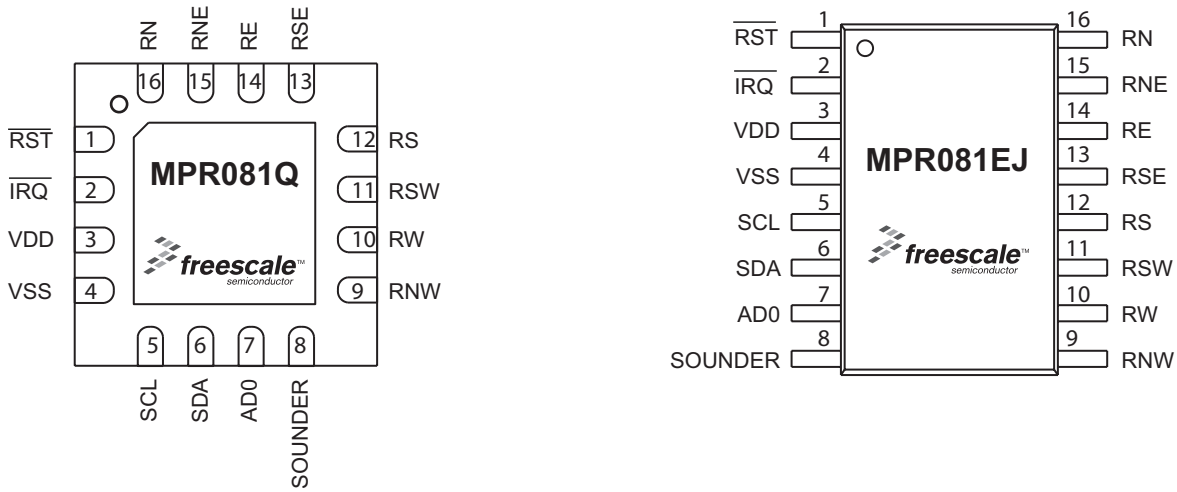


Figure 2. MPR081 Pinout

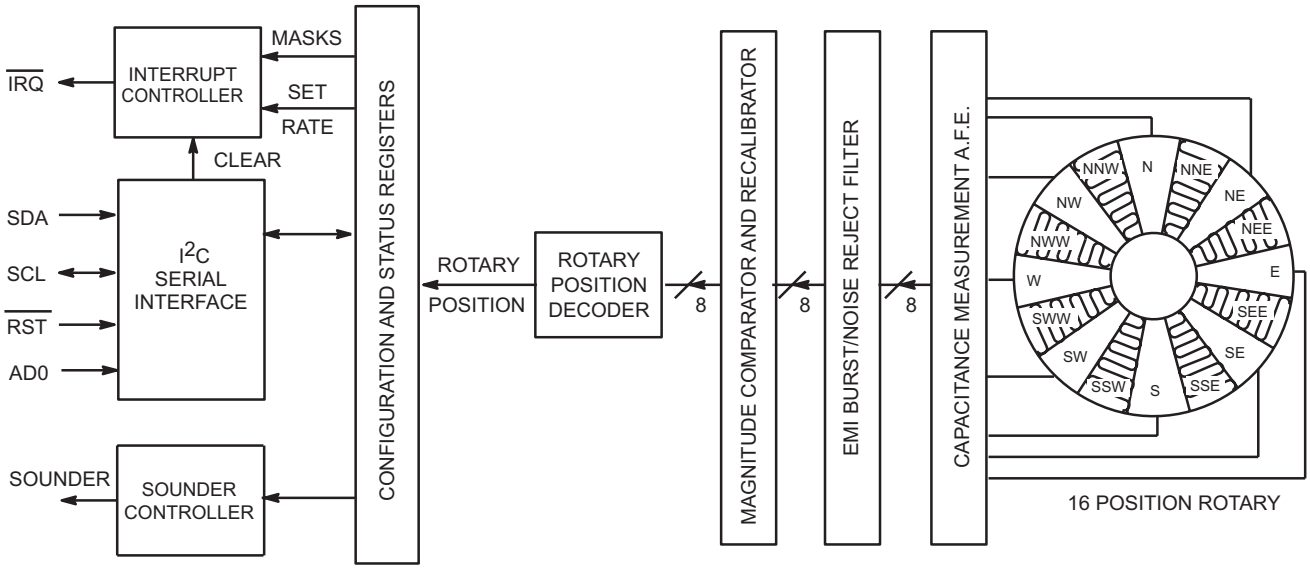


Figure 3. Internal Block Diagram

DETAILED DESCRIPTION

FUNCTIONAL OVERVIEW

The MPR081user interface controller monitors various combinations of capacitive touch pads, capacitive sliders, capacitive rotaries, and mechanical keys. The device includes a piezo buzzer driver which generates key click sounds to provide audible feedback of pad touches and/or key presses. The MPR081 also uses a standardized user register set to configure the part on power up, and to read pad, slider and key status. The commonality between products in the MPR08 family of controllers simplifies migration between parts.

Table 7. MPR08 Family Overview

Product	Bus	Sounder	Rotary Slider	Touch Pad Array	Main Attribute
MPR081	I^2C with $\overline{RST}$	Yes	16-Positions	—	Highest resolution rotary
MPR082	I^2C with $\overline{RST}$	Yes	—	20 Pads(1)	Two independent arrays of 10 touch pads

1. The 20 pads are implemented by two independent arrays of 10 touch pads.

A quick word on terminology:

- A mechanical **keyswitch** is a switch containing, at its simplest, two contacts which have either a high (>10 MΩ) or a low resistance (<10 kΩ) between them depending on switch position. Momentary push switches normally are low resistance when pressed. Latching switches (such as slide switches) provide high resistance in one position, low resistance in the other.
- A capacitive **touch pad** is a contactless 'key' which detects the presence or absence of a finger. The raw detection output is a single bit giving touch condition.
- A capacitive **rotary** is a group of touch pads arranged in a ring for which not only the presence or absence of a finger is detected, but also the position of a finger along the circumference of the rotary.
- A capacitive **slider** is an elongated touch pad for which not only the presence or absence of a finger is detected, but also the position of a finger along the length of the slider. The raw detection output is a single bit giving touch condition, plus a multi-bit word for position. A typical application is a volume control, where one end of the slider corresponds to minimum volume and the other end to maximum.
- A **full pad** is a touch pad whose conductive area is connected to one electrode of the touch controller and ground.
- A **split pad** is a touch pad whose conductive area is connected to more than one electrode of the touch controller. For the MPR08 family, a split pad is always connected to two electrodes and typically looks like a pair of interlaced fingers.
- A **pad array** is a collection of full and split pads interconnected to each other and a number of electrode lines. The number of pads available in a pad array with N electrode lines using full and two-electrode split pads is sum(1 to N), made up of N full pads and sum(1 to (N-1)) split pads. The MPR082 uses two sets of 4 electrode lines and, therefore, each 4-electrode pad array has a capability of 4 full pads and sum(1 to 3) or 1+2+3 = 6 split pads, and a total pad count of sum(1 to 4) or 1+2+3+4 = 10 full plus split pads.
- A pad array with **n key lockout** will only report one touch at a time. Multiple simultaneous touches are ignored.
- A pad array with **2 key rollover** ignores further pads after touching a first pad. If a pad is touched and held, and then a second pad is touched, the second pad is ignored. If the first pad is released while the second pad is still touched, then the second pad will be reported as a new touch.
- A pad array with **n-key rollover** allows any number of pads will be detected as pressed in succession or simultaneously without requiring any previous pads to be released first.

SERIAL INTERFACE

SERIAL-ADDRESSING

The MPR081 operates as a slave that sends and receives data through an I^2C 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bi-directional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MPR081 and generates the SCL clock that synchronizes the data transfer.

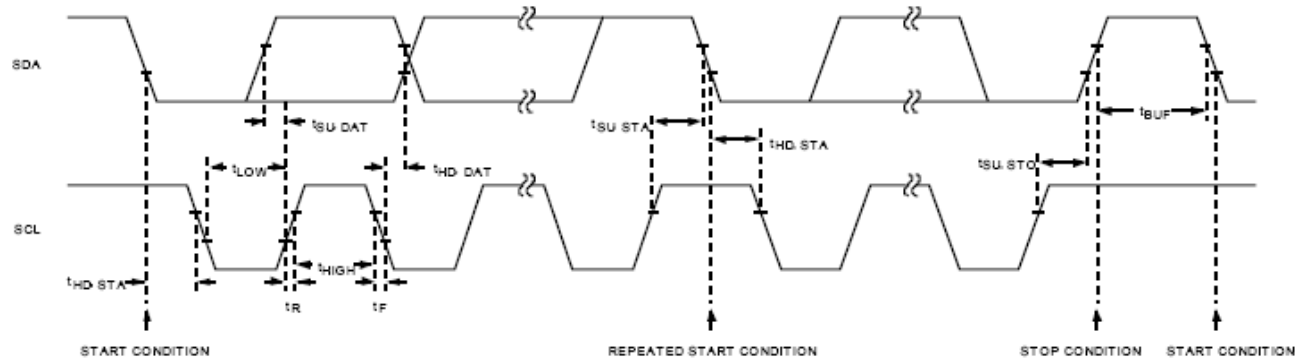


Figure 4. 2-Wire Serial Interface Timing Details

The MPR081 SDA line operates as both an input and an open-drain output. A pull-up resistor, typically 4.7 kΩ, is required on SDA. The MPR081 SCL line operates only as an input. A pull-up resistor, typically 4.7 kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 5) sent by a master, followed by the MPR081's 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

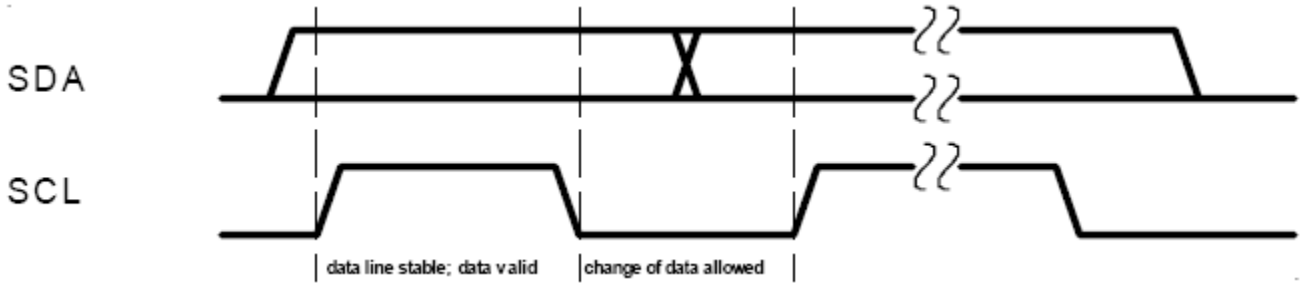


Figure 5. Start and Stop Conditions

START AND STOP CONDITIONS

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

BIT TRANSFER

One data bit is transferred during each clock pulse (Figure 6). The data on SDA must remain stable while SCL is high.

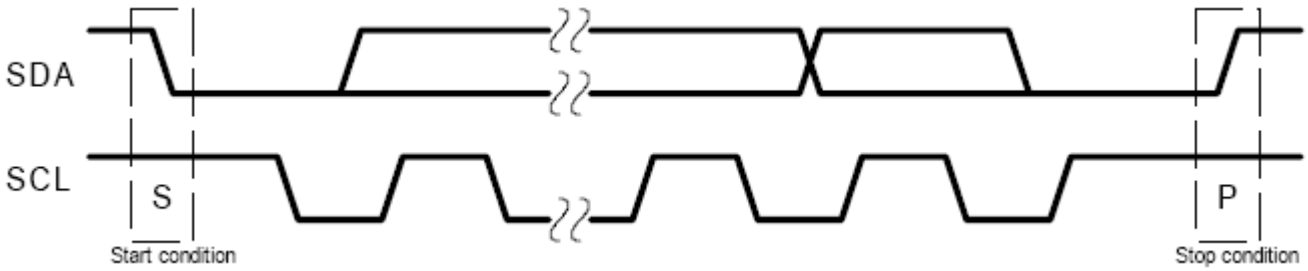


Figure 6. Bit Transfer

ACKNOWLEDGE

The acknowledge bit is a clocked 9th bit (Figure 7) which the recipient uses to handshake receipt of each byte of data. Thus each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MPR081, the MPR081 generates the acknowledge bit because the MPR081 is the recipient. When the MPR081 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

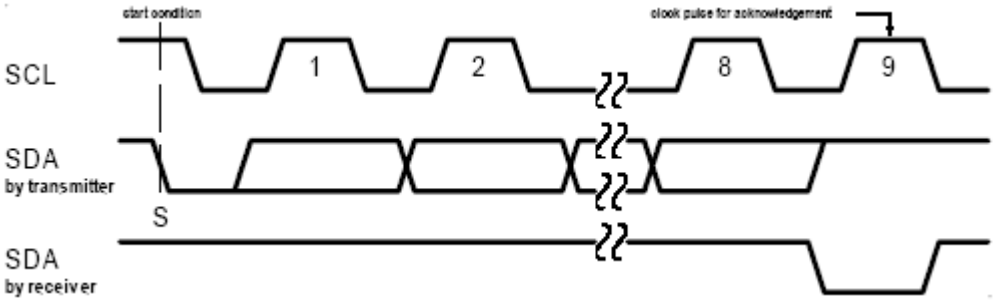


Figure 7. Acknowledge

THE SLAVE ADDRESS

The MPR081 has a 7-bit long slave address (Figure 5). The bit following the 7-bit slave address (bit eight) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The MPR081 has a factory set I²C slave address which is normally 1001100 (0x4C). Contact the factory to request a different I²C slave address, which is available in the range 0001000 to 1110111 (0x08 to 0xEF).

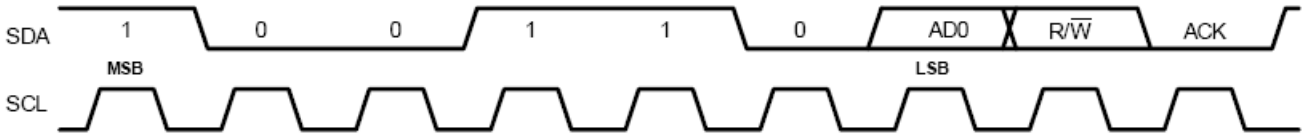


Figure 8. Slave Address

The MPR081 monitors the bus continuously, waiting for a START condition followed by its slave address. When a MPR081 recognizes its slave address, it acknowledges and is then ready for continued communication.

MESSAGE FORMAT FOR WRITING THE MPR081

A write to the MPR081 comprises the transmission of the MPR081's keyscan slave address with the R/$\overline{W}$ bit set to 0, followed by at least one byte of information. The first byte of information is the command byte. The command byte determines which register of the MPR081 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MPR081 takes no further action (Figure 9) beyond storing the command byte. Any bytes received after the command byte are data bytes.

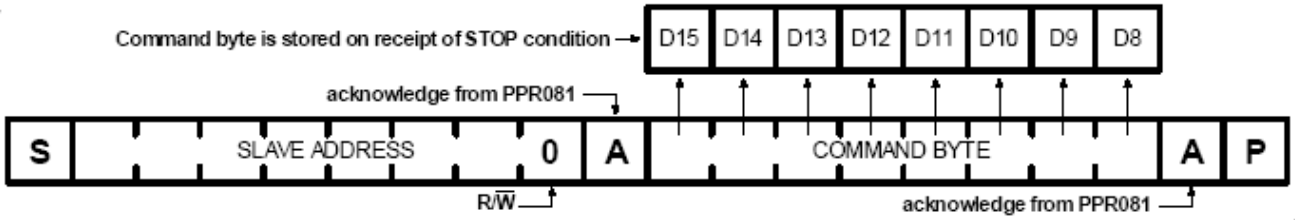


Figure 9. Command Byte Received

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MPR081 selected by the command byte (Figure 10).

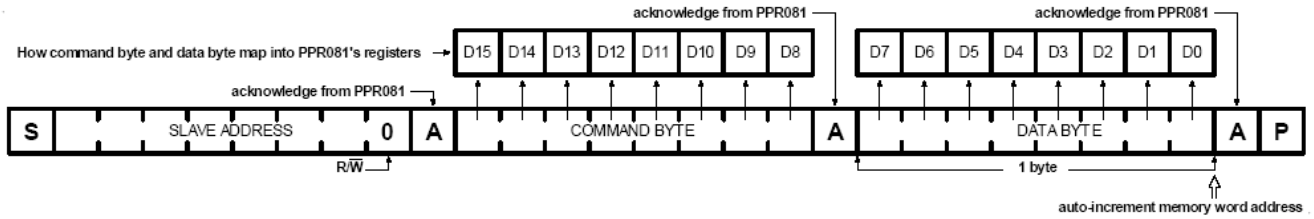


Figure 10. Command and Single Data Byte Received

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MPR081 internal registers because the command byte address generally auto-increments (Table 8).

MESSAGE FORMAT FOR READING THE MPR081

The MPR081 is read using the MPR081's internally stored command byte as address pointer, the same way the stored command byte is used as address pointer for a write. The pointer generally auto-increments after each data byte is read using the same rules as for a write (Table 11). Thus, a read is initiated by first configuring the MPR081's command byte by performing a write (Figure 9). The master can now read 'n' consecutive bytes from the MPR081, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to re-set the command byte's address because the stored command byte address will generally have been auto-incremented after the write (Table 8).

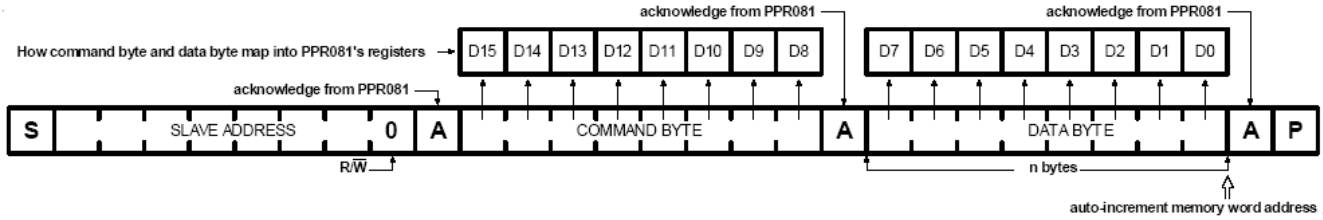


Figure 11. 'n' Data Bytes Received

OPERATION WITH MULTIPLE MASTERS

If the MPR081 is operated on a 2-wire interface with multiple masters, a master reading the MPR081 should use repeated start(s) between the write(s) which sets the MPR081's address pointer, and the read(s) that take the data from the location(s). This is because it is possible for master #2 to take over the bus after master #1 has set up the MPR081's address pointer, but before master #1 has read the data. If master #2 subsequently re-sets the master of the MPR08's address pointer, then master #1's read may be from an unexpected location.

DEVICE RESET

The reset input $\overline{RST}$ is an active-low input. When taken low, $\overline{RST}$ clears any transaction to or from the MPR081 on the serial interface and configures the internal registers to the same state as a power-up reset (Table 9). The MPR081 then waits for a START condition on the serial interface.

CONTROLLING AND READING THE MPR081

REGISTER ORGANIZATION

The MPR081 is a peripheral that is controlled and monitored though a small array of internal registers which are accessed through the I^2C bus.

INITIAL POWER-UP

On power-up, the interrupt output $\overline{IRQ}$ is reset, and $\overline{IRQ}$ will go high. The registers are reset to the values shown in Table 9.

STANDBY MODE

When the serial interface is idle, the MPR081 automatically enters standby mode. If any of the features are used, the operating current rises because the internal timing oscillator is running and toggling counters.

Figure 12. Master Tick Counter and Pad/Key Input Sampling with Autorepeat

INTERRUPT CONTROLLER AND $\overline{\text{IRQ}}$ OUTPUT

The $\overline{\text{IRQ}}$ pin is an open-drain, latching interrupt output which automatically alerts changes to a user-configurable combination of keyswitches and/or touch pads. $\overline{\text{IRQ}}$ requires an external pullup resistor, which can be connected to any voltage up to VDD. When set active low, $\overline{\text{IRQ}}$ is reset high immediately after the slave address acknowledge of the first subsequent read or write access to the MPR081. If an interrupt causing event occurs during an I^2C transmission to the MPR081, the interrupt is not asserted. Instead, it is asserted after the I^2C transmission is terminated (by a STOP condition or a repeated START condition), but only if the affected registers were not read during the I^2C communication. This avoids unnecessary assertion of the interrupt.

An interrupt can be enabled for:

- Initial touch (when rotary condition goes from untouched to touched)
- Touch release

ROTARY TOUCH INTERFACE

The rotary interface has to distinguish touch status through varying user conditions (different finger sizes in bare hands or gloves) and environmental conditions (electrical and RF noise, sensor contamination with dirt or moisture). The rotary circuitry reports status as one of five conditions: rotary untouched, and rotary touched in one of four positions.

Normally, the rotary is only touched in one position, ideally near the middle of one of the four pads. If a touch occurs more or less between pads, either the nearest pad will be given or the touch will be ignored depending on exact touch position and finger size. The rotary circuitry interprets multiple simultaneous rotary touches (more than one rotary pad being touched at the same time) as best it can. The scenarios are as follows:

1. Two rotary pads touched at the same time
   - If the two touched rotary pads are both full or both split, the touches are ignored until one is removed
   - If one touched rotary pad is full and the other touched rotary pad is split, the full pad position will be reported.
   - If the full pad touch is removed first, the split pad position now will be reported.
2. First one rotary pad is touched and held, then a second rotary pad is touched and held.
   - The second touch will be ignored and the first touch will continue to be active. If the first touch is removed while the second pad is still being touched, then the second pad becomes the only touched pad and so is reported.

Table 8. Register Address Map

Register	Register Address								Register Address	Auto-Increment Address	Auto-Increment Loop
	D15	D14	D13	D12	D11	D10	D9	D8			
FIFO	0	0	0	0	0	0	0	0	0x00	0x00	FIFO
Fault	0	0	0	0	0	0	0	1	0x01	0x02	↓
Rotary Status	0	0	0	0	0	0	1	0	0x02	0x00	↳ → ↑ FIFO
Rotary Configuration	0	0	0	0	0	0	1	1	0x03	0x04	↓
Sensitivity	0	0	0	0	0	1	0	1	0x04	0x05	↓
Master Tick Counter	0	0	0	0	0	1	1	0	0x05	0x06	↓
Touch Acquisition Sample Rate	0	0	0	0	0	1	1	1	0x06	0x07	↓
Sounder	0	0	0	0	1	0	0	0	0x07	0x08	↓
Sleep Period	0	0	0	0	1	0	0	1	0x08	0x09	↓
Configuration	0	0	0	0	1	0	1	0	0x09	0x00	↳ → ↑ FIFO

Table 9. Power-Up Register Configurations

Register Function	Power-Up Condition	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
FIFO	FIFO is empty	0x00	0	0	0	0	0	0	0	0
Fault	No faults	0x01	0	0	0	0	0	0	0	0
Rotary Status	Rotary is untouched	0x02	0	0	0	0	0	0	0	0
Rotary Configuration	Rotary is enabled, without interrupts, with sounder enabled	0x03	1	0	0	0	0	0	0	1
Sensitivity	Level is very sensitive	0x04	0	0	0	0	0	0	0	0
Master Tick Counter	Master tick period is 10 ms	0x05	0	0	0	0	0	1	0	1
Touch Acquisition Sample Rate	Touch acquisition sample rate is 5 master tick periods	0x06	0	0	0	0	0	1	0	0
Sounder	Sounder is globally enabled, 10 ms of 1 kHz	0x07	0	0	0	0	0	0	0	1
Sleep Period	Sleep mode is disabled	0x08	0	0	0	0	0	0	0	0
Configuration	Shutdown mode. $\overline{\text{IRQ}}$ is disabled	0x09	0	0	0	0	0	0	0	0

Table 10. FIFO Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
FIFO Register[1]	**1**	**0x00**	**More Flag**	**Empty Flag**	**Overflow Flag**	**Rotary Pad that has been detected as pressed**				
FIFO Status										
Clear the FIFO. Subsequent reads without any intervening addition(s) to the FIFO will return 1'b0100000	0	0x00	Clear FIFO (D7 - D0 data is don't care; it is not stored)							
This data is not the last FIFO item. FIFO has not overflowed.	1		1	0	0	X	X	X	X	X
This data is not the last FIFO item. FIFO did overflow, discarding the most recent entries.			1	0	1	X	X	X	X	X
This data is the last FIFO item. FIFO has not overflowed. Subsequent reads without any intervening addition(s) to the FIFO will return 1'b0100000			0	0	0	X	X	X	X	X
This data is the last FIFO item. FIFO did overflow, discarding the most recent entries (FIFO overflow flag will now be cleared). Subsequent reads without any intervening addition(s) to the FIFO will return 1'b0100000			0	0	1	X	X	X	X	X
FIFO is empty			0	1	0	0	0	0	0	0
Rotary Input Events										
Rotary has been released	1	0x00	X	X	X	0	0	0	0	0
Rotary is in position North (N)			X	X	X	1	0	0	0	0
Rotary is in position NNE			X	X	X	1	0	0	0	1
Rotary is in position NE			X	X	X	1	0	0	1	0
Rotary is in position NEE			X	X	X	1	0	0	1	1
Rotary is in position East (E)			X	X	X	1	0	1	0	0
Rotary is in position SEE			X	X	X	1	0	1	0	1
Rotary is in position SE			X	X	X	1	0	1	1	0
Rotary is in position SSE			X	X	X	1	0	1	1	1
Rotary is in position South (S)			X	X	X	1	1	0	0	0
Rotary is in position SSW			X	X	X	1	1	0	0	1
Rotary is in position SW			X	X	X	1	1	0	1	0
Rotary is in position SWW			X	X	X	1	1	0	1	1
Rotary is in position West (W)			X	X	X	1	1	1	0	0
Rotary is in position NWW			X	X	X	1	1	1	0	1
Rotary is in position NW			X	X	X	1	1	1	1	0
Rotary is in position NNW			X	X	X	1	1	1	1	1

1. Reading or writing the MPR08 clears $\overline{IRQ}$, $\overline{IRQ}$ will only be re-asserted by an event after the FIFO has been emptied by read(s).

Table 11. Fault Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Fault Register	**1**	0x01	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Fault**
Write Fault Register	**0**		**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
No faults have been detected on the electrode inputs	1		X	X	X	X	X	X	0	0
One or more electrode inputs is detected as shorted to V_{DD}			X	X	X	X	X	X	0	1
One or more electrode inputs is detected as shorted to V_{SS}			X	X	X	X	X	X	1	0

Table 12. Current Rotary Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Current Rotary Status Register	**1**	0x02	**0**	**0**	**0**	**Current Rotary Position**				
Write Current Rotary Status Register	**0**		**A write to this register is ignored, and has no effect**							
Rotary is released or is not enabled	1		0	0	0	0	0	0	0	0
Rotary is in position North (N)			0	0	0	1	0	0	0	0
Rotary is in position NNE			0	0	0	1	0	0	0	1
Rotary is in position NE			0	0	0	1	0	0	1	0
Rotary is in position NEE			0	0	0	1	0	0	1	1
Rotary is in position East (E)			0	0	0	1	0	1	0	0
Rotary is in position SEE			0	0	0	1	0	1	0	1
Rotary is in position SE			0	0	0	1	0	1	1	0
Rotary is in position SSE			0	0	0	1	0	1	1	1
Rotary is in position South (S)			0	0	0	1	1	0	0	0
Rotary is in position SSW			0	0	0	1	1	0	0	1
Rotary is in position SW			0	0	0	1	1	0	1	0
Rotary is in position SWW			0	0	0	1	1	0	1	1
Rotary is in position West (W)			0	0	0	1	1	1	0	0
Rotary is in position NWW			0	0	0	1	1	1	0	1
Rotary is in position NW			0	0	0	1	1	1	1	0
Rotary is in position NNW			0	0	0	1	1	1	1	1

Table 13. Rotary Configuration Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Rotary Configuration Register	**1**	0x03	**RotClickEN**	**0**	**0**	**0**	**RotR**	**RotT**	**0**	**RotEN**
Write Rotary Configuration Register	**0**			**X**	**X**	**X**			**X**	
Disable Rotary function entirely	X		X	X	X	X	X	X	X	0
Enable Rotary function			X	X	X	X	X	X	X	1
Disable Rotary touch or press action entering FIFO			X	X	X	X	X	0	X	X
Enable Rotary touch action entering FIFO as values 1'bxxx10000 through 1'bxxx11111			X	X	X	X	X	1	X	1
Disable Rotary release action entering FIFO			X	X	X	X	0	X	X	X
Enable Rotary released action entering FIFO as value 1'bxxx01111			X	X	X	X	1	X	X	1
Rotary touches do not cause the sounder to operate			0	X	X	X	X	X	X	1
Rotary touches operate the sounder			1	X	X	X	X	X	X	1

Table 14. Sensitivity Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Number of Position Register	**1**	0x04	**0**	**0**	**0**	**Sensitivity Level**				
Write Number of Position Register	**0**		**X**	**X**	**X**					
Sensitivity setting is level 1	1		**X**	**X**	**X**	**X**	**X**	0	0	0
Sensitivity setting is level 2			**X**	**X**	**X**	**X**	**X**	0	0	1
Sensitivity setting is level 3			**X**	**X**	**X**	**X**	**X**	0	1	0
Sensitivity setting is level 4			**X**	**X**	**X**	**X**	**X**	0	1	1
Sensitivity setting is level 5			**X**	**X**	**X**	**X**	**X**	1	0	0
Sensitivity setting is level 6			**X**	**X**	**X**	**X**	**X**	1	0	1
Sensitivity setting is level 7			**X**	**X**	**X**	**X**	**X**	1	1	0

Table 15. Master Tick Period Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Master Tick Period Register	**1**	0x05	**0**	**0**	**0**	**Master Tick**				
Write Master Tick Period Register	**0**		**X**	**X**	**X**					
Master Tick Period is 5 ms	X		X	X	X	0	0	0	0	0
Master Tick Period is 6 ms			X	X	X	0	0	0	0	1
Master Tick Period is 7 ms			X	X	X	0	0	0	1	0
Master Tick Period is 8 ms			X	X	X	0	0	0	1	1
- all the way through to -			—	—	—	—	—	—	—	—
Master Tick Period is 33 ms			X	X	X	1	1	1	0	0
Master Tick Period is 34 ms			X	X	X	1	1	1	0	1
Master Tick Period is 35 ms			X	X	X	1	1	1	1	0
Master Tick Period is 36 ms			X	X	X	1	1	1	1	1

Table 16. Touch Acquisition Sample Rate Register Format

Register	Register Address	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Touch Acquisition Sample Rate Register	**0x06**	**Touch Acquisition Sample Rate**							
Touch acquisition sample rate is 1 master tick period	0x06	X	X	0	0	0	0	0	0
Touch acquisition sample rate is 2 master tick periods		X	X	0	0	0	0	0	1
Touch acquisition sample rate is 3 master tick periods		X	X	0	0	0	0	1	0
Touch acquisition sample rate is 4 master tick periods		X	X	0	0	0	0	1	1
- all the way through to -		—	—	—	—	—	—	—	—
Touch acquisition sample rate is 61 master tick periods		X	X	1	1	1	1	0	0
Touch acquisition sample rate is 62 master tick periods		X	X	1	1	1	1	0	1
Touch acquisition sample rate is 63 master tick periods		X	X	1	1	1	1	1	0
Touch acquisition sample rate is 64 master tick periods		X	X	1	1	1	1	1	1

Table 17. Sounder Configuration Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Sounder Configuration Register	**1**	0x07	**0**	**0**	**0**	**0**	**0**	**SoundD**	**SoundF**	**SoundEN**
Write Sounder Configuration Register	**0**		**X**	**X**	**X**	**X**	**X**			
Globally disable sounder output	1		X	X	X	X	X	X	X	0
Globally enable sounder output			X	X	X	X	X	X	X	1
Sounder frequency is 1 kHz			X	X	X	X	X	X	0	1
Sounder frequency is 2 kHz			X	X	X	X	X	X	1	1
Sounder click period is 10 ms			X	X	X	X	X	0	X	1
Sounder click period is 20 ms			X	X	X	X	X	1	X	1

Table 18. Sleep Period Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Number of Position Register	**1**	0x08	**Duration of Sleep Cycle**							
Write Number of Position Register	**0**									
Sleep Mode is disabled, sensor is always running	1		0	0	0	0	0	0	0	0
Sleep period is 10 x touch acquisition sample period			X	X	X	X	0	0	1	0
Sleep period is 20 x touch acquisition sample period			X	X	X	X	0	0	1	1
Sleep period is 30 x touch acquisition sample period			X	X	X	X	0	1	0	0
Sleep period is 40 x touch acquisition sample period			X	X	X	X	0	1	0	1
Sleep period is 50 x touch acquisition sample period			X	X	X	X	0	1	1	0
Sleep period is 60 x touch acquisition sample period			X	X	X	X	0	1	1	1
Sleep period is 70 x touch acquisition sample period			X	X	X	X	1	0	0	0
Sleep period is 80 x touch acquisition sample period			X	X	X	X	1	0	0	1
Sleep period is 90 x touch acquisition sample period			X	X	X	X	1	0	1	0
Sleep period is 100 x touch acquisition sample period			X	X	X	X	1	0	1	0
Idle timeout period is 8 x touch acquisitions sample period			0	0	0	1	X	X	X	X
Idle timeout period is 16 x touch acquisitions sample period			0	0	1	0	X	X	X	X
Idle timeout period is 32 x touch acquisitions sample period			0	0	1	1	X	X	X	X
—all the way through to—			—	—	—	—	—	—	—	—
Idle timeout period is 112 x touch acquisitions sample period			1	1	1	0	X	X	X	X
Idle timeout period is 120 x touch acquisitions sample period			1	1	1	1	X	X	X	X

Table 19. Configuration Register Format

Register	R/$\overline{W}$	Register Address	Register Data							
			D7	D6	D5	D4	D3	D2	D1	D0
Read Configuration Register	**1**	0x09	**Interrupt Rate**			RESET	N/A	WAKE	IRQEN	RUN
Write Configuration Register	**0**									
MPR081 is in shutdown, and will not scan the rotary. Note that FIFO contents are *not* cleared when entering shutdown and can be read any time during shutdown.	X		X	X	X	1	X	X	X	0
MPR081 is operating, scanning the rotary, with $\overline{IRQ}$ interrupt output disabled. Poll the FIFO register 0x00 and/or the Current Rotary register 0x02 to determine current rotary status. Note that FIFO contents are cleared before exiting shutdown			X	X	X	1	X	X	0	1
MPR081 is operating, scanning the rotary, with $\overline{IRQ}$ interrupt output enabled. $\overline{IRQ}$ behavior is controlled by Interrupt Rate bits D5-D7, and is asserted on the first entry into the FIFO from empty. Note that FIFO contents are cleared before exiting shutdown			X	X	X	1	X	X	1	1
MPR081 will go into low power sleep mode after an idle period timeout. While in low power sleep mode, device cannot be addressed via I^2C except by asserting the wake pin.			X	X	X	1	X	0	1	X
MPR081 will remain awake and can be addressed at anytime via I^2C.			X	X	X	1	X	1	1	X
System reset asserted. MPR081 can be addressed via I^2C at anytime.			X	X	X	0	X	X	1	1
System reset de-asserted. MPR081 can be addressed via I^2C at anytime.			X	X	X	1	X	X	1	1
$\overline{IRQ}$ interrupt is immediate when FIFO changes from empty			0	0	0	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 4 master tick periods after the last $\overline{IRQ}$ rise			0	0	1	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 12 master tick periods after the last $\overline{IRQ}$ rise			0	1	0	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 20 master tick periods after the last $\overline{IRQ}$ rise			0	1	1	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 28 master tick periods after the last $\overline{IRQ}$ rise			1	0	0	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 36 master tick periods after the last $\overline{IRQ}$ rise			1	0	1	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 44 master tick periods after the last $\overline{IRQ}$ rise			1	1	0	1	X	X	1	1
$\overline{IRQ}$ interrupt asserts no sooner than 52 master tick periods after the last $\overline{IRQ}$ rise			1	1	1	1	X	X	1	1

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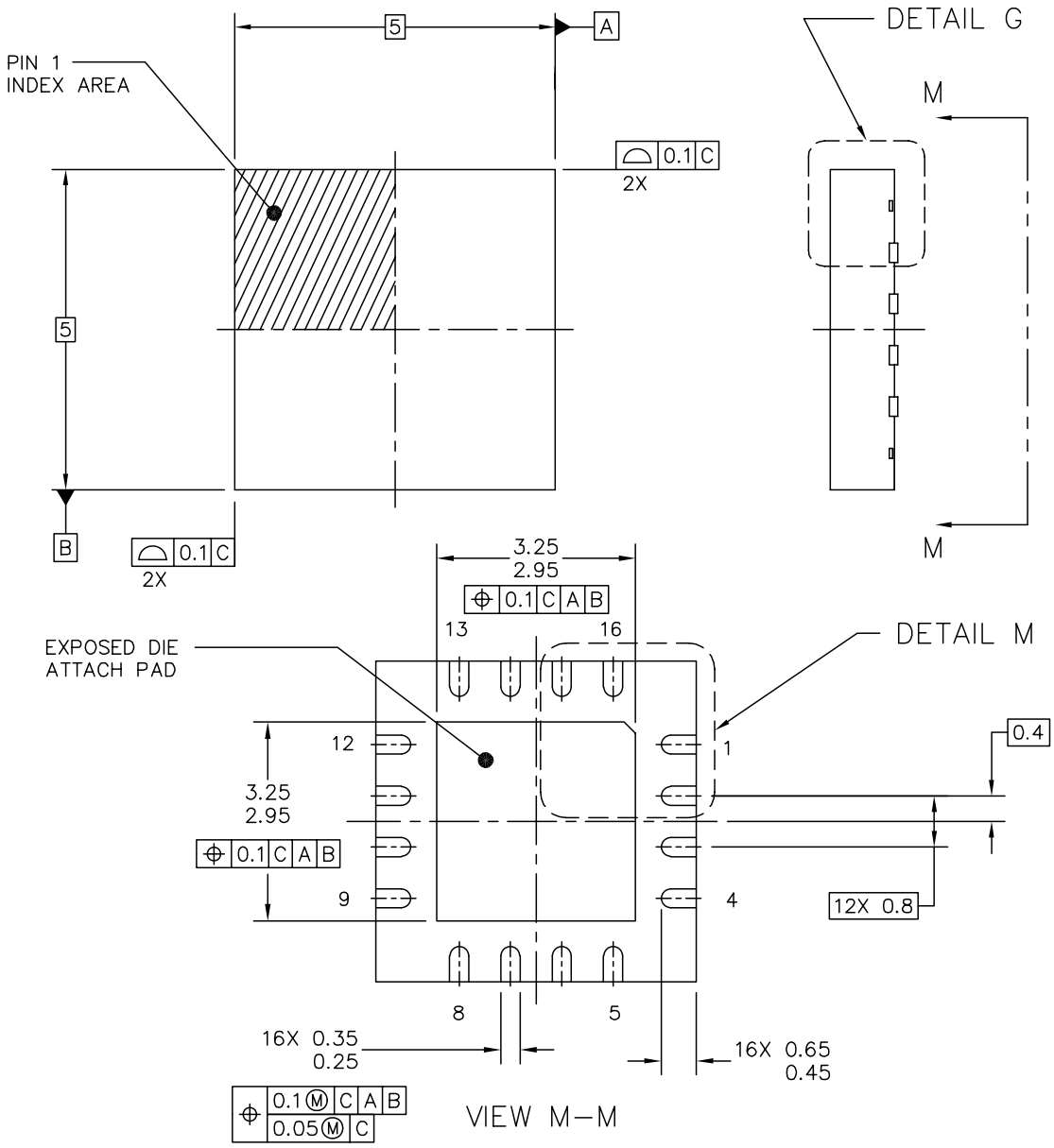

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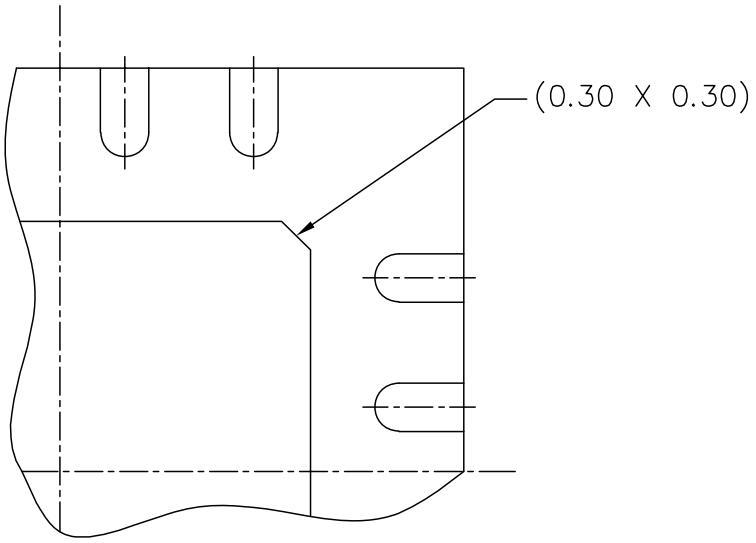

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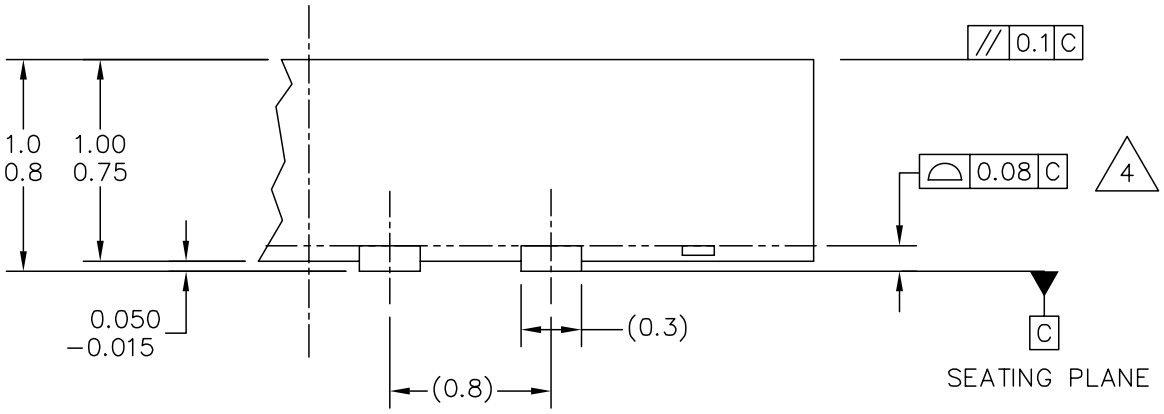

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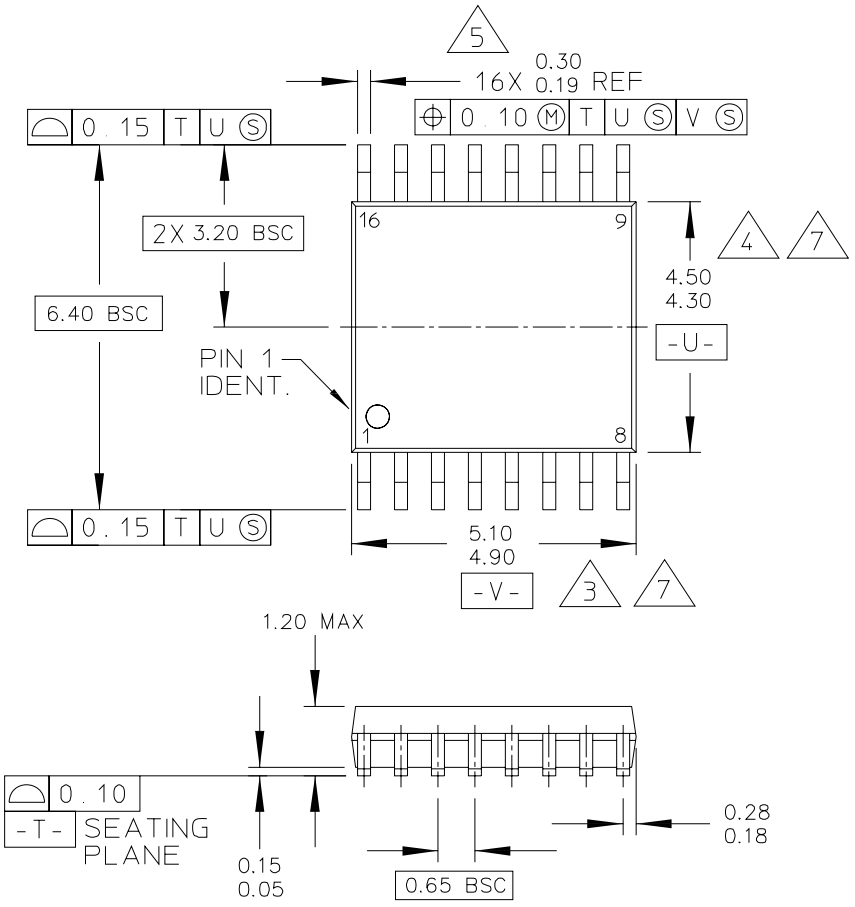

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MPR081

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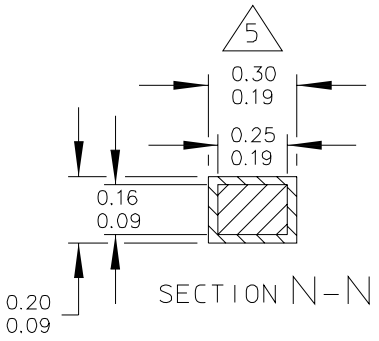

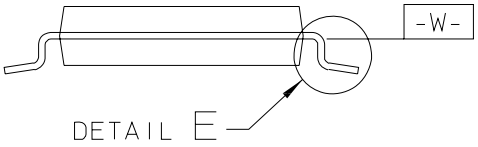

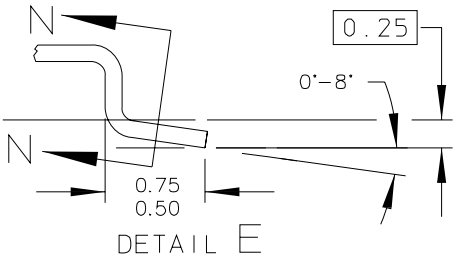

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