

DATA SHEET

74F166

8-bit bidirectional universal shift register

Product specification

1991 Feb 14

IC15 Data Handbook

8-bit bidirectional universal shift register

74F166

FEATURES

- High impedance NPN base inputs for reduced loading (20 μ A in high and low states)
- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- Expandable to 16 bits in 8-bit increments
- Industrial temperature range available (-40°C to +85°C)

DESCRIPTION

The 74F166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active low parallel enable (\overline{PE}) input. When the \overline{PE} is low one setup time before the low-to-high clock transition, parallel data is entered into the register.

When \overline{PE} is high, data is entered into internal bit position Q0 from serial data input (Ds), and the remaining bits are shifted one place to the right (Q0 \rightarrow Q1 \rightarrow Q2, etc.) with each positive going clock transition.

For expansion of the register in parallel to serial converters, the Q7 output is connected to the Ds input of the succeeding stage. The clock input is gated OR structure which allows one input to be used as an active-low clock enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The low-to-high transition of \overline{CE} input should only take place while the CP is high for predictable operation. A low on the master reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a low state.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F166	175MHz	50mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
16-pin plastic DIP	N74F166N	I74F166N	SOT38-4
16-pin plastic SO	N74F166D	I74F166D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Parallel data inputs	1.0/0.033	20 μ A/20 μ A
Ds	Serial data input (shift right)	2.0/0.066	40 μ A/40 μ A
CP	Clock input (active rising edge)	1.0/0.033	20 μ A/20 μ A
\overline{CE}	Clock enable input (active low)	1.0/0.033	20 μ A/20 μ A
\overline{PE}	Parallel enable input (active low)	1.0/0.033	20 μ A/20 μ A
\overline{MR}	Master reset input (active low)	2.0/0.066	40 μ A/40 μ A
Q7	Data output	50/33	1.0mA/20mA

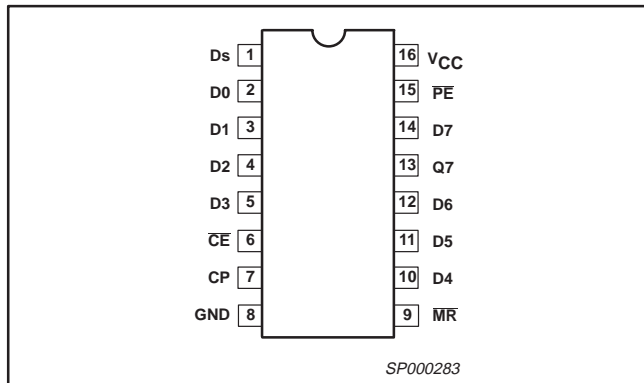
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the low state.

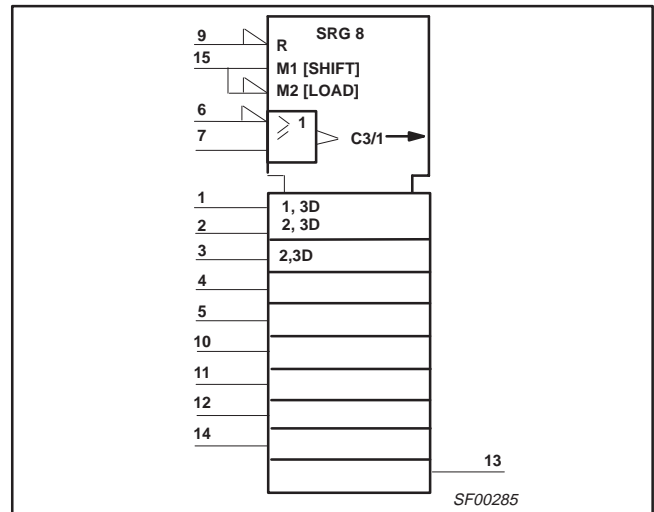
8-bit bidirectional universal shift register

74F166

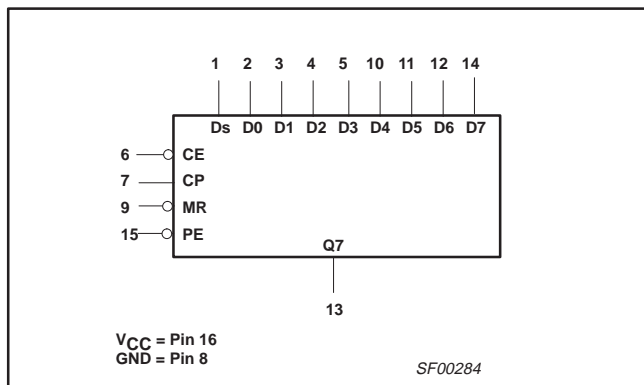
PIN CONFIGURATION



IEC/IEEE SYMBOL



LOGIC SYMBOL



FUNCTION TABLE

INPUTS					Qn REGISTER		OUTPUT	OPERATING MODE
PE	CE	CP	DS	D0 - D7	Q0	Q1 - Q6	Q7	
l	l	↑	X	l - l	L	L - L	L	Parallel load
l	l	↑	X	h - h	H	H - H	H	
h	l	↑	l	X - X	L	q0 - q5	q6	Serial shift
h	l	↑	h	X - X	H	q0 - q5	q6	
X	h	X	X	X - X	qn	q1 - q6	q7	Hold (do nothing)

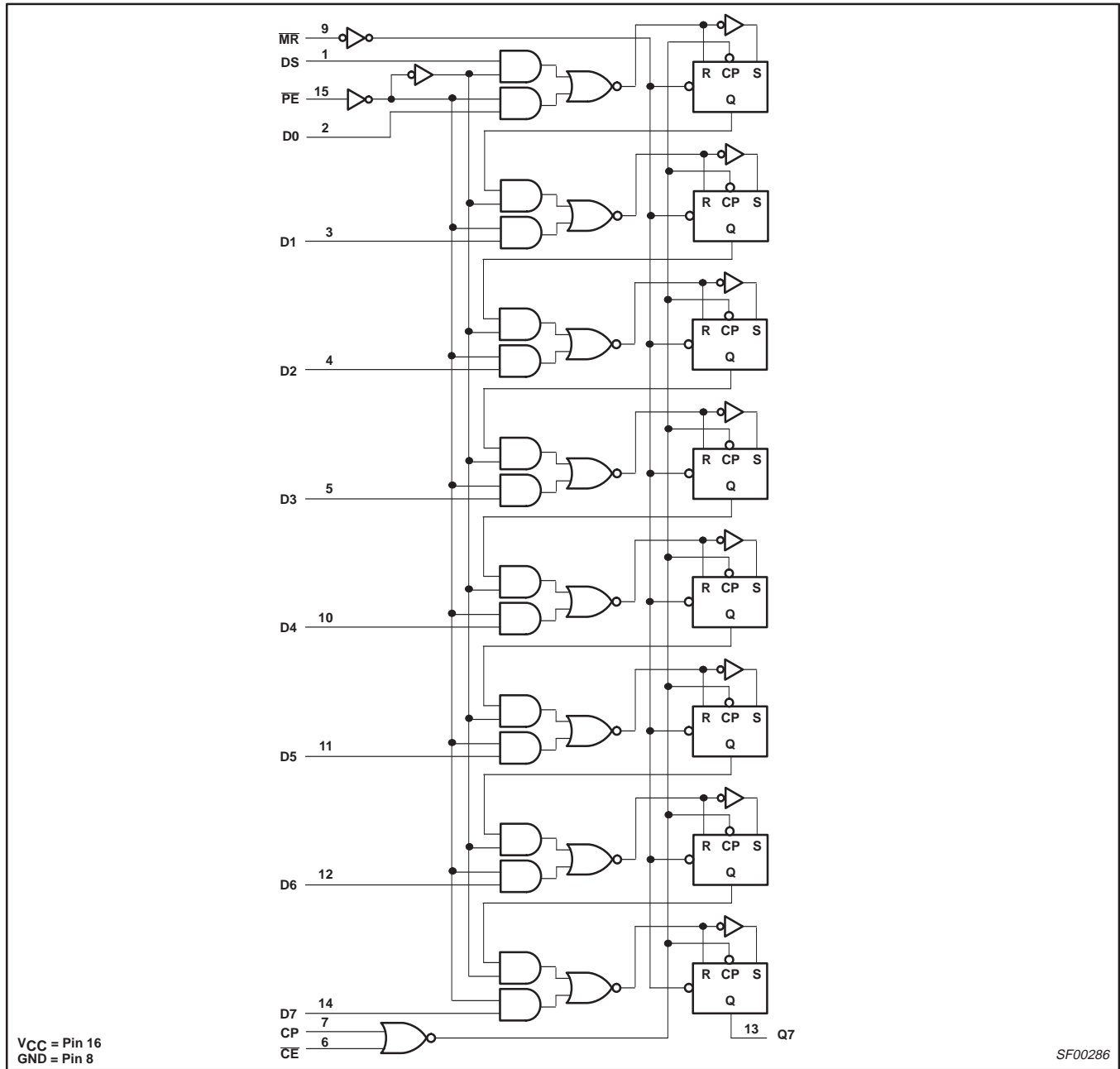
Notes to function table

- H = High-voltage level
- h = High voltage level one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low voltage level one setup time before the low-to-high clock transition
- qn = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the low-to-high clock transition
- X = Don't care
- ↑ = Low-to-high clock transition

8-bit bidirectional universal shift register

74F166

LOGIC DIAGRAM



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74F166

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	-0.5 to +7.0	V	
V _{IN}	Input voltage	-0.5 to +7.0	V	
I _{IN}	Input current	-30 to +5	mA	
V _{OUT}	Voltage applied to output in high output state	-0.5 to V _{CC}	V	
I _{OUT}	Current applied to output in low output state	40	mA	
T _{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T _{stg}	Storage temperature range	-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT	
		MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5.0	5.5	V	
V _{IN}	High-level input voltage	2.0			V	
V _{IL}	Low-level input voltage			0.8	V	
I _{Ik}	Input clamp current			-18	mA	
I _{OH}	High-level output current			-1	mA	
I _{OL}	Low-level output current			20	mA	
T _{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	-40		+85	°C

8-bit bidirectional universal shift register

74F166

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT	
					MIN	TYP ²	MAX		
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = MAX	±10%V _{CC}	2.5			V
					±5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}		0.30	0.50	V
					±5%V _{CC}		0.30	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V	
I _I	Input current at maximum input voltage	others CE, CP ³	V _{CC} = 0.0V, V _I = 7.0V				100	μA	
I _{IH}	High-level input current	others	V _{CC} = MAX, V _I = 2.7V				20	μA	
		MR, Ds					40	μA	
		Industrial only			others			40	μA
					MR, Ds			80	μA
I _{IL}	Low-level input current	others	V _{CC} = MAX, V _I = 0.5V				-20	μA	
		MR, Ds					-40	μA	
I _{OS}	Short-circuit output current ⁴		V _{CC} = MAX			-60	-150	mA	
I _{CC}	Supply current (total)		V _{CC} = MAX, PE = CE = Dn = GND, MR = Ds = 4.5V, CP = ↑			50	70	mA	

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- When testing CP, CE must remain in high state, whereas CP must remain in high state when testing CE.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			T _{amb} = +25°C			T _{amb} = 0°C to +70°C		T _{amb} = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f _{max}	Maximum clock frequency	Waveform 1	135	175		110		100		ns
t _{PLH} t _{PHL}	Propagation delay CP to Q7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	5.0 3.5	13.0 9.0	ns
t _{PHL}	Propagation delay MR to Q7	Waveform 2	4.0	6.5	8.5	4.0	9.5	4.0	9.5	ns

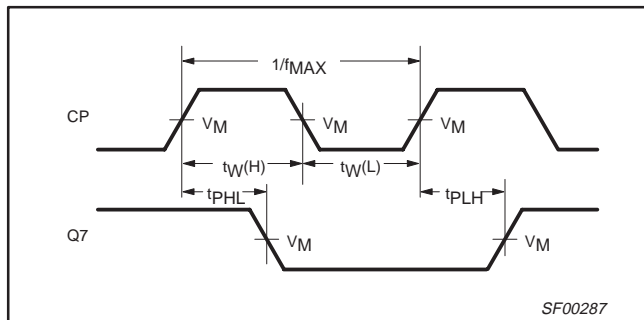
8-bit bidirectional universal shift register

74F166

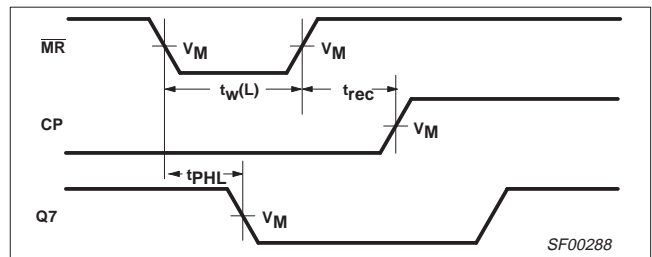
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25^{\circ}C$			$T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$		$T_{amb} = -40^{\circ}C \text{ to } +85^{\circ}C$		
			$V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		$V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
MIN	TYP	MAX	MIN	MAX	MIN	MAX				
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low Dn, Ds to CP, \overline{CE}	Waveform 3	3.0 2.5			4.0 3.0			4.0 3.0	ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn, Ds to CP	Waveform 3	0.0 0.0			1.0 0.0			1.0 0.0	ns
$t_h(H)$ $t_h(L)$	Hold time, high or low Dn, Ds to \overline{CE}	Waveform 3	1.5 0.0			2.0 0.0			2.0 0.0	ns
$t_{su}(L)$	Setup time, low \overline{CE} to CP	Waveform 3	5.0			6.0			6.0	ns
$t_h(H)$	Hold time, high \overline{CE} to CP	Waveform 3	0.0			0.0			0.0	ns
$t_{su}(H)$ $t_{su}(L)$	Setup time, high or low PE to CP, \overline{CE}	Waveform 3	3.0 3.0			4.0 4.0			4.0 6.0	ns
$t_h(H)$ $t_h(L)$	Hold time, high or low PE to CP	Waveform 3	0.0 0.0			0.0 0.0			0.0 0.0	ns
$t_w(H)$ $t_w(L)$	CP pulse width, high or low	Waveform 1	3.0 4.5			3.5 5.0			3.5 6.0	ns
$t_w(L)$	\overline{MR} pulse width, low	Waveform 2	4.0			4.0			4.0	ns
t_{rec}	Recovery time: \overline{MR} to CP	Waveform 2	4.0			4.5			4.5	ns

AC WAVEFORMS



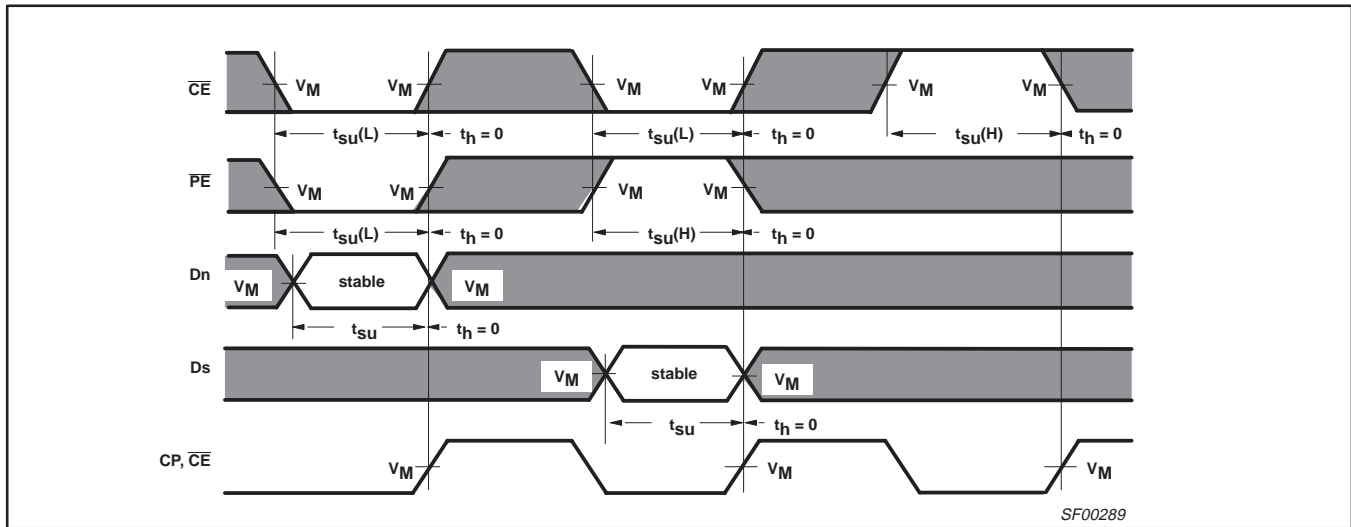
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time

8-bit bidirectional universal shift register

74F166

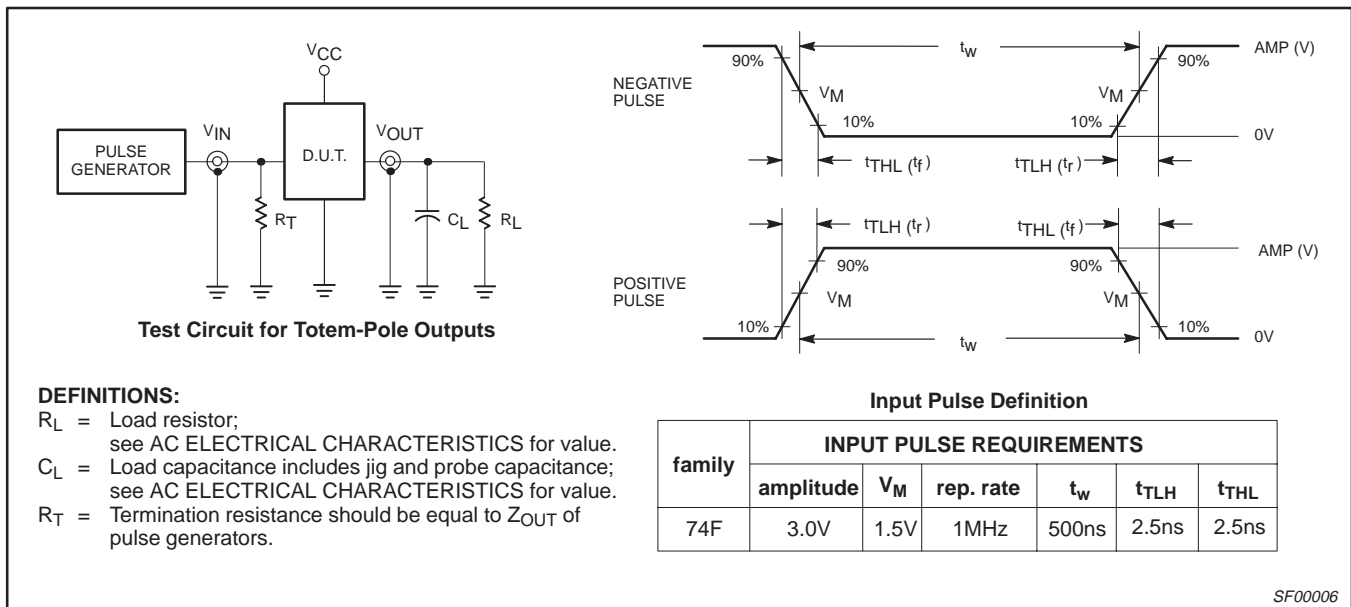


Waveform 3. Setup and hold times

Notes to AC waveforms

1. For all waveforms, $V_M = 1.5V$.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



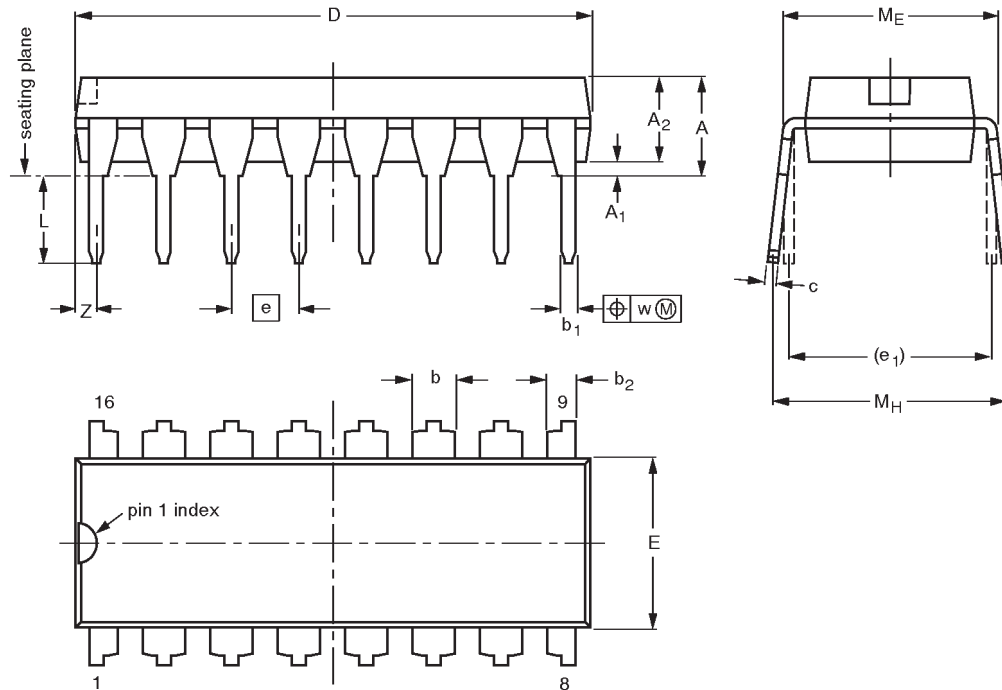
SF00006

8-bit bidirectional universal shift register

74F166

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

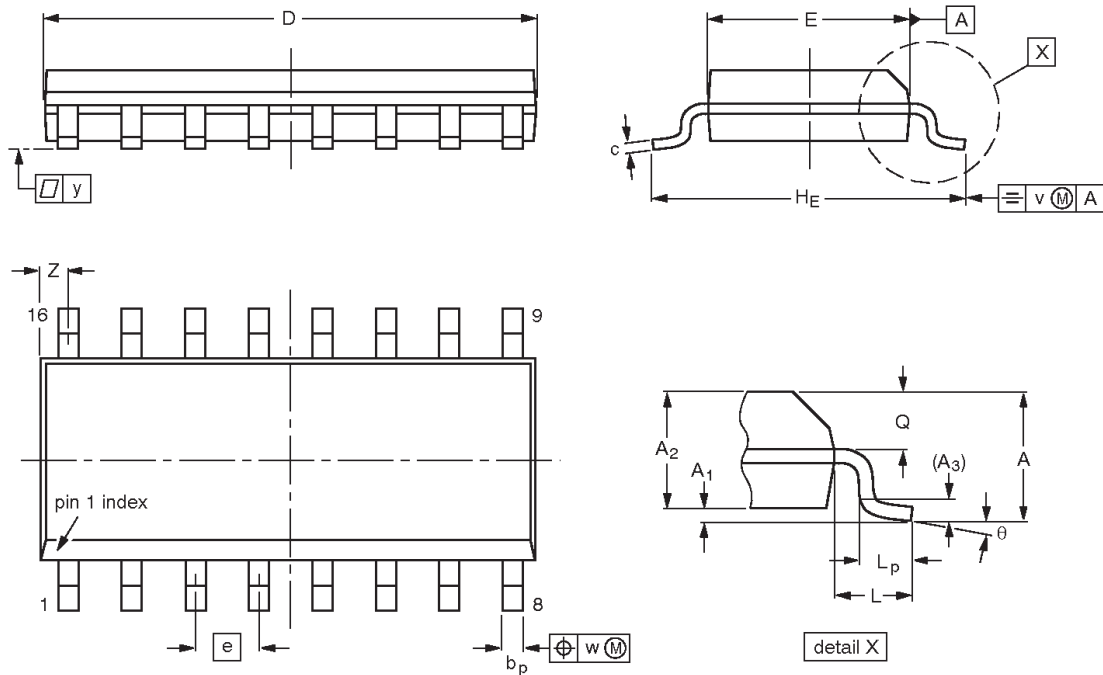
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

8-bit bidirectional universal shift register

74F166

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.25	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

8-bit bidirectional universal shift register

74F166

NOTES

8-bit bidirectional universal shift register

74F166

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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