INTEGRATED CIRCUITS

DATA SHEET

74F08Quad two-input AND gate

Product specification

1995 Apr 19

IC15 Data Handbook

Philips Semiconductors



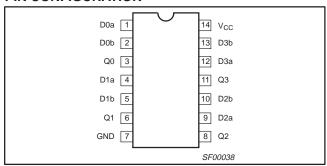


74F08

• 74F08 Available for industrial range (-40°C to +85°C)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F08	4.1ns	7.1mA

PIN CONFIGURATION



ORDERING INFORMATION

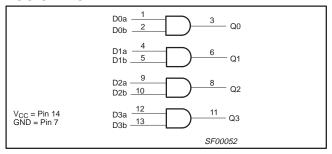
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5.0V $\pm 10\%$, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5.0V $\pm 10\%$, T_{amb} = -40° C to $+85^{\circ}$ C	PKG DWG#
14-pin plastic DIP	N74F08N	174F08N	SOT27-1
14-pin plastic SO	N74F08D	I74F08D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data output	50/33	1.0mA/20mA

 $\textbf{NOTE:} \ \ \text{One (1.0) FAST unit load is defined as: } 20 \mu \text{A in the High state and 0.6mA in the Low state.}$

LOGIC DIAGRAM



FUNCTION TABLE

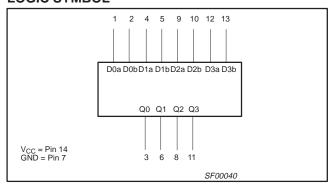
INP	JTS	OUTPUT			
Dna	Dnb	Qn			
L	L	L			
L	Н	L			
Н	L	L			
Н	Н	Н			

NOTES:

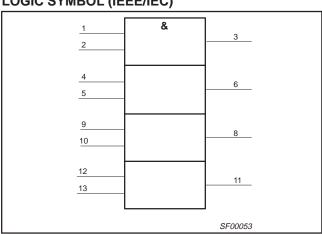
H = High voltage level

L = Low voltage level

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V	
I _{IN}	Input current	-30 to +5	mA	
V _{OUT}	Voltage applied to output in High output state	–0.5 to V _{CC}	V	
I _{OUT}	Current applied to output in Low output state		40	mA
_		Commercial range	0 to +70	°C
T _{amb}	Operating free-air temperature range	Industrial range	-40 to +85	°C
T _{stg}	Storage temperature range	perature range		

RECOMMENDED OPERATING CONDITIONS

CVMDOL	PARAMETER		UNIT			
SYMBOL	PARAMETER	MIN	NOM	MAX	1 00011	
V _{CC}	Supply voltage	4.5	5.0	5.5	V	
V _{Ih}	High-level input voltage	2.0			V	
V _{IL}	Low-level input voltage			0.8	V	
I _{IK}	Input clamp current			-18	mA	
I _{OH}	High-level output current			-1	mA	
I _{OL}	Low-level output current			20	mA	
т.	Operating free-air temperature range	Commercial range	0		+70	°C
lamb	Operating nee-all temperature range	Industrial range	-40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

OVMDOL	DADAMETED		TEST CONDITIO	NO1		LIMITS		
SYMBOL	PARAMETER	FARAMETER		TEST CONDITIONS			MAX	UNIT
V	LP ale leavel and and and to all		$V_{CC} = MIN, V_{IL} = MAX$	±10%V _{CC}	2.5			V
V _{OH}	High-level output voltage		V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4		V
V	VoL Low-level output voltage		$V_{CC} = MIN, V_{IL} = MAX$	±10%V _{CC}		0.30	0.50	V
VOL			$V_{IH} = MIN, I_{OI} = MAX$	±5%V _{CC}		0.30	0.50	V
V _{IK}	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$			-0.73	-1.2	V
I _I	Input current at maximum voltage	input	V _{CC} = MAX, V _I = 7.0V				100	μΑ
I _{IH}	High-level input current		$V_{CC} = MAX, V_I = 2.7V$				20	μΑ
I _{IL}	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$				-0.6	mA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX		-60		-150	mA
la-	Cupply ourrant (total)	I _{CCH}	$V_{CC} = MAX$ $V_{IN} = 4.5V$			5.5	8.3	mA
Icc	Supply current (total)		$V_{CC} = MAX$	V _{IN} = GND		8.6	12.9	mA

NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- 3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

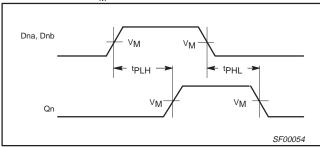
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AC ELECTRICAL CHARACTERISTICS

			LIMITS								
SYMBOL	PARAMETER	TEST CONDITION	$T_{amb} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50pF,$ $R_{L} = 500\Omega$			V _{CC} = +5. C _L =	C to +70°C 0V ± 10% 50pF, 500Ω	T _{amb} = -40° V _{CC} = +5. C _L = : R _L =	UNIT		
			MIN			MIN	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay Dna, Dnb to Qn	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	3.0 2.5	6.6 6.3	2.5 2.5	6.6 6.3	ns	

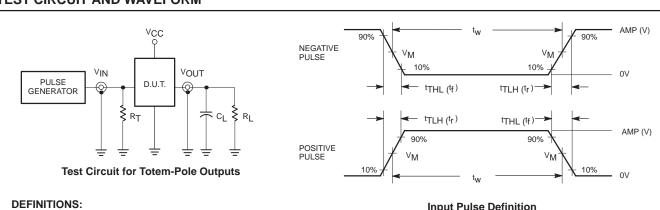
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.



Waveform 1. Propagation Delay for Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM



 R_L = Load resistor;

see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse	Definition
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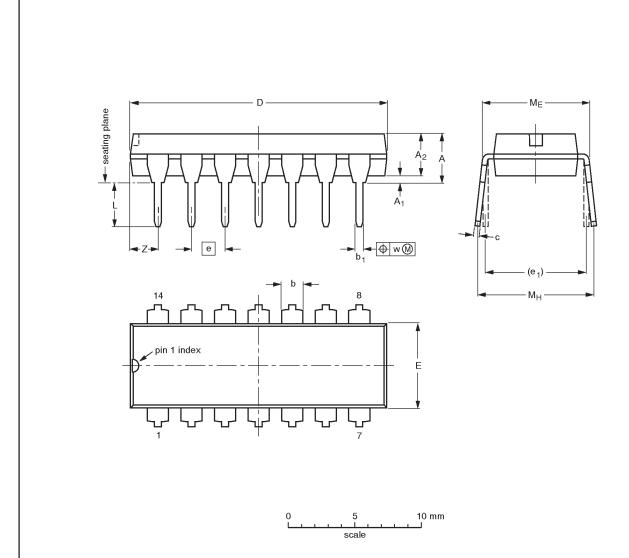
	family	INP	INPUT PULSE REQUIREMENTS									
		amplitude	V _M rep. rate		t _w	t _{TLH}	t _{THL}					
	74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns					

SF00006

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

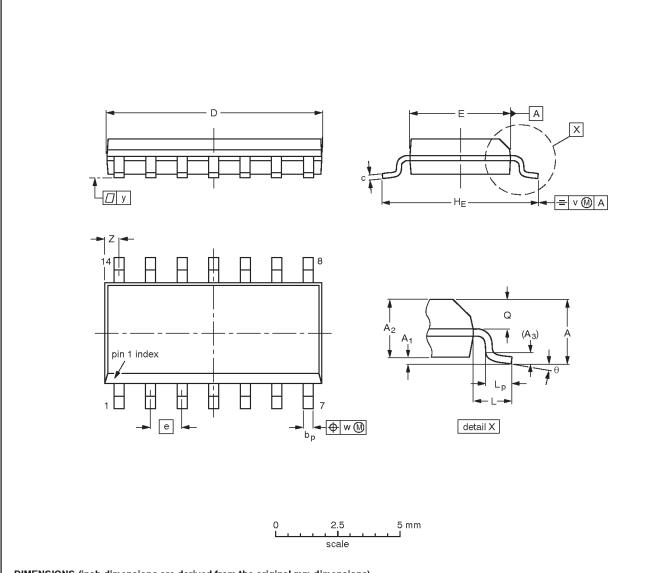
	OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
		IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
	SOT27-1	050G04	MO-001AA			92-11-17 95-03-11	

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT108-1	076E06S	MS-012AB			-95-01-23- 97-05-22	

Philips Semiconductors Product specification

Quad 2-input AND gate

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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^[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code Date of release: 10-98

Document order number: 9397-750-05055

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