PNX8510; PNX8511

Analog companion chip

Rev. 04 – 12 January 2004 Product data

1. General description

The PNX8510; PNX8511 is an analog backend companion chip to digital ICs processing video and audio signals.

The primary difference between the PNX8510 and the PNX8511 is:

- PNX8510 includes the Macrovision™ pay-per-view copy protection system
- PNX8511 does not include Macrovision™

PNX8510/11 provides two video encoders through two standardized D1 interfaces. The encoders can be bypassed to get direct access to the video DACs for higher resolution displays. PNX8510/11 also contains a sophisticated sync raster engine which can be utilized to generate various synchronization patterns for interlaced and non-interlaced image formats. The sync raster engine together with an up-sampling filter and a sync insertion unit compose a complete HDTV-capable data path including tri-level sync generation.

PNX8510/11 also provides two independent pairs of stereo audio DACs with two corresponding I^2S-bus interfaces.

Figure 1 shows the PNX8510/11 with a typical source decoder.

2. Features

2.1 PNX8510

- Six 10-bit video DACs running at up to 135 MHz 1LSB DNL
- Four audio DACs arranged as two stereo pairs
- Two built-in digital video encoders
- PAL B/G, NTSC-M and SECAM encoding
- Two 10-bit D1 inputs with embedded VBI data
- Two I^2S-bus independent audio input ports
- I^2C-bus programmable (slave interface)
- Support for high resolution video out up to 81 MHz interface clock rate
- Support for input modes 2xD1, RGB, 1x 2D1 muxed, 24/30-bit RGB, DD1
- Programmable generation of embedded analog and external digital sync signals compliant to VESA and SMPTE 274 standards
- VBI encoding for standard definition video out

- Teletext insertion for PAL-WST, NTSC-WST, NABTS
- VPS video programming service encoding
- Closed caption encoding
- CGMS copy generation management system according to CPR-1204
- Internal color bar generator for standard definition video out
- JTAG-controlled test signals on video and audio converters
- Macrovision™ pay-per-view copy protection system, rev. 7.1 (SCART support with Macrovision™ copy protection on the RGB lines)

2.2 PNX8511

- PNX8511 has all the features of PNX8510 with the exception of Macrovision™

3. Applications

- Digital Television
- Set-top Box
- Multimedia Applications

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PNX8510HW/B1	HTQFP100	Plastic thermal enhanced thin quad flat package; 100 leads, body 14 x 14 x 1 mm, exposed die pad	SOT638-1
PNX8511HW/B1	HTQFP100	Plastic thermal enhanced thin quad flat package; 100 leads, body 14 x 14 x 1 mm, exposed die pad	SOT638-1

5. Block diagram

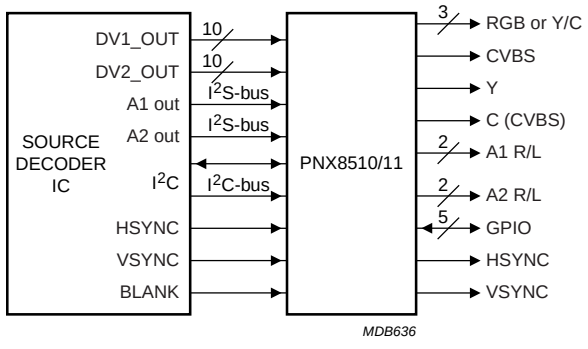


Fig 1. System level diagram

6. Pinning information

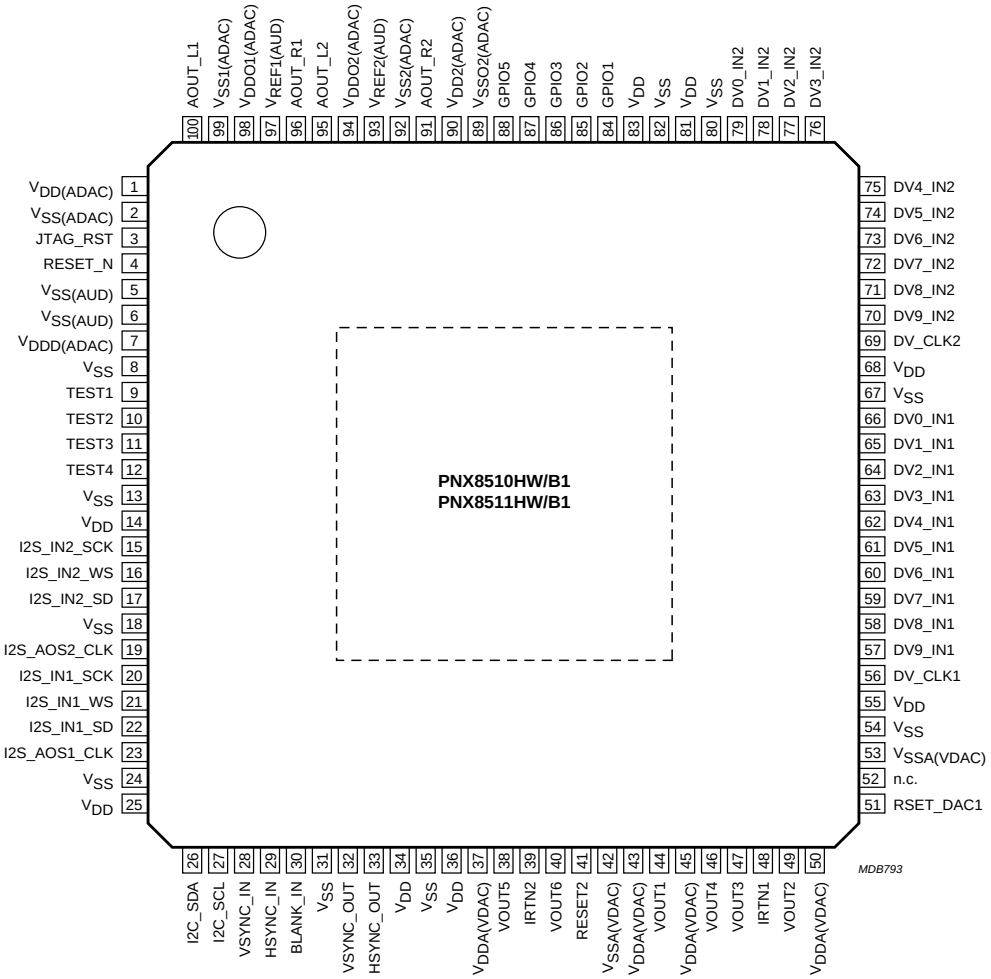


Fig 2. Pin configuration

6.1 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
$V_{DD(ADAC)}$	1	-	Audio DAC analog supply
$V_{SS(ADAC)}$	2	-	Audio DAC analog ground
JTAG_RST	3	-	JTAG reset
RESET_N	4	-	Chip reset in signal (low active)
$V_{SS(AUD)}$	5	-	Audio digital ground
$V_{SS(AUD)}$	6	-	Audio digital ground
$V_{DDD(ADAC)}$	7	-	Audio DAC digital supply
V_{SS}	8	-	Digital ground
TEST1	9	I	JTAG controller test data input
TEST2	10	O	JTAG controller test data output

Table 2: Pin description *...continued*

Symbol	Pin	Type	Description
TEST3	11	I	JTAG controller test clock input
TEST4	12	I	JTAG controller test mode select input
V_{SS}	13	-	Digital ground
V_{DD}	14	-	Digital supply
I2S_IN2_SCK	15	I/O	Bit clock IO for secondary audio channel
I2S_IN2_WS	16	I/O	Word select IO for secondary audio channel
I2S_IN2_SD	17	I	Serial data in for secondary audio channel
V_{SS}	18	-	Digital ground
I2S_AOS2_CLK	19	I	Oversampling clock input for secondary audio channel
I2S_IN1_SCK	20	I/O	Bit clock IO for primary audio channel
I2S_IN1_WS	21	I/O	Word select IO for primary audio channel
I2S_IN1_SD	22	I	Serial data in for primary audio channel
I2S_AOS1_CLK	23	I	Oversampling clock input for primary audio channel
V_{SS}	24	-	Digital ground
V_{DD}	25	-	Digital supply
I2C_SDA	26	I/O	I^2C data line (bi-directional)
I2C_SCL	27	I	I^2C clock line (input)
VSYNC_IN	28	I	Vertical sync input for primary video interface
HSYNC_IN	29	I	Horizontal sync input for primary video interface
BLANK_IN	30	I	Blanking input signal for primary video pipeline
V_{SS}	31	-	Digital ground
VSYNC_OUT	32	O	Vertical sync output for primary video pipeline
HSYNC_OUT	33	O	Horizontal sync output for primary video pipeline
V_{DD}	34	-	Digital supply
V_{SS}	35	-	Digital ground
V_{DD}	36	-	Digital supply
$V_{DDA(VDAC)}$	37	-	Analog supply for video DACs
VOUT5	38	O	Video output for secondary channel, Y/CVBS-DAC
IRTN2	39	-	Current return path for C-DAC and CVBS/Y-DAC
VOUT6	40	O	Video output for secondary channel, C-DAC
RESET2	41	-	Current setting resistor for secondary channel DACs
$V_{SSA(VDAC)}$	42	-	Analog ground for video DACs
$V_{DDA(VDAC)}$	43	-	Analog supply for video DACs
VOUT1	44	O	Video output for primary video DAC 1 (CVBS/Y)
$V_{DDA(VDAC)}$	45	-	Analog supply for video DACs
VOUT4	46	O	Video output for primary video DAC 4 (Blue)
VOUT3	47	O	Video output for primary video DAC 3 (Y/Green)
IRTN1	48	-	Current return path for all primary channel DACs
VOUT2	49	O	Video output for primary video DAC 2 (C/red)
$V_{DDA(VDAC)}$	50	-	Analog supply for video DACs
RSET_DAC1	51	-	Current setting resistor for primary channel DACs

Table 2: Pin description *...continued*

Symbol	Pin	Type	Description
n.c.	52	-	No connection (leave floating)
$V_{SSA(VDAC)}$	53	-	Analog ground for video DACs
V_{SS}	54	-	Digital ground
V_{DD}	55	-	Digital supply
DV_CLK1	56	-	Primary video interface clock
DV9_IN1	57	I	Primary video D1 input
DV8_IN1	58	I	Primary video D1 input
DV7_IN1	59	I	Primary video D1 input
DV6_IN1	60	I	Primary video D1 input
DV5_IN1	61	I	Primary video D1 input
DV4_IN1	62	I	Primary video D1 input
DV3_IN1	63	I	Primary video D1 input
DV2_IN1	64	I	Primary video D1 input
DV1_IN1	65	I	Primary video D1 input
DV0_IN1	66	I	Primary video D1 input
V_{SS}	67	-	Digital ground
V_{DD}	68	-	Digital supply
DV_CLK2	69	-	Secondary video interface clock
DV9_IN2	70	I	Secondary video D1 input
DV8_IN2	71	I	Secondary video D1 input
DV7_IN2	72	I	Secondary video D1 input
DV6_IN2	73	I	Secondary video D1 input
DV5_IN2	74	I	Secondary video D1 input
DV4_IN2	75	I	Secondary video D1 input
DV3_IN2	76	I	Secondary video D1 input
DV2_IN2	77	I	Secondary video D1 input
DV1_IN2	78	I	Secondary video D1 input
DV0_IN2	79	I	Secondary video D1 input
V_{SS}	80	-	Digital ground
V_{DD}	81	-	Digital supply
V_{SS}	82	-	Digital ground
V_{DD}	83	-	Digital supply
GPIO1	84	I/O	General purpose input/output
GPIO2	85	I/O	General purpose input/output
GPIO3	86	I/O	General purpose input/output
GPIO4	87	I/O	General purpose input/output
GPIO5	88	I/O	General purpose input/output
$V_{SS02(ADAC)}$	89	-	Audio DAC output buffer supply
$V_{DD2(ADAC)}$	90	-	Audio DAC supply
AOUT_R2	91	O	Audio output for right secondary audio channel
$V_{SS2(ADAC)}$	92	-	Audio DAC ground

Table 2: Pin description *...continued*

Symbol	Pin	Type	Description
$V_{REF2(AUD)}$	93	-	Audio DAC reference
$V_{DD02(ADAC)}$	94	-	Audio DAC output buffer supply
AOUT_L2	95	O	Audio output for left secondary audio channel
AOUT_R1	96	O	Audio output for right primary audio channel
$V_{REF1(AUD)}$	97	-	Audio DAC reference
$V_{DDO1(ADAC)}$	98	-	Audio DAC output buffer supply
$V_{SS1(ADAC)}$	99	-	Audio DAC ground
AOUT_L1	100	O	Audio output for left primary audio channel

7. Functional description

7.1 Video pipeline

The video pipeline contains two independent video channels. The primary channel is used to display graphic or video content on a standard television, CRT monitor or an HDTV system. The secondary video channel may connect to a VCR or a second standard TV for recording or secondary display purposes. No high definition or RGB output is available through the second video channel.

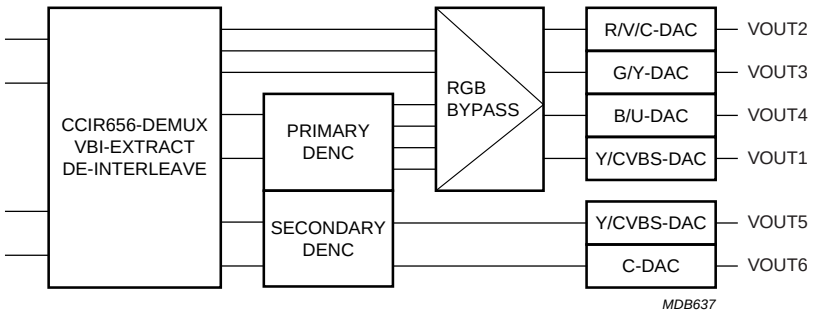


Fig 3. Video path block diagram

The two video pipelines are driven by two standard D1 interfaces, which can operate in various modes in 8 or 10-bit precision. The video modes are described below.

7.1.1 Video modes

The video interfaces and sync raster engines are designed in a generic way. The only limiting factor is the data rate of the received video streams. All formats with a total interface speed requirement below 81 MHz can be displayed by the PNX8510/11.

Table 3: Primary video channel standard interface modes

Interface modes	Mode	Interface speed
4:4:4 RGB or YUV or YCrCb or YPrPb	4:4:4 Muxed Components 10/8-bit	up to 81 MHz
4:2:2 YUV or YCrCb or YPrPb	4:2:2 Muxed components 10/8-bit	up to 81 MHz

Table 4: Primary video channel standard display modes

Display modes	Mode	Interface speed	Used data path
PAL/NTSC/SECAM 4:2:2 YUV i.e. PAL: 864 pixel/line x 312.5 lines/field x 50Hz = 13.5 MHz/Y samples 6.75 MHz/U samples 6.75 MHz/V samples	4:2:2 Muxed components 10/8-bit	27 MHz	SD-CVBS-data path
PAL/NTSC/SECAM RGB/YUV i.e. PAL: 864 pixel/line x 312.5 lines/field x 50 Hz = 13.5 MHz/Y samples 6.75 MHz/U samples 6.75 MHz/V samples	4:2:2 Muxed components 10/8-bit	27 MHz	SD-CVBS and RGB/YUV data paths
2FH PAL/NTSC/SECAM 4:4:4 RGB/YUV/YCrCb/YPrPb i.e. PAL: 864 pixel/line x 312.5 lines/field x 50 Hz x2 = 27 MHz/component	4:4:4 Muxed Components 10/8-bit	81 MHz	HD-data path
480P PAL/NTSC/SECAM 4:4:4 RGB/YUV/YCrCb/YPrPb i.e. PAL: 864 pixel/line x 625 lines/field x 50 Hz = 27 MHz/component	4:4:4 Muxed Components 10/8-bit	81 MHz	HD-data path
Generic D1 mode; the interface clock can run up to 81 MHz, the components can have either 4:2:2 or 4:4:4 color resolution, but must be in the correct color space.	4:4:4 Muxed components/ 4:2:2 Muxed components (use of both D1 interfaces required) 10/8-bit	up to 81 MHz	HD-data path

Table 5: Secondary video channel standard interface modes

Interface modes	Mode	Interface speed
4:2:2 YUV or YCrCb or YPrPb	4:2:2 Muxed components 10/8-bit	27 MHz

Table 6: 24/30-Bit RGB/YUV mode

Both D1 interfaces and the secondary audio channel are combined to provide high-speed direct access to video DACs

Display/interface mode		Mode	Interface speed
Pin assignment 24-bit mode	**Pin assignment 30-bit mode**		
24/30-bit RGB/YUV[1]		24-bit direct RGB/YUV 8/10-bit	up to 81 MHz
red[7] - I²S_IN2_SD	red[9] - I²S_IN2_SD		
red[6] - I²S_IN2_WS	red[8] - I²S_IN2_WS		
red[5] - I²S_IN2_SCK	red[7] - I²S_IN2_SCK		
red[4] - I²S_AOS2_CLK	red[6] - I²S_AOS2_CLK		
red[3] - DV_IN1[9]	red[5] - DV_IN1[9]		
red[2] - DV_IN1[8]	red[4] - DV_IN1[8]		
red[1] - DV_IN1[7]	red[3] - DV_IN1[7]		
red[0] - DV_IN1[6]	red[2] - DV_IN1[6]		
	red[1] - GPIO[5]		
green[7] - DV_IN1[5]	red[0] - GPIO[4]		
green[6] - DV_IN1[4]			
green[5] - DV_IN1[3]	green[9] - DV_IN1[5]		
green[4] - DV_IN1[2]	green[8] - DV_IN1[4]		
green[3] - DV_IN1[1]	green[7] - DV_IN1[3]		
green[2] - DV_IN1[0]	green[6] - DV_IN1[2]		
green[1] - DV_IN2[9]	green[5] - DV_IN1[1]		
green[0] - DV_IN2[8]	green[4] - DV_IN1[0]		
	green[3] - DV_IN2[9]		
blue[7] - DV_IN2[7]	green[2] - DV_IN2[8]		
blue[6] - DV_IN2[6]	green[1] - GPIO[3]		
blue[5] - DV_IN2[5]	green[0] - GPIO[2]		
blue[4] - DV_IN2[4]			
blue[3] - DV_IN2[3]	blue[9] - DV_IN2[7]		
blue[2] - DV_IN2[2]	blue[8] - DV_IN2[6]		
blue[1] - DV_IN2[1]	blue[7] - DV_IN2[5]		
blue[0] - DV_IN2[0]	blue[6] - DV_IN2[4]		
	blue[5] - DV_IN2[3]		
	blue[4] - DV_IN2[2]		
	blue[3] - DV_IN2[1]		
	blue[2] - DV_IN2[0]		
	blue[1] - GPIO[1]		
	blue[0] - DV_CLK2		

[1] In case of the 24/30-bit full parallel input, no secondary audio channel is available.

Table 7: Single interface mode 2 (D1)

Display/interface mode	Mode	Interface speed
Single Interface Mode 2 (D1) Accommodates 2 synchronous multiplexed D1 streams for low cost applications (both streams are extracted).	2x muxed 4:2:2 single D1 8/10-bit	54 MHz

Table 8: Interleaved interface mode

Display/interface mode	Mode	Interface speed
Interleaved interface mode Same formats as in single interface mode 1 and 2 but only one of the two interleaved video streams is extracted per interface. Selection of the extracted slice is possible by software, Usage of two PNX8510/11 chips possible to support up to 4 display/record devices	2x muxed 4:2:2 single D1 or 2x muxed 4:4:4 RGB/YUV 8/10-bit	54 MHz or 81 MHz or pos-neg edge 27 MHz (SAA7128 compliant)

Table 9: Combined double D1 mode

Display/interface mode	Mode	Interface speed
Combined double D1 mode:[1] the two D1 interfaces are combined to carry a single HDTV stream in 4:2:2 YUV or 4:2:2 YPrPb format primary D1: Y channel secondary D1: muxed UV or PrPb channel i.e.: 1920x1080 60 Hz interlaced 2200 pixel/line x 562.5 lines/field x 60 Hz = 74.25 MHz/Y samples 37.125 MHz/Cr/Pr samples 37.125 MHz/Cb/Pb samples	2 combined D1 8/10-bit	up to 81 MHz per D1

[1] In case of the combined double D1 mode, no secondary display channel is available

The PNX8510/11 supports color space conversion only in the primary RGB standard definition data path. For the high definition part of the primary video data path and for the secondary video data path no color space conversion is available. Hence the video data has to be provided in the display destination color space.

Aside from built-in video encoders, which generate all necessary timing and filtering for an appropriate sync raster for PAL, NTSC and SECAM, the PNX8510/11 contains a separate raster-generation engine which also supports but is not limited to the HD-formats, such as the SMPTE 274M. The PNX8510/11 also contains an up-sampling filter to convert 4:2:2 formats (other than standard definition formats) to 4:4:4.

In the case of combined double D1 mode, no secondary display channel is available.

If the interface is operated in D1 mode, the data stream presented to the interface has to be D1 compliant i.e., the maximum and minimum codes (8-bit 0x00 0xFF, 10-bit 0x000 0x3FF) must not occur during active video.

A detailed description of video input data formats can be found in Section 7.1.2. The video modes listed correspond to the settings of the DEMUX_MODE bits in the register 0x95 VMUXCTL Section 8.1. If the video interface clock frequency is not equivalent to the processing and the video DAC operation frequency the appropriate divider registers in the audio/clock register section have to be programmed. As a general rule the settings in Table 10 should be used:

Table 10: Clock frequency settings

Mode	Interface clock	Processing clock	DAC clock
4:2:2 YUV SD Single Interface Mode	27 MHz	27 MHz	27 MHz
4:4:4 RGB 2FH Single Interface Mode	81 MHz	27 MHz	27 MHz
4:2:2 YUV 1080i Double Interface Mode	74.25 MHz	74.25 MHz	74.25 MHz

7.1.2 Video input modes

The PNX8510/11 video interface supports a wide variety of video formats. The video interface is designed in a generic fashion. It is de-coupled from the actual video data paths in the system and imposes only a few restrictions on the video data streams provided to the chip.

This section explains the possible video stream formats and provides details on synchronizing the PNX8510/11 with respect to a particular video data format.

The PNX8510/11 accepts the video formats shown in Figure 4 to Figure 10 on a single interface with up to 81 MHz interface clock:

YUV 4:2:2

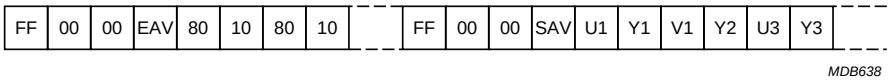


Fig 4. YUV 4:2:2

This is the CCIR-656 compliant format and will mainly be used at an interface speed of 27 MHz to feed the video encoder modules in the chip.

This is the standard interface format for the secondary video encoder pipeline unless the chip is used in High Definition (HD) mode.

The YUV 4:2:2 format can also be used to feed the HD data path as long as the pixel clock rate stays below 81 MHz. To operate the HD data path with 4:2:2 source material the 4:2:2 to 4:4:4 filter should be enabled to achieve the best video quality.

RGB 4:4:4

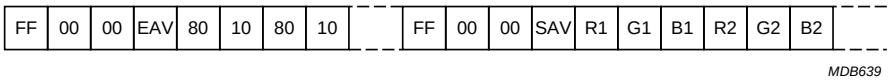


Fig 5. RGB 4:4:4

This mode is only useful if the HD data path in the PNX8510/11 is in operation. The RGB 4:4:4 interface mode is not applicable to the standard definition RGB path operation due to the implicit clocking requirements. The data rate for standard definition RGB 4:4:4 data would be 13.5 MHz per component resulting in an interface speed of 40.5 MHz. Because the chip does not contain any PLLs, it is not possible to extract 27 MHz out of the interface clock.

YUV 4:4:4

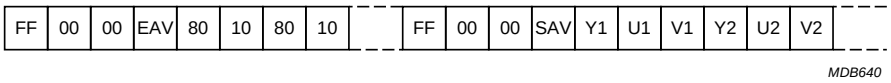


Fig 6. YUV 4:4:4

This mode is useful only if the HD data path in the PNX8510/11 is in operation.

YUV 4:2:2 Interleaved

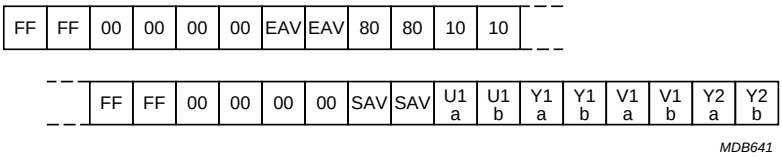


Fig 7. YUV 4:2:2 Interleaved

This mode supports two video data streams through one physical video interface. It can be used to utilize both video encoder channels in the chip with one interface only or to hook up two PNX8510/11 devices to one source providing an interleaved data stream. Each chip extracts one slice from the interleaved stream. This video format is useful for the encoder standard definition data path only.

RGB 4:4:4 Interleaved

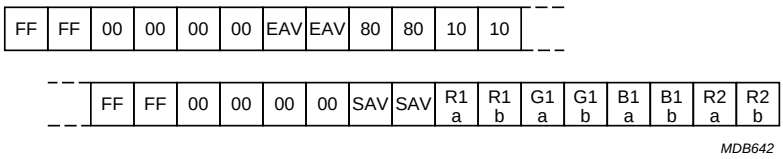


Fig 8. RGB 4:4:4 Interleaved

This mode supports two video data streams through one physical video interface. It can be used to utilize both video encoder channels in the chip with one interface only or to hook up two PNX8510/11 devices to one source providing an interleaved data stream. Each chip extracts one slice from the interleaved stream. This video format is useful for the standard definition RGB data path as well as for the HD data path.

YUV 4:4:4 Interleaved

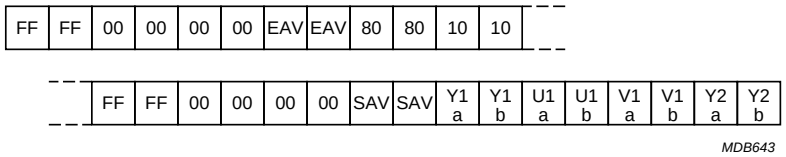


Fig 9. YUV 4:4:4 Interleaved

This mode supports two video data streams through one physical video interface. It can be used to utilize both video encoder channels with one interface only or to hook up two PNX8510/11 devices to one source providing an interleaved data stream. Each chip extracts one slice from the interleaved stream. This video format is useful for the HD data path only.

There are two modes defined for interleaved data streams. One is to run the interface at twice the speed and provide a qualifier on the HSYNC input to qualify a certain slice. The qualifier is essentially the interface clock divided by two.

The other interleaved interface format works on both clock edges of the interface clock, so one slice is latched at the positive edge and the other slice is latched at the negative edge of the interface clock.

YUV 4:2:2 HD two-channel format

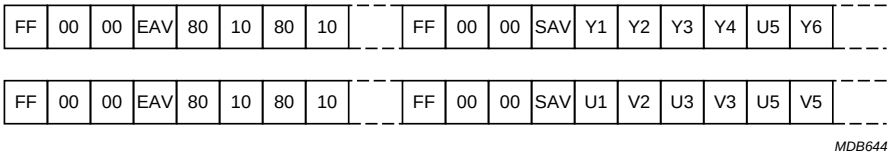


Fig 10. YUV 4:2:2 HD two-channel format

This format is used only for high definition video modes that exceed interface clock requirements of 81 MHz. For this video interface mode, both physical interfaces of the chip are utilized. The primary interface gets a D1-like data stream, which only contains the luminance information, while the secondary D1 interface carries the chrominance information.

7.1.3 Video input module

The video input module is responsible for accommodating all supported video data formats. It delivers a de-multiplexed and de-sliced data stream to the video processing modules.

As depicted in Figure 11, the IC has two video input ports which can accommodate 8 or 10-bit wide video data streams.

The normal mode of operation is that the DV1 interface is routed to the primary video data paths and the DV2 interface is routed to the secondary video data paths. The IC however accepts also so called sliced data formats. A sliced data format contains two single video data streams multiplexed together on a component basis. A more detailed description of the arrangement of the components can be found in Section 7.1.2. To enable sliced data formats the SLICE_MODE bit of the register VMUXCTL (register offset 0x95) has to be set.

The De-Slice module essentially takes the two data streams apart by simply two to one de-multiplexing. The routing of the resulting two video data streams is determined by setting the SEL register bits in the primary and secondary video data path apertures appropriately. Sliced data formats come in two different flavors: double edge and qualified.

The double edge slice format has data changes on the positive and the negative clock edge where as the qualified mode qualifies one data stream of the two multiplexed ones with an active high on the HSYNC signal. To use this mode the USE_QUALIFIER bit in the register INPCTL (offset 0x3A) must be set. The order of the slice qualification can be changed by setting the QUAL_INVERT bit of the same register (offset 0x3A).

Since each of the video input interfaces can accept sliced data formats a total of four video data streams could be routed into the IC and two of them can be selected to be forwarded to the primary and the secondary video display pipeline.

The structure of the video input module is shown in Figure 11.

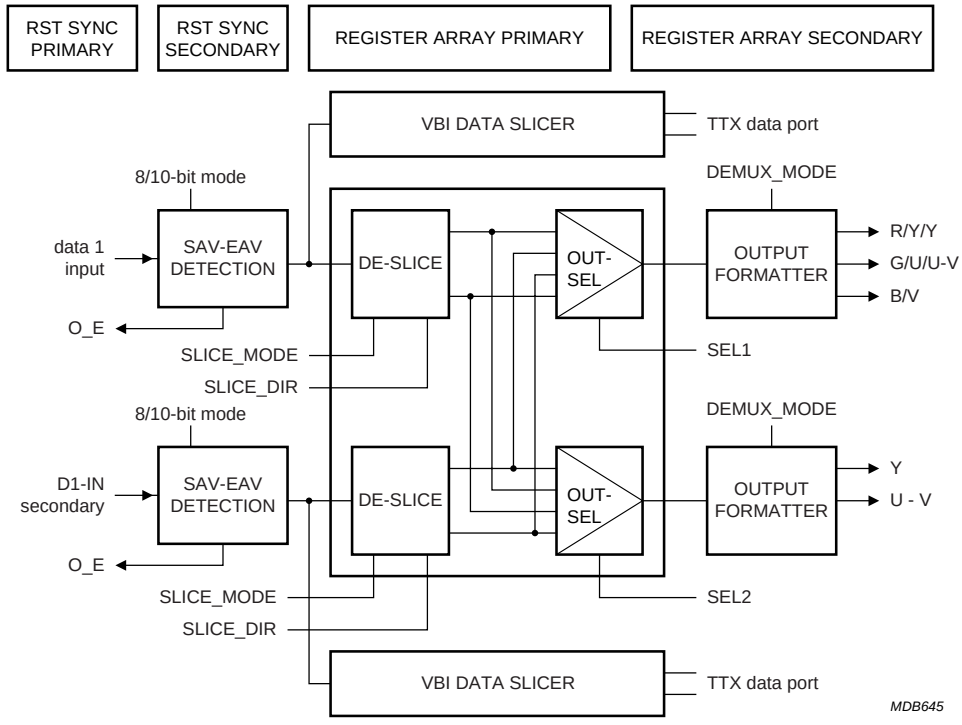


Fig 11. Block diagram - video input module

7.1.4 Video DAC control

The PNX8510/11 contains six video DACs, four dedicated to the primary video pipeline and two to the secondary video processing path.

The first DAC of the primary video channel (VOUT1) is always assigned to the primary standard definition data path. The output of the DAC can be changed from CVBS to Y by resetting the CVBSEN bit of the register DACCTRL (offset 0x2D) to zero.

The second DAC of the primary video channel (VOUT2) is assigned to either the standard definition (SD) data path or High Definition (HD) data path. In the SD mode, it carries the chrominance, C (Y/C operation) if the CEN bit in the DACCTRL (offset 0x2D) is set or the Red/V channel (RGB/Component mode operation) if the CEN bit of the DACCTRL (offset 0x2D) is reset. In HD mode (SD_HD bit of INPCTL register, offset 0x3A is set to zero) this DAC carries either the Red channel or the Y channel depending on whether the HD path is operated in RGB or YUV mode. Note that the CEN bit must be reset for HD operation.

The third DAC of the primary video channel (VOUT3) is also assigned to either the standard definition (SD) data path or High Definition (HD) data path. In SD mode, it carries the luminance channel if the VBSEN bit in the DACCTRL (offset 0x2D) is set or the Green/Y channel if the VBSEN bit is reset (RGB/Component mode operation). If the high definition data path is operational (SD_HD=1’b0) this DAC carries the Green or U channel depending on whether the HD path is operated in YUV or RGB mode.

The configuration of the fourth DAC in the primary video data path (VOUT4) can not be changed with a programming register. This DAC carries the Blue or U channel in standard definition mode and the Blue or V channel if the high definition data path is active.

The configuration of the DACs for the secondary video data path is limited to the CVBS/Y DAC (VOUT5). If the CVBSEN bit in the DACCTRL register (offset 0x2D) is set, this DAC carries the CVBS signal. Resetting the bit results in the Y signal being assigned to this DAC.

The second DAC of the secondary video pipeline (VDAC6) always carries the chrominance signal.

7.1.5 VBI data

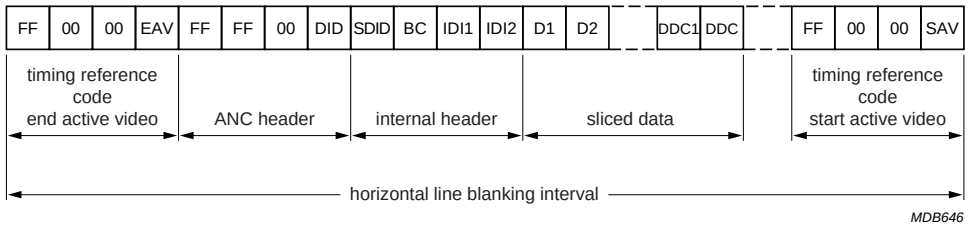
VBI data extraction from a D1 data stream is only supported for standard definition formats. The extraction follows the concept of Philips video decoders, such as the SAA7114. Both video interfaces can carry VBI data information. The content of the VBI data is entirely determined by the source decoder chip software driver.

The PNX8510/11 supports two VBI data streams. The limitation to two VBI data streams implies certain limitations when using multiple PNX8510/11 chips in a system. In this case one PNX8510/11 gets either one or two (all) VBI data streams. The other PNX8510/11 IC would get one or none.

Only the ANC/SAV-EAV header style VBI data encoding mode is supported in the PNX8510/11. According to these standards VBI data is always inserted in the horizontal blanking interval of a line. The data is preceded by an ANC header which is

programmable. An internal header following the ANC contains a programmable sliced data identifier with the number of data bytes transmitted and two internal identification tokens containing data type, field type and line number. Figure 12 illustrates how the data is encoded in the horizontal blanking interval.

Remark: In standard definition mode, only 8 of the 10 available signal lines of the D1 interface are used. The two LSB lines are fixed to zero.



See Table 11 to Table 16for code description

Fig 12. ANC VBI data insertion in D1

Table 11: VBI header/data codes

Name	Function
SAV	start of active video
DID	data identifier: ignored, has to be set to 0x11h
SDID	sliced data identification: ignored, has to be set to 0x11h
BC	byte count describes the number of succeeding decoded data bytes
IDI1	internal data identification 1: OP, FID, LineNumber[8:3]
IDI2	internal data identification 2: OP, LineNumber[2:0], Data Type
D1-Ddc	data bytes
EAV	end of active video

Table 12: VBI data header format

LN = Line Number, BC = Byte Count, DT = Data Type

Code	D9	D8	D7	D6	D5	D4	D3	D2
SDID	1	1	1	1	1	1	1	1
DID	1	1	1	1	1	1	1	1
BC	-	-	BC5	BC4	BC3	BC2	BC1	BC0
IDI1	-	field ID 0=field 1 1=field 2	LN8	LN7	LN6	LN5	LN4	LN3
IDI2	-	LN2	LN1	LN0	DT3	DT2	DT1	DT0

Table 13: SAV/EAV codes NTSC

Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-19	0	1	1	0
20-263	0	0	1	0

Table 13: SAV/EAV codes NTSC*...continued*

Line Number	F	V	H (EAV)	H (SAV)
264-265	0	1	1	0
266-282	1	1	1	0
283-525	1	0	1	0

Table 14: SAV/EAV codes PAL

Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

Table 15: SAV/EAV sequence

SAV/EAV	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
status word	1	F	V	H	P3	P2	P1	P0	0	0

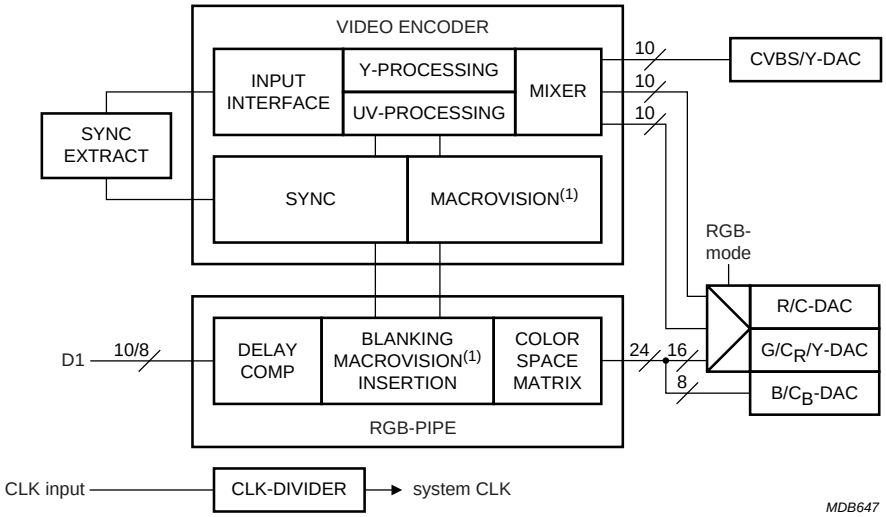
[1] P0 to P3 are protection bits and calculated in the following way:
P3=V^H, P2=F^H, P1=F^V, P0=F^V^H

Table 16: Supported data types

Data Type	Standard
0000	Teletext EuroWST
0010	VPS video programming service
0011	WSS wide screen signalling
0100	closed caption
1100	US NABTS
1111	Programming (SubAddr1-Data1-SubAddr2-Data2...)

7.1.6 Primary video channel

Figure 13 illustrates the different modes of operation for the primary video channel.



Standard definition operating mode

Fig 13. Primary display pipe

PNX8510/11 supports color space conversion only in the primary RGB Standard definition data path. The fixed coefficients of this color space matrix are as follows:

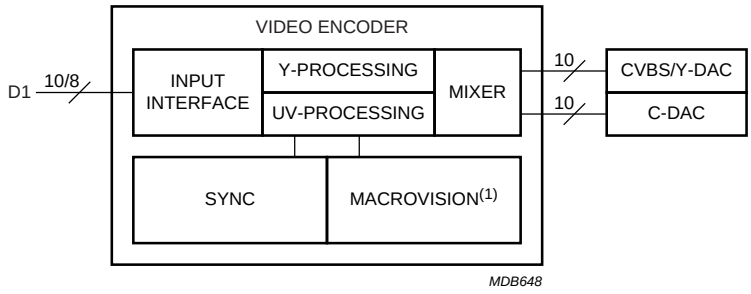
R = Y + 1.371 x Cr

G = Y - (0.336 x Cb + 0.698 x Cr)

B = Y + 1.732 x Cb

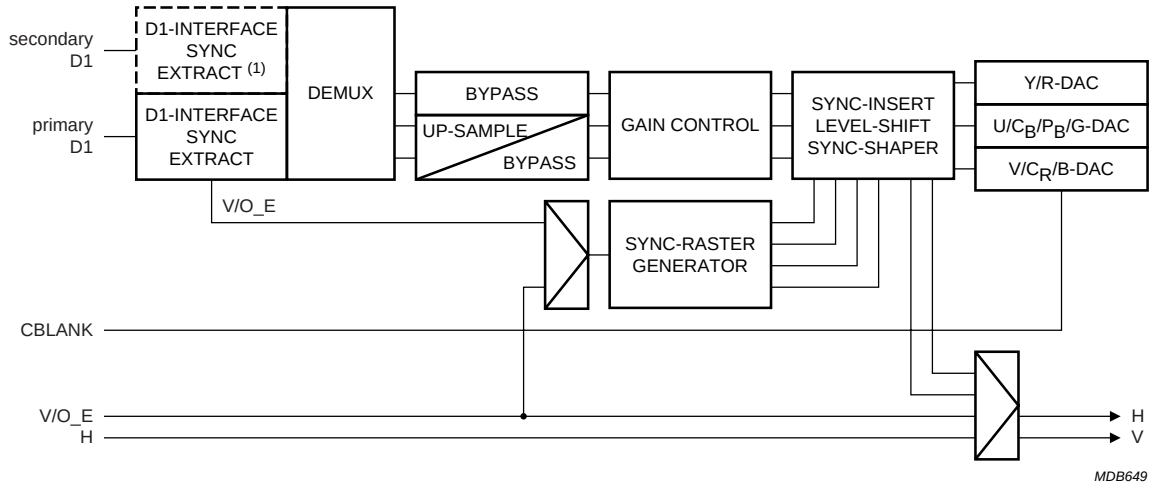
7.1.7 Secondary video channel

The secondary display consists of the Y and UV processing data path of a video encoder only. The synchronization information will be extracted from the incoming D1 data stream. The structure of the secondary display pipe is shown in Figure 14.



Standard definition operating mode

Fig 14. Secondary display pipe



HD operation mode

Fig 15. Primary display pipe

7.1.8 PAL/NTSC/SECAM encoder

The PAL/NTSC/SECAM encoder accepts the YUV data and encodes it into an NTSC, PAL or SECAM video signal. From Y, U and V data, the encoder generates luminance, chrominance and subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (offset is programmable to enable different black level setups). In order to enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and the blanking period. Chrominance is modified in gain (programmable separately for U and V). The standard dependent burst is inserted before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate.

One of the interpolation stages can be bypassed providing a higher color bandwidth, which can be used for Y and C output. The register bits FSC0 to FSC3 set the subcarrier frequency. To make sure the subcarrier is locked to the line frequency, as the standards require, the sync generator is able to reset the subcarrier generation periodically. This feature is controlled by the PHRES (register MULTICTL, offset 0x6E) programming bits. These features are available to generate a standard interlaced signal; they will not work in non-interlaced mode.

A crystal-stable master clock of 27 MHz, which is twice the CCIR line-locked pixel clock of 13.5 MHz, is received from the interface clock pins. The encoder synthesizes all necessary internal signals, color subcarrier frequency, and synchronization signals from that clock.

For ease of analog post filtering, the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

Programming flexibility includes NTSC-M, PAL-B, SECAM main standards as well as other variations. A number of possibilities are provided for setting different video parameters, such as:

- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude

The sync generator generates all the signals required to control the signal processing, provide the composite sync signal, insert the color burst, etc.

The encoder includes a cross-color reduction filter to reduce cross talk between the luminance and chrominance channels. In the CVBS signal, the signal amplitude is reduced by 15/16 to avoid overflow.

7.1.9 Luminance and Chrominance Processing

The Y processing provides a high performance 5 MHz lowpass filter. It adjusts the level range according to the standard and inserts the sync and blanking pulses. The insertion stage generates the correct pulse shapes. No further processing is necessary of the D/A converters for this purpose.

Chroma processing operates on the baseband signals as long as possible. At first, the signal amplitudes are adjusted and the burst is inserted. Afterwards the signals are passed through a 1.4 MHz lowpass filter. This filter can be switched to a higher cut-off frequency to allow more chroma bandwidth with S-Video. The quadrature modulator uses a DTO (Discrete Time Oscillator) with 32-bit resolution for the subcarrier generation. Even with this high resolution, the DTO cannot generate the carrier locked to the line frequency as the standards require without further means. So the sync generator is able to reset the DTO periodically. This feature is controlled by the PHRES programming bits. These modes may only be switched on if the encoder is programmed to generate a standard signal; they will not work in non-interlaced mode.

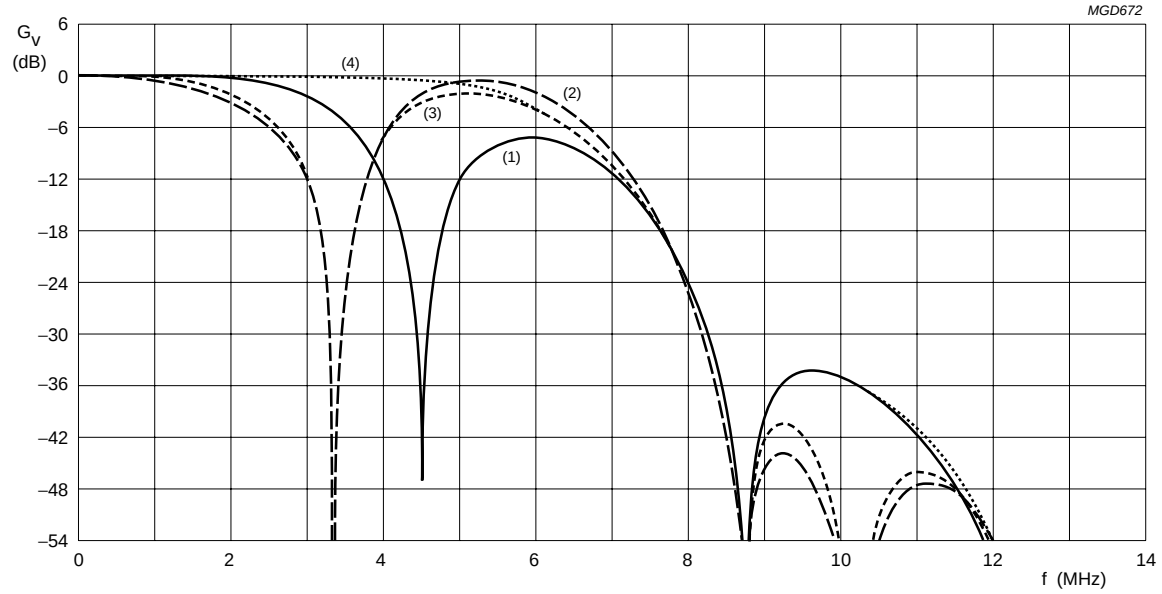


Fig 16. Luminance transfer characteristic 1

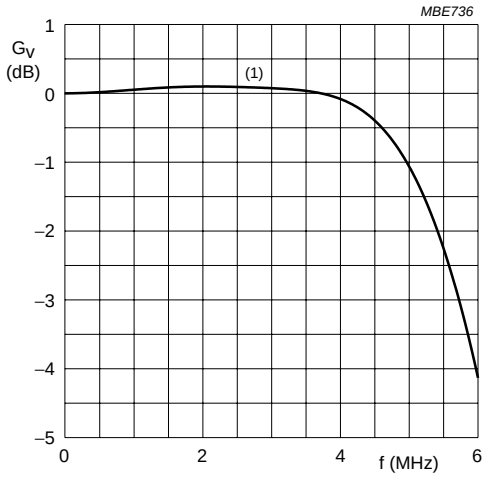


Fig 17. Luminance transfer characteristic 2

Table 17: Luminance transfer characteristics

Register CCRS, offset 0x5f defines the luminance transfer characteristics

CCRS	Luminance Transfer Characteristics
01	(1)
10	(2)
11	(3)
00	(4)

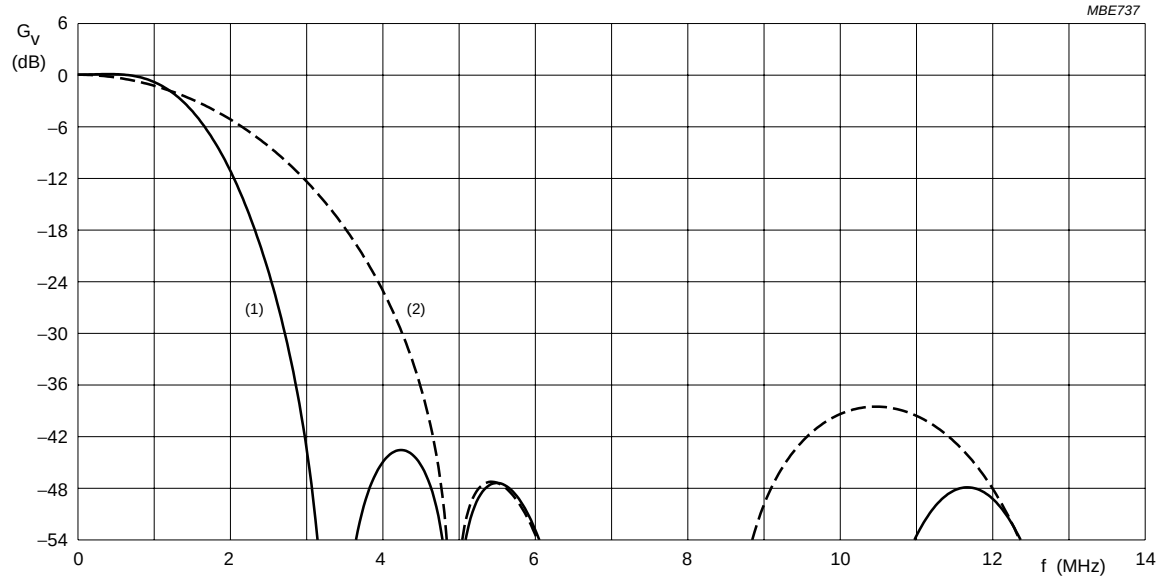


Fig 18. Chrominance transfer characteristic 1

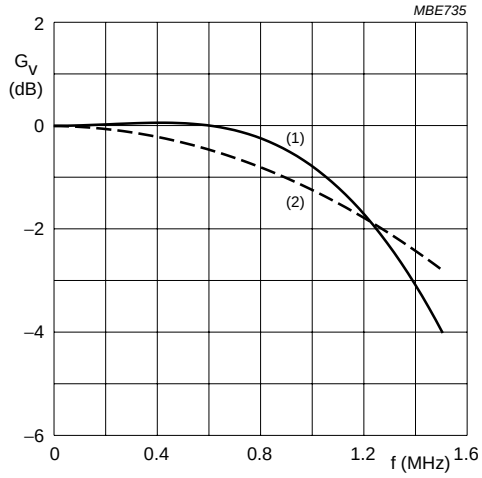


Fig 19. Chrominance transfer characteristic 2

Table 18: Chrominance transfer characteristics

Register SCBW, offset 0x61 defines the chrominance transfer characteristics

SCBW	Chrominance Transfer Characteristics
1	(1)
0	(2)

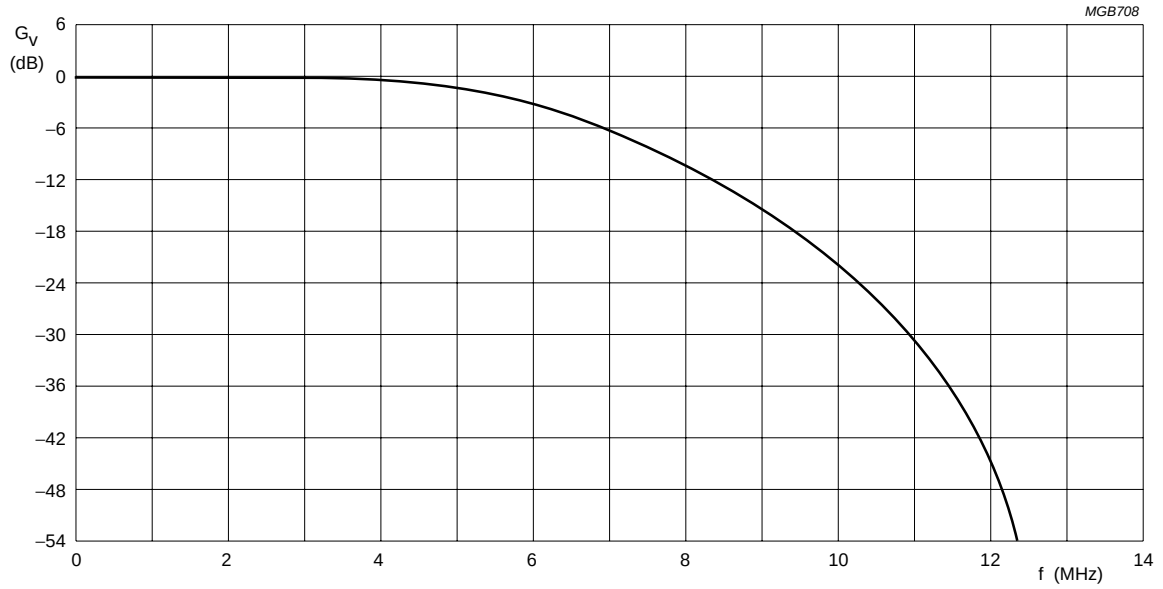


Fig 20. Luminance transfer characteristic in RGB

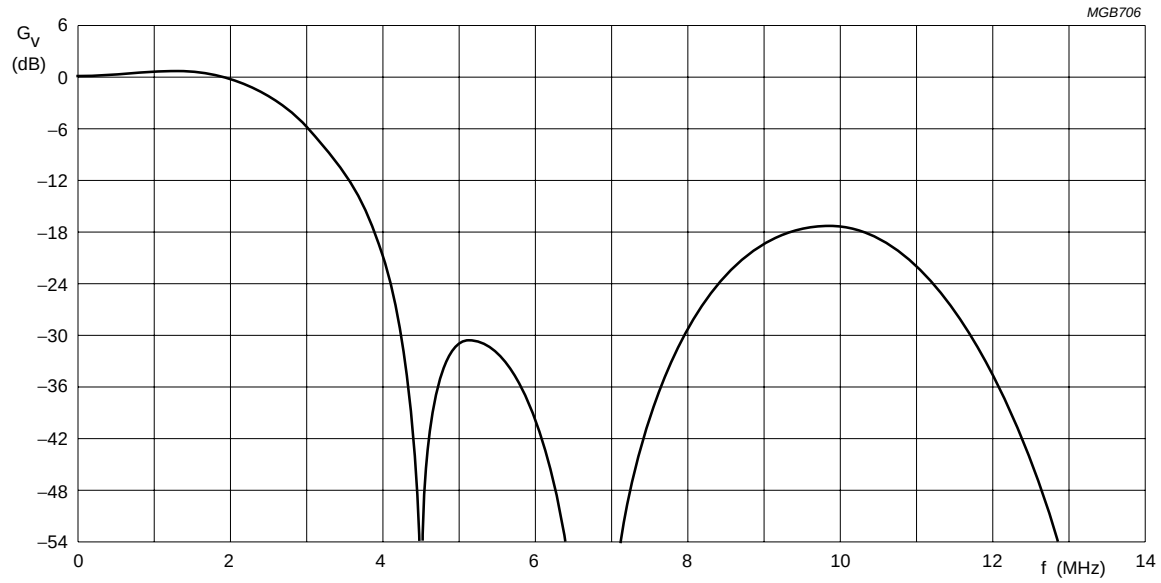


Fig 21. Color difference transfer characteristic in RGB

7.1.10 Sync generator

The sync generator is the timing master of the encoder. It generates all the signals required to control the signal processing, provide the composite sync signal, insert the color burst, etc. Via the FISE control bit (register STDCTL, offset 0x61), the circuit can be set to generate 50 Hz patterns for e.g., PAL B or 60 Hz patterns (NTSC M). It is possible to modify the number of lines per field by ±0.5 lines to generate a non-interlaced output signal. The sync generator also provides HS (Horizontal Sync), VS (Vertical Sync) and O_E (Odd/Even) signals to control the rest of the encoder.

7.1.11 Macrovision™ - PNX8510

The encoder supports Macrovision™ Anti-Taping for both NTSC and PAL. There is no Macrovision™ insertion for SECAM defined, however for AGC Pseudo Sync and BP pulses the same settings used for PAL could be used for SECAM. The different steps of this process can be programmed separately. The Macrovision™ control block provides all necessary timing and level information for inserting the correct pulses in the CVBS/Y/C/RGB/YUV data stream. Furthermore it provides the signals used to modify the subcarrier generator according to the Macrovision™ Burst Inversion requirements.

The encoder uses a blanking level during the vertical blanking interval that is defined by the value of BLNVB, thus providing two different programmable blanking levels. Outside vertical blanking, value of BLNNL is effective, which should be reduced according to Macrovision™ requirements. The copy protection means can be activated independently by the respective control bits. The Macrovision™ registers and definition of each of these registers are defined in a separate Macrovision™ Supplement document.

Remark: Macrovision™ is not available in PNX8511.

7.2 HD data path

The high definition data path of the PNX8510/11 IC features an up-sampling filter, gain control and a universal sync insertion engine.

Input formats supported by the high definition data path are:

- Double D1 mode:16/20 bit 422 (8/10 bit for Y and 8/10 bit for U/V); DEMUX_MODE of Register VMUXCTL, offset 0x95 is set to 3’b011
- Single interface HD 422 mode (UYVY 422 D1 format); DEMUX_MODE of Register VMUXCTL, offset 0x95 is set to 3’b100
- Single interface 444 (RGB/YUV 444 format); DEMUX_MODE of Register VMUXCTL, offset 0x95 is set to 3’b001
- Full 24/30 bit parallel input mode (YUV/RGB 444 formats); VMODE of Register MISCCTRL, offset 0xA5 is set to zero

RGB and YUV data types are accepted. However, there is no color space conversion in the HD data path so the input data type has to match the display data type.

The up-sampling filter can be applied to convert incoming 422 data formats to 444.

The data path also provides individual gain control for RGB/YUV which allows a +/-0.5x amplitude change (HD_GAIN_RY, HD_GAIN_GU, HD_GAIN_BV control registers).

The HD sync insertion module following the filter and gain control circuits provides flexible insertion of synchronization signals into the Y, Y and V or R, G and B data paths. The insertion can be chosen on a component basis (Y/R_SYNC_INS_EN, U/G_SYNC_INS_EN, V/B_SYNC_INS_EN control registers) and the sync generator provides individual tables for the components. A more detailed description of the sync generator can be found in the next paragraph.

7.2.1 HD-sync generator module

This section describes the operation and programming of the high definition (HD) video data path sync unit.

The module's purpose is to provide the video data path that bypasses the digital video encoders with the appropriate synchronization pattern. The module design provides maximum flexibility in terms of raster generation for all interlaced and non-interlaced ATSC formats. The sync engine is capable of providing a combination of event-value pairs which can be used to insert certain values at specified times in the outgoing data stream. It can also be used to generate digital signals associated with time events. They can be used as digital Horizontal and Vertical synchronization signals.

The sync raster generation is fully programmable to accommodate different requirements. The raster generation can be either progressive or interlaced. Digital sync signal generation (Horizontal, Vertical and Blank) as well as analog embedded sync generation are supported. The picture position is adjustable through the programmable relation between the sync pulses and the video contents.

The generation of embedded analog sync pulses is bound to a number of events which can be defined for a line. Several of these line-timing definitions can exist in parallel. For the final sync raster composition a certain sequence of lines with different sync event properties has to be defined. The sequence specifies a series of line types and the number of occurrences of this specific line type.

After the sequence has completed, it restarts from the beginning. In this way, the sync raster generation is generic and can be adopted to different standards (different sync shapes, various H-timing, interlaced, progressive...). However, to generate a stable picture, it is important that the sequence fits precisely to the incoming data stream in terms of the total number of pixels per frame.

The sync engine's flexibility is achieved by using a sequence of linked lists carrying the properties for the image, the lines as well as fractions of lines. The list dependencies are illustrated in Figure 22.

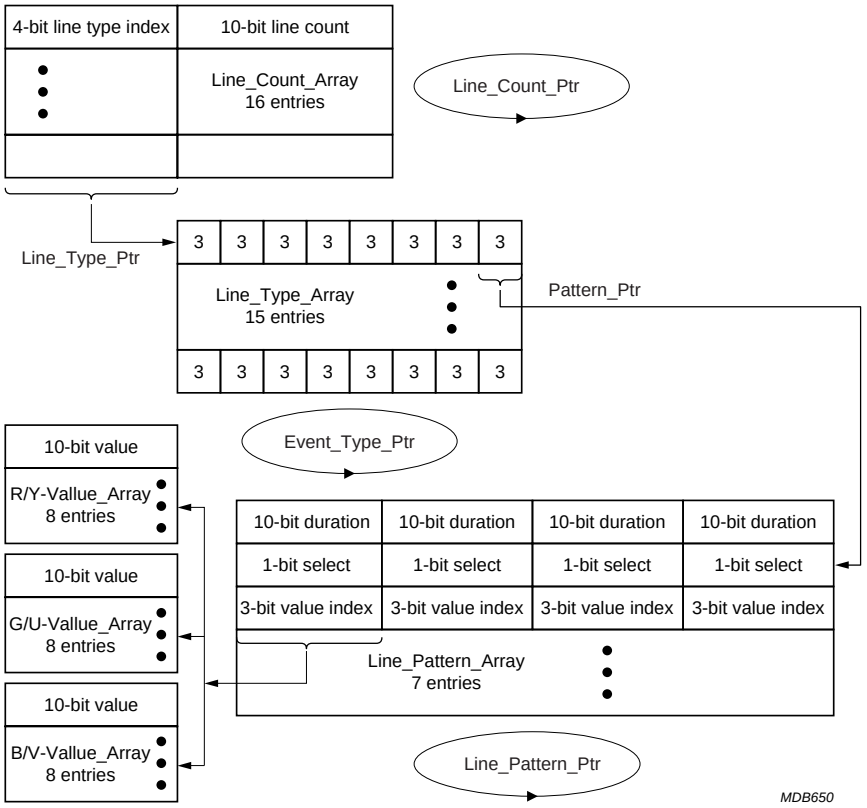


Fig 22. Sync engine list dependencies

The first table is called “Line_Count_Array” and serves as an array to hold the correct sequence of lines composing the synchronization raster. It can contain up to 16 entries. Each entry holds a 4-bit index (counted from 1 through 16)) and a 10-bit counter value.

The 4-bit index is a pointer to a line in the next table called “Line_Type_Array.” A 10-bit counter value specifies how often this particular line is repeated. If the necessary line count for a particular line exceeds the 10 bits, it has to use two table entries. This table has to be terminated with a dummy entry containing a ‘0’ index and ‘0’ line count.

The second table, “Line_Type_Array” holds up to 15 entries (counted from 1 through 15). Each entry can contain up to eight index pointers which point to another table called, “Line_Pattern_Array.” These pointers represent parts of a line raster. A line may be split up into a sync, a blank and an active portion followed by another blank portion, which would require four index pointers in one entry of the table. It is possible to have less than eight index pointers in any entry, in which case those index pointers should be filled with ‘0.

The third table is called “Line_Pattern_Array” and it can contain a maximum of seven entries (counted from 1 though 7). The entries are used to define portions of a line representing a certain value for a certain number of clock cycles. Each of these seven entries can store up to four groups of “duration, select and value index.” It is possible to have less than four groups in any entry, in which case those groups should be filled

with 0. ”Duration” is a 10-bit value representing the number of clock cycles. “Select” indicates whether the value is actually inserted into the video data stream or not. “Value index” is a 3-bit index into the next table in the linked list called “Value array.” Certain bits of the “value index” can also be used to generate a digital sync raster provided at the H- and V-sync outputs of the PNX8510/11.

“Value array” can hold up to 8 values (counted from 0 though 7) which are 10-bit signed 2’s complement.

7.2.2 Trigger generation

To ease the trigger setup for the sync generation module, a set of registers is provided to set up the screen raster defined as width and height. A trigger position can be specified as an x, y coordinate within the overall dimensions of the screen raster. If the x, y counter matches the specified coordinates, a trigger pulse is generated which pre-loads the tables with their initial values. Refer to the 1080i example for the trigger programming.

Important Notes

- The “duration” in the “Line_Pattern_Array” that needs to be programmed should be 1 cycle less than the actual duration required.
- For the registers LCNT_ARRAY_ADR (offset 0x82), LTYPE_ARRAY_ADR (offset 0x86), LPATT_ARRAY_ADR (offset 0x8E), “addr+1” should be written to finish writing the data meant for “addr,” for example:

For the registers LCNT_ARRAY_ADR (offset 0x82), LTYPE_ARRAY_ADR (offset 0x86), LPATT_ARRAY_ADR (offset 0x8E), “addr+1” should be written to finish writing the data meant for “addr,” for example:

LTYPE_ARRAY_LINE1 = 0x14

LTYPE_ARRAY_LINE2 = 0x05

LTYPE_ARRAY_LINE3 = 0x00

LTYPE_ARRAY_LINE_ADR = 0x01

Note the next address, 0x02, is written to finish writing to the previous address 0x01.

LTYPE_ARRAY_LINE_ADR = 0x02

LTYPE_ARRAY_LINE1 = 0x14

LTYPE_ARRAY_LINE2 = 0x03

LTYPE_ARRAY_LINE3 = 0x00

LTYPE_ARRAY_LINE_ADR = 0x02

Note the write to next address, 0x03

LTYPE_ARRAY_LINE_ADR = 0x03

LTYPE_ARRAY_LINE1 = 0x0C

LTYPE_ARRAY_LINE2 = 0x03

LTYPE_ARRAY_LINE3 = 0x00

LTYPE_ARRAY_LINE_ADR = 0x03

Note the write to next address, 0x04

LTYPE_ARRAY_LINE_ADR = 0x04

- The HD Sync Generator inserts a definable sync pattern (that normally includes blanking) into the video line. This includes a 'Select' bit [in the Line_Pattern_Array] which determines whether the current portion of the line should display video or generated sync. Each portion of the line has a color value defined, which will be displayed if Select=1. There is a 1 pixel path difference between 'Select' and 'Value', resulting in the momentary display of the color value for 1 pixel width until the Select bit switches active video to the output display.

The work around for the above problem is to ensure that the Value array entry for the 'active' portion of the line is set the same as the previous portion of the line. This will normally mean setting the value to blanking level. This will ensure that during the 1 clock path difference, the color value output will be the same as for the previous portion of the line. This will remove the observed spike.

The listing below outlines an example on how to set up the sync tables for a 1080i HD raster:

```
// hd-sync config file for 1080i

#line_count_array

//index //line_count
------------------
25//5 lines vsync
41//1 line sync-black-sync-black
614//14 lines blank
1537//537 lines active video
65//5 lines blank
51//1 line sync-black-sync-blank
24//4 lines sync
31//1 line sync blank sync black
615//15 lines blank
1537//537 lines active video
65//5 lines blank
00//dummy lines
00//dummy lines
00//dummy lines
00//dummy lines
00//dummy lines
#line_type_array
//p8p7p6p5p4p3p2p1
---------------
00000034 //sync-full active line
00002424 //sync-half blank-sync-half blank
00001424 //sync-half blank-sync-half black
00001414 //sync-half black-sync-half black
00002414 //sync-half black-sync-half blank
00000054 //sync-full line black
00000000
00000000
```

```
00000000
00000000
00000000
00000000
00000000
00000000
00000000
#line_pattern_array
//d=duration s=select v=value
//d4s4v4d3s3v3d2s2v2d1s1v1
--------------------
000000431387913 //half line black
000000431387910 //half line blank
431395906959065913 //full active line
000871343124311 //sync pulse
431395913959135913 //full line black
000000000000
000000000000

#value_array
//signed values
// YUV
--------------
-51200//broad pulse level
-512-432-432//lower sync tip
102432432//upper sync tip
-20400//black/blank level org
000
000
000
000
```

#other

//trigger_line

// preload of the line count in

//addr 0x9a-0x99 -hex values

99 3

9a 00

//trigger_duration

// preload of duration of the line pattern array

//addr 0x9c-0x9b -hex values

9c 0

9b 2

//trigger pointer

9d 0x11

// bit 1:0 loads the counter value of line count array

// bit 7:4 loads the counter value of the line pattern array

//sync raster

//sync height

ae 0x64

af 0x04

//sync width

b0 0x97

b1 0x08

//sync trigger pos

//trigger pos x

b4 0x15

b5 0x00

//trigger pos y

b2 0x15

b3 0x00

A complete example of register settings for 1080i is given in Section 9.

The listing below outlines an example on how to set up the sync tables for a 720p raster:

```
// hd-syn config file for 720p

#line_count_array

//index line_count
-------------------------------------
25//5 lines vsync
320//20 lines blank
1360//360 lines active video
1360//360 lines active video
35//5 lines blank
00//dummy lines
00//dummy lines
00//dummy lines
00//dummy lines
00

#line_type_array
```

```
//p8p7p6p5p4p3p2p1
-------------------------------------
00000034 //sync-full line active
00000024 //sync-full line blank (vsync)
00000054 //sync-full line black (v-blanking)
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000

#line_pattern_array
//dur4sel4val4dur3sel3val3dur2sel2val2dur1sel1val 1
-----------------------------------------------------
000000000000 //empty
00069137141071410 //full line blank
6913639006390014913 //full line active
000691339123911 //sync pulse
6913639136391314913 //full line black
000000000000
000000000000

#value_array Y
//signed values
  YUV
------------------------
-51200//broad pulse level
-512-432-432//lower sync tip
102432432//black/blank level org
000
000
000
000
```

7.2.3 Signature analysis

PNX8510/11 allows the signature analysis to be done on both primary and the secondary video channels and read the two signatures separately. The signature analysis is done on the upper 8 bits of the interface. The video channel select for the signature analysis is defined by the “SIG_SELECT” of the SIGCTRL (offset 0xBA) register.

The signature is calculated as per the following CRC algorithm:

```
// * This is a simple table based CRC-16 that computes the CRC

// * four bits at a time. This requires a small (16 entry) lookup table.

// * lookup table for non-reversed parallel CRC algorithms

//   unsigned int crc16_table[16]={

//        0x0000, 0x8005, 0x800f, 0x000a,
```

```
//       0x801b, 0x001e, 0x0014, 0x8011,
//       0x8033, 0x0036, 0x003c, 0x8039,
//       0x0028, 0x802d, 0x8027, 0x0022
//   };
//
// * Unlike the serial method, this algorithm does not require any additional
//  * operations to finish the CRC after the message is processed
// * This routine uses crc1 to hold the crc.
// */
//
//   void parallel_crc1(c)
//   int c;
//   {
//      int r1 ;
//
//      /* calculate CRC using the 4 bit LUT method */
//      /* upper 4 bits */
//      r1 = crc16_table[((crc1>>12) & 0xF) ^ ((c & 0xf0) >> 4)];
//      crc1 = ((crc1 << 4) & 0xFFF0) ^ r1;
//
//      /* lower 4 bits */
//      r1 = crc16_table[((crc1>>12) & 0xF) ^ (c & 0x0f)];
//      crc1 = ((crc1 << 4) & 0xFFF0) ^ r1;
//   }
```

7.2.4 Limitations of the video pipe

In all HD modes, the video encoder will be switched off. Either a separate sync signal or the embedded syncs of the D1 input can be used to generate the sync raster driving the display device.

7.3 Audio pipeline

The PNX8510/11 has two independent stereo channels, each connected to a separate audio interface. The primary audio channel is usually associated with the primary video channel and carries the accompanying sound information. The

secondary audio channel usually carries the audio belonging to the record (secondary) video channel. Because they might originate from different sources, the two interfaces are operated by independent clocks.

Mute on/off is programmable by a register setting. Table 19 describes the expected audio performance.

Table 19: Audio performance

Parameter	QFP100
Dynamic range	85dB
S/(N+Disto.)	>85dB

The audio path has three general blocks: input, interpolation, and DAC.

- The input is, by default, a 24-bit I^2S interface. However, it can be programmed to accept other formats.
- The interpolator scales, filters and oversamples the incoming data by 64 x its sampling frequency. The result goes to a Noise Shaper, which shifts in-band noise to frequencies well above the audio spectrum. This provides a very high signal-to-noise ratio.
- Finite Impulse Response DACs convert the 1-bit data stream to analog output voltage.

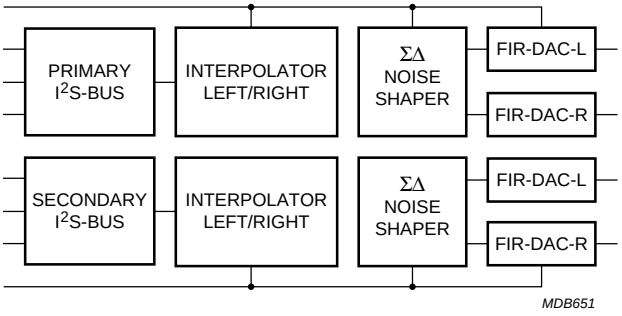


Fig 23. Audio path block diagram

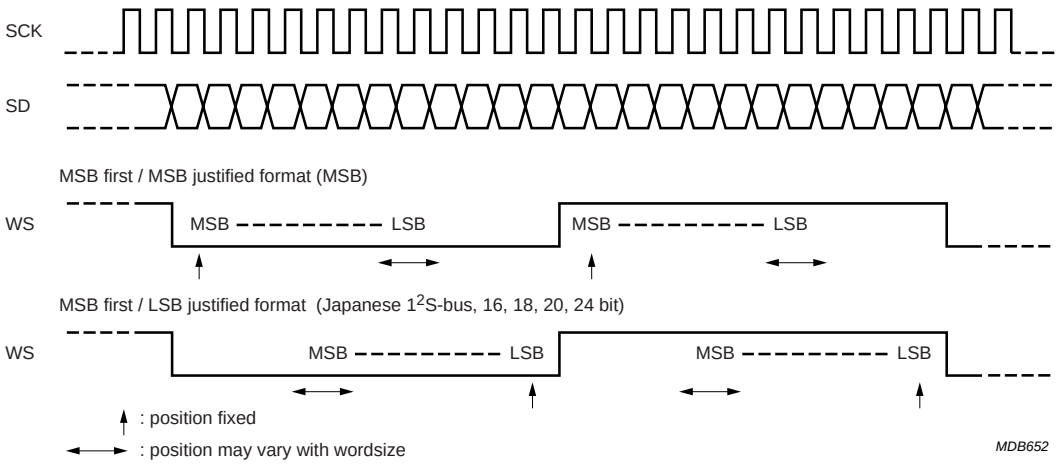
7.3.1 Audio interface operation

The audio interfaces can be operated in either slave or master mode:

- In slave mode, all required clocks (System CLK, SCK and WS) must be generated externally and must be synchronous with each other.
- In master mode, the PNX8510/11 only gets the System CLK and generates SCK and WS clocks synchronously to the applied System CLK. In this mode, System CLK is equal to 128 x Fs where Fs is the audio sampling frequency.

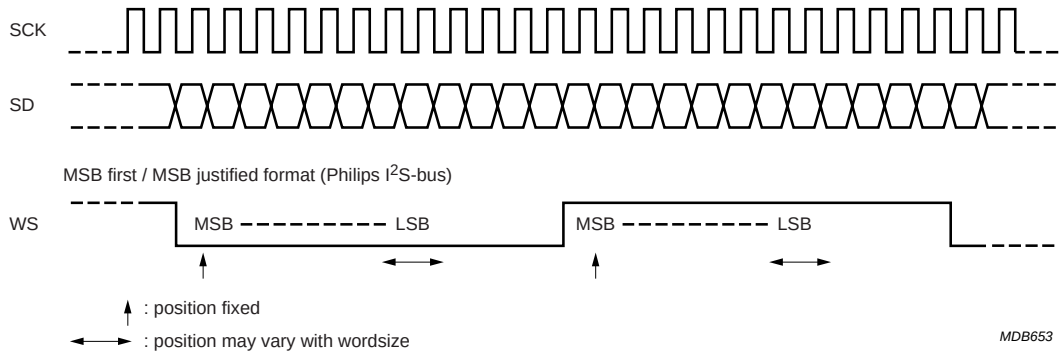
Audio input timing

Figure 24 and Figure 25 illustrate the different modes of operation for the I²S interface used in the PNX8510/11.



Justification bit is not delayed.

Fig 24. Input formats



Justification bit is one bit clock delayed.

Fig 25. Input format

Table 20: I²S signals

Port	Description
SCK	Bit clock
SD	PCM data
WS	Word Select; left and right clock is equal to the sample rate.

7.3.2 Mute modes

The audio modules of the PNX8510/11 have several mute functions. The mute operation is controlled via the bits “quickmute, and mutemode” of the programming register, INTERPOLATOR_REG2(offset 0x00FD).

Quick mute

This is an overriding quickmute on the master channel, which mutes the interpolator output signal in 32 samples using the cosine roll-off coefficients instead of 32x32 samples to mute the output. This means whenever the quickmute register is set to one, independent of what the mute setting of the micro controller is, the output is muted.

Mute mode

This register sets the mute mode for the MASTER MUTE to either soft mute (setting is ‘0’) or to quick mute (setting = ‘1’). For the master channel the quickmute function and the micro controller mute function are OR’d.

Table 21: Mute mode control

Quick mute	Micro controller mute	Function
0	0	No mute
0	1	1 micro controller mute...mute mode depends on the ‘mutemode’ setting.
1	X	Overriding quick mute function

Table 22: Mute Mode Function

While in Mute Mode, releasing the ‘mute’ bit applies a graduated cosine startup

Mute mode	Function
0	Mute function via micro controller interface is set to “soft mute.”
1	Mute function via micro controller interface is set to “quick-mute.”

Figure 26 shows the signal flow for the mute control.

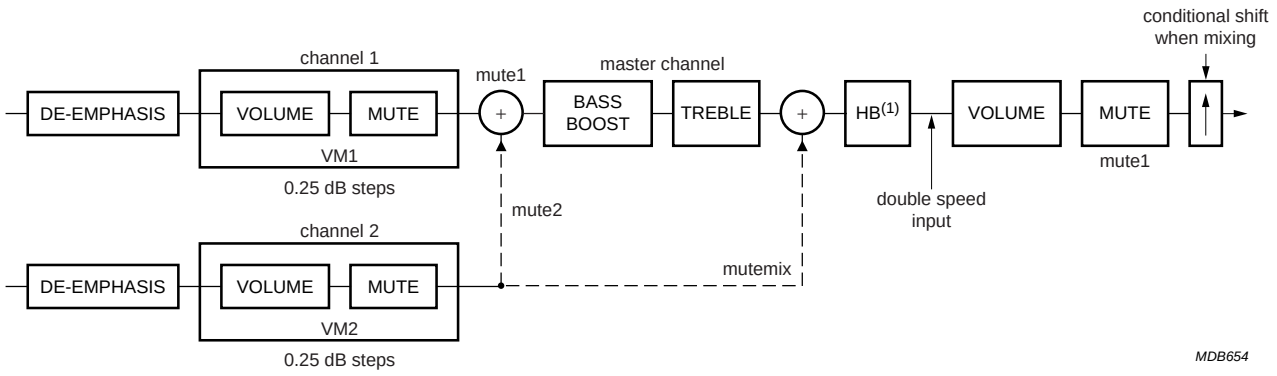


Fig 26. Mixing possibilities in interpolator 4v0

7.4 Programming interface

The configuration of the various interface modes and the digital video encoder setup can be controlled via an I^2C interface or a special VBI data packet sent during the horizontal blanking interval. With the VBI programming interface, a reliable real-time programming for the PNX8510/11 video blocks can be accomplished. For instance, this mode makes it very easy to carry the necessary programming data over to the digital encoder to encode a certain teletext packet in a specific scanline without

extensive buffering. The format for programming registers in the PNX8510/11 via the VBI interface can be found in Section 7.1.5. Note that reprogramming clocks and audio registers are not possible via the VBI interface.

The PNX8510/11 is an I^2C slave device only. It uses four dedicated slave addresses to address the primary, secondary, audio and remaining control registers. The I^2C address set can be configured during reset with a pull-up or pull-down combination of GPIO pins.

Table 23 shows the register sets and the relationship with the 'xy' bits in the address structure.

Table 23: Relation of 'xy' with register sets

Address= GPIO5-GPIO4-XY-GPIO3-GPIO2-GPIO1-R/W

Register Set	x	y
VIDEO 1	0	0
VIDEO 2	0	1
AUDIO 1 / VIDEO 1 and AUDIO 1 clocks	1	0
AUDIO 2/ VIDEO 2 and AUDIO 2 clocks	1	1

Table 24 shows an example of how the I^2C device addresses are determined.

Table 24: I^2C Address determination

Register Set	Selection Example
VIDEO 1	IIC address selection example:
VIDEO 2	GPIO5-2 are set to logic one and GPIO1 is set to zero during the PNX8510/11rest.
AUDIO 1 / VIDEO 1 and AUDIO 1 clocks	Address = GPIO5-GPIO4-XY-GPIO3-GPIO2-GPIO1-R/W
AUDIO 2/ VIDEO 2 and AUDIO 2 clocks	Address = 1-1-XY-1-1-0-R/W
	VIDEO1 = 1-1-0-0-1-1-0-R/W = 0xCC(write), 0xCD(read)
	VIDEO2 = 1-1-0-1-1-1-0-R/W = 0xDC (write), 0xDD(read)
	AUDIO1 = 1-1-1-0-1-1-0-R/W = 0xEC(write), 0xED(read)
	AUDIO2 = 1-1-1-1-1-1-0-R/W = 0xFC(write), 0xFD(read)

A detailed description of all programming registers can be found in Section 8.

7.5 GPIO block

GPIOs are multi-purpose pins. They may be programmed as input/output and used to carry signals into the IC or to monitor the status of the IC. The selection of these I/O pins is controlled through programmable registers. The GPIO module can be programmed via subaddress 90-95 of the primary video pipe.

The GPIO pins operate in two basic modes; Bootstrap mode and GPIO mode. During chip reset the GPIOs are in bootstrap mode. The status of all GPIO pins is monitored and used to determine the set of I^2C device addresses the IC responds to.

After the chip reset is released, the GPIO pins may be used in GPIO mode. In output mode each GPIO pin can be set to logic one or zero by programming the appropriate register. In input mode the status of each GPIO can be monitored by reading the

appropriate status register. In addition to the register-driven I/O mode, some of the GPIO pins are used to reflect the status of internal signals. Some GPIO pins are also used as additional inputs to functional units if operated in input mode.

7.5.1 Operation

GPIO set during reset

During reset the GPIO output is disabled. GPIO_in is stored as gpio_in_stored and retains its value until the next reset. This stored value determines the I^2C device addresses. After reset, GPIO pins can be programmed for output with the OEN and OUT_SEL bits.

Checking/setting the GPIO status

Each GPIO pin is multiplexed four times to increase usability. Figure 27 outlines the internal structure of one GPIO pin. In output mode the selection of the signal routed out to a GPIO pin is performed with the OUT_SEL register bits. The OEN bit is low active and enables the GPIO output mode. If OUT_SEL is set to 2'b11 and the OEN bit is set to zero, the GPIO pin can be set or reset by writing a one or zero into the STATUS location of the GPIO register. All other OUT_SEL settings are listed in Table 29.

To read the external status of a GPIO pin, the OEN needs to be set to one to avoid conflicts with signals routed out of the chip. If GPIO_IN_EN4 is set to one, the status of the GPIO pin can be monitored by reading the STATUS bit of the appropriate GPIO register. The function of all relevant GPIO_IN/OUT signals are listed in Figure 27 and Table 25.

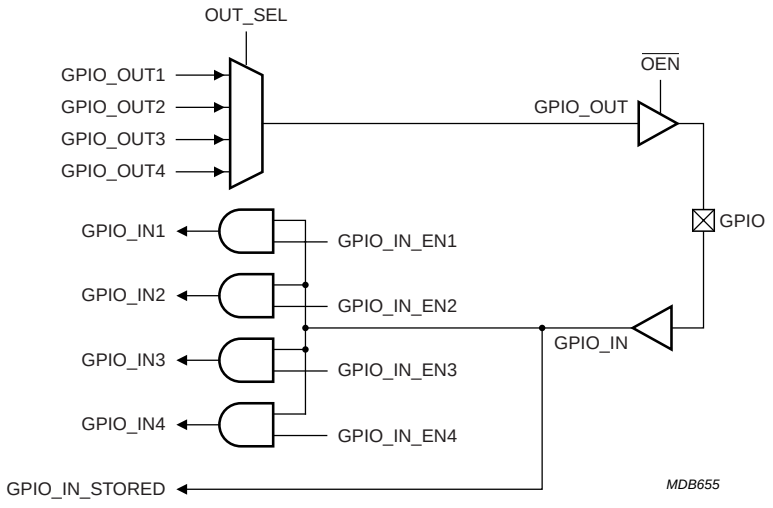


Fig 27. Operation modes for one GPIO in the PNX8510/11

Table 25: Specific GPIO assignments

Signal	Description
gpio5_out1	Composite sync secondary encoder
gpio5_out2	Vertical sync primary encoder
gpio5_in3	30-bit parallel video input mode: bit[1] = red channel

Table 25: Specific GPIO assignments...*continued*

Signal	Description
gpio4_out1	Data request secondary encoder
gpio4_out2	Composite sync primary encoder
gpio4_in3	30-bit parallel video input mode: bit[0] = red channel
gpio3_out1	Enable y secondary encoder (1/2 of the encoder operation frequency)
gpio3_out2	Odd/even signal primary encoder
gpio3_in1	Real time control input primary encoder
gpio3_in2	Real time control input secondary encoder
gpio3_in3	30-bit parallel video input mode: bit[1] = green channel
gpio2_out1	Odd/even signal secondary encoder
gpio2_out2	Data request primary encoder
gpio2_in3	30-bit parallel video input mode: bit[0] = green channel
gpio1_out1	Vertical sync secondary encoder
gpio_in3	30-bit parallel video input mode: bit[0] = blue channel
	All other settings are reserved for future use

7.6 Clock module

All of the PNX8510/11 modules receive their input clocks from the clocks module. The top level structure of the clocks module is Figure 28.

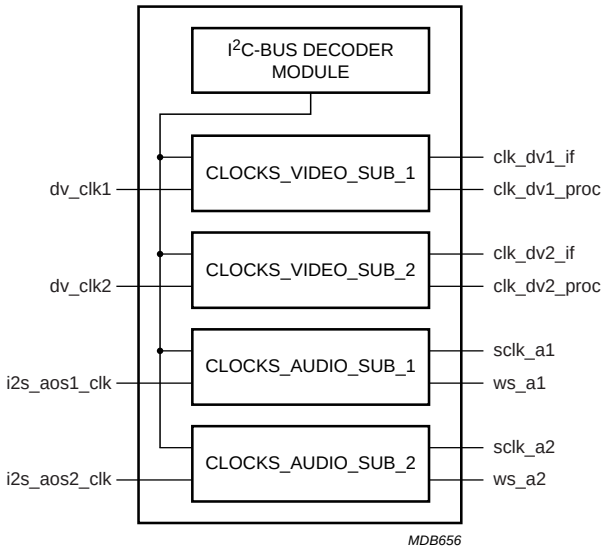


Fig 28. Clocks module

The PNX8510/11 in normal operation mode receives four external clocks. Two clocks dv_clk1 and dv_clk2 are the clocks used for the primary and secondary video data paths. The other two clocks assemble the audio over-sampling clocks for the primary and secondary audio channel.

The PNX8510/11 video clocks are used to create two internal clocks: one for operating the video input interface (clk_dv1_if, clk_dv2_if), and one for operating the main video processing pipeline (clk_dv1_proc, clk_dv2_proc).

The audio interface normally operates in slave mode (over-sampling clock, word select and bit clock are provided from the externally connected I^2S master). However the PNX8510/11 can be operated in master mode. This mode only requires the over-sampling clock to be provided. The bit clock and the word select signals are subdivided from the over-sampling clock and provided to the chip pins.

Remark: Both video clocks (DV_CLK1 and DV_CLK2) and an audio clock (I2S_AOS1_CLK) have to be connected to the device for proper functioning of the I^2C programming interface. These clocks must be provided before the reset line (RESET_N) is pulled high to ensure correct initialization of the device. For more information refer to Section 10.4.

If the two video pipelines are sourced by only one video input interface operating in sliced mode, both video pipelines must receive the same input clock originating from the same sliced data source.

7.6.1 Clocks video submodule

The generation of the various clock signals needed for video pipelines takes place in the clocks video module. Figure 29 shows a block diagram of this module. The configuration registers for the clocks module can be found in Section 8.2.

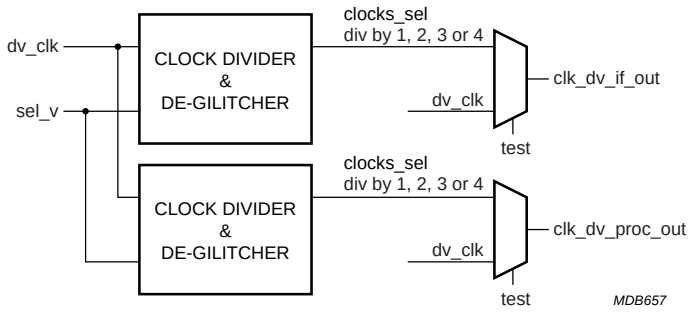


Fig 29. Clocks video submodule

7.6.2 Clocks audio submodule

The input clocks for the audio block are generated in the clocks audio submodule. Figure 30 shows a block diagram for this submodule

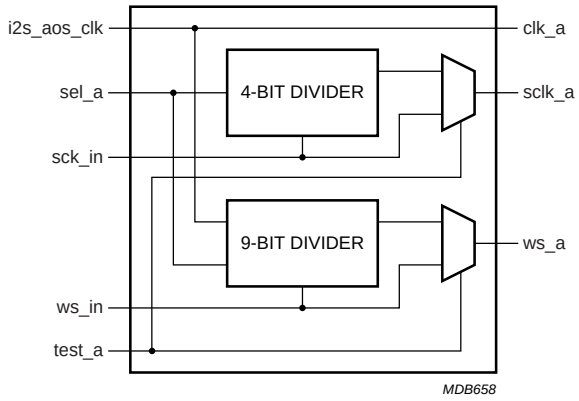


Fig 30. Clocks audio submodule

7.7 Test mode

This section describes how the analog test modes are implemented in the PNX8510/11. Note that these test modes are intended for production test only. The chip needs to be brought into analog test mode via the JTAG boundary scan controller. Once the chip is in analog test mode the different test modes can be enabled via the GPIO pins. The data input for the video DACs is provided via the DV1 interface for DACs 1 through 4 and via the DV2 interface for DACs 5 and 6 respectively. The “main switch” for the test mode is controlled by the JTAG boundary scan controller. Once the chip is in analog test mode, the GPIO pins can be used to select certain combinations outlined in the tables.

Table 26: Video DAC test modes

GPIO2	GPIO3	Test
0	0	VDAC1 and VDAC5 active
0	1	VDAC2 and VDAC6 active
1	0	VDAC3 and VDAC5 active
1	1	VDAC4 and VDAC6 active

For the video DACs 1 to 4, the primary 10-bit D1 interface (DV1_IN[9:0]) provides the 10-bit input. Video DACs 5 and 6 are stimulated through the secondary D1 interface (DV2_IN[9:0])

Table 27: Audio DAC test modes

GPIO4	GPIO5	Test
0	0	ADAC1/2 and ADAC3/4 stereo pair first and second channel off
0	1	ADAC1/2 stereo pair first channel active
1	0	ADAC3/4 stereo pair second channel active
1	1	ADAC1/2 and ADAC3/4 stereo pair first and second channel active

The serial audio data streams for the first stereo pair are provided through the I2S_IN1_SD and the I2S_IN1_WS pins. The audio DAC pair 3 and 4 get their serial data through pins I2S_IN2_SD and I2S_IN2_WS.

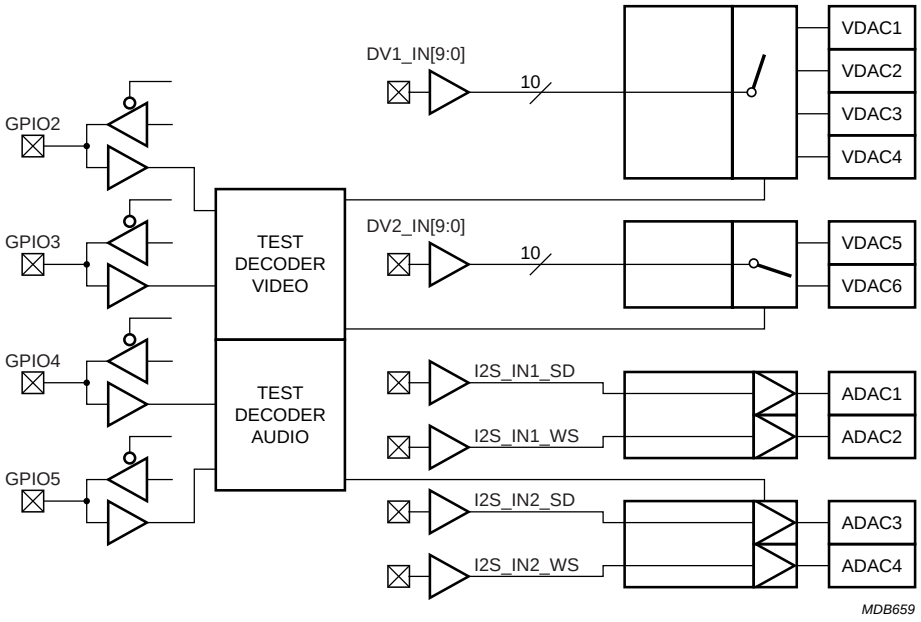


Fig 31. Audio and video DAC test modes

8. Register descriptions

The PNX8510/11 register space is divided into four different spaces. Each of them is addressed by a different I^2C device address. The first address space is dedicated to the primary video channel, the second space belongs to the secondary video channel. The third I^2C address space accommodates the registers that control the first audio channel. The fourth I^2C space is used to address the secondary audio channel.

The video channel registers are only listed once. Because the secondary video channel does not support high definition or RGB output, its registers have some minor differences, which are noted in Table 28 and Table 29 as “Not present in secondary video channel.”

The slave addresses are selectable during boot. The registers for the primary and secondary audio and video modules are identical, except as noted in the register definitions. Table 28 and Table 29 provide the offset– the base address is dependent on the module.

The actual address spaces are determined at boot time according to the GPIO settings. For more information refer to Section 7.4.

Table 28: PNX8510/11 register summary

*Descriptions with * have different meaning, or are not present in secondary video address space. See Table 29 for more details.*

Address	Name	Description
Video address space		
0x00	STATUS	Status register
0x1A	MSMT	Monitor sense mode threshold

Table 28: PNX8510/11 register summary…*continued*

*Descriptions with * have different meaning, or are not present in secondary video address space. See Table 29 for more details.*

Address	Name	Description
0x1B	MSMS	Monitor sense mode status
0x26	WSS1	Wide screen signaling data
0x27	WSS2	Wide screen signaling enable
0x28	BCTL	Burst control
0x29	BCTL2	Burst control
0x2A	CGD1	Copy guard
0x2B	CGD2	Copy guard
0x2C	CGD	Copy guard enable
0x2D	DACCTL	DAC control *
0x38	GAIN_Y	Gain adjust for Y component (SD RGB/YUV data path)*
0x39	GAIN_UV	Gain adjust for UV component (SD RGB/YUV data path)*
0x3A	INPCTL	Input control register *
0x54	VPS1	Video programming system
0x55	VPS2	Video programming system
0x56	VPS3	Video programming system
0x57	VPS4	Video programming system
0x58	VPS5	Video programming system
0x59	VPS6	Video programming system
0x5A	CHPS	Color subcarrier phase
0x5B	GAINU	Gain adjust for U component
0x5C	GAINV	Gain adjust for V component
0x5D	BLCKL	Black level adjust
0x5E	BLNNL	Blank level adjust
0x5F	BLNVB/CCR	Cross color reduction / blank level (during vertical blank)
0x61	STDCTL	Video standard control
0x62	BSTA	Burst amplitude control
0x63– 66	FSC0-FSC3	Color subcarrier frequency control
0x67	L21O0	Closed captioning odd field
0x68	L21O1	Closed captioning odd field
0x69	L21E0	Closed captioning even field
0x6A	L21E1	Closed captioning even field
0x6C	TRGCTL1	SD trigger control
0x6D	TRGCTL2	SD trigger control
0x6E	MULTICTL	Sync and blank control
0x6F	TTXCTL	VBI insertion control
0x70	ADWHS	Active display window start
0x71	ADWHE	Active display window end
0x72	ADWHS/E	Active display window - MSB
0x73	TTXHS	TTX control

Table 28: PNX8510/11 register summary…*continued*

*Descriptions with * have different meaning, or are not present in secondary video address space. See Table 29 for more details.*

Address	Name	Description
0x74	TTXHL/TTXHD	TTX control
0x75	CSYNCA	Composite sync control
0x76	TTXOVS	TTX insertion control odd field
0x77	TTXOVE	TTX insertion control odd field
0x78	TTXEVS	TTX insertion control even field
0x79	TTXEVE	TTX insertion control even field
0x7A	FAL	First active line
0x7B	LAL	Last active line
0x7C	TTXCTRL	TTX format control
0x7E	DTTXL	TTX mask
0x7F	DTTXL2	TTX mask
0x80	LCNT_ARRAY_LINE	HD sync generator control *
0x81	LCNT_ARRAY_LINE	HD sync generator control *
0x82	LCNT_ARRAY_ADR	HD sync generator control *
0x83– 0x85	LTYPE_ARRAY_LINE	HD sync generator control *
0x86	LTYPE_ARRAY_ADR	HD sync generator control *
0x87– 0x8D	LPATT_ARRAY_LINE	HD sync generator control *
0x8E	LPATT_ARRAY_ADR	HD sync generator control *
0x90– 0x94	GPIO5-GPIO1	GPIO control *
0x95	VMUXCTL	Video input mode control *
0x96– 0x97	VALUE_ARRAY_LINE	HD sync generator control *
0x98	VALUE_ARRAY_ADR/EVENT_TYPE_PTR	HD sync generator control *
0x99– 0x9A	TRIGGER_LINE	HD sync generator control *
0x9B– 0x9C	TRIGGER_DURATION	HD sync generator control *
0x9D	TRIGGER_PTR	HD sync generator control *
0x9E	BLANK_Y	Programmable blank level for Y (SD RGB/YUV data path) *
0x9F	BLANK_UV	Programmable blank level for UV (SD RGB/YUV data path) *
0xA0	RGB_CTRL	Color space matrix bypass enable *
0xA2	BORDER_Y	Border color
0xA3	BORDER_U	Border color
0xA4	BORDER_V	Border color
0xA5	MISCCTRL	DAC and trigger control *
0xA6	HDCTRL	HD video path control *
0xA7	SYNC_DELAY	Sync and VBI programming control
0xA8	BLANK_R/Y	Blank offset control HD video path *
0xA9	BLANK_G/U	Blank offset control HD video path *
0xAA	BLANK_B/V	Blank offset control HD video path *
0xAE	SYNC_HEIGHT1	HD sync generator screen height *

Table 28: PNX8510/11 register summary…*continued*

*Descriptions with * have different meaning, or are not present in secondary video address space. See Table 29 for more details.*

Address	Name	Description
0xAF	SYNC_HEIGHT2	HD sync generator screen height *
0xB0	SYNC_WIDTH1	HD sync generator screen width *
0xB1	SYNC_WIDTH2	HD sync generator screen width *
0xB2	SYNC_TRIGPOS_Y1	HD sync generator vertical position control1 *
0xB3	SYNC_TRIGPOS_Y2	HD sync generator vertical position control2 *
0xB4	SYNC_TRIGPOS_X1	HD sync generator horizontal position control1 *
0xB5	SYNC_TRIGPOS_X2	HD sync generator horizontal position control2 *
0xB6	SIG1	Video signature *
0xB7	SIG2	Video signature *
0xB8	SIG3	Video signature *
0xB9	SIG4	Video signature *
0xBA	SIGCTRL	Video signature analyzer control *
0xBC	BLANK_MSBs	Blank offset control *
0xBE	R/Y Value Array Line	R/Y value array data *
0xBF	B/U Value Array Line	B/U value array data *
0xC0	G/V Value Array Line	G/V value array data *
0xC1	Value Array Line MSBs	Value array data MSBs *
0xC2	DAC1 ADJ	Coarse current control DAC1 *
0xC3	DAC2 ADJ	Coarse current control DAC2 *
0xC4	DAC3 ADJ	Coarse current control DAC3 *
0xC5	DAC4 ADJ	Coarse current control DAC4 *
0xC6	DACC ADJ	Common current fine adjust for DACs 1-4 *
0xC7	HD_Gain R/Y	Gain adjust HD path *
0xC8	HD_Gain G/U	Gain adjust HD path *
0xC9	HD_Gain B/V	Gain adjust HD path *
Audio/clock address space		
0x0000	CLK_AUDIO	Audio clock control
0x0001	CLK_IF	Video interface clock control
0x0002	CLK_PROC_DIV	Video processing clock control
0x0003	CLK_DAC_DIV	Video DAC clock control
0x00F4	I^2S_SET_REG	Audio interface control
0x00F5– 00FB	FEATURE_REG	Audio feature control
0x00FC	INTERPOLATOR_REG1	Audio feature control
0x00FD	INTERPOLATOR_REG2	Audio feature control
0x00FE	Audio DAC power on register	Audio DAC control

8.1 Video address space

Table 29: PNX8510/11 video registers

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
Offset 0x00 STATUS				
7	VER2	R	0	Version ID bit 2
6	VER1	R	0	Version ID bit 1
5	VER0	R	1	Version ID bit 0
4	CCRDO	R	-	Closed caption encoding done for odd field
3	CCRDE	R	-	Closed caption encoding done for even field
2	Unused		-	
1	FSEQ	R	-	Field Sequence 1 = During first field of a sequence 0 = Not the first field of a sequence
0	O_E	R	-	Status of the ODD/EVEN flag in the encoder
Registers 0x01 through 0x10 must be initialized to zero.				
Offset 0x1A MSMT				
7:0	MSMT	R/W	-	Monitor sense mode threshold for DACs comparator
Offset 0x1B MSMS				
7	MSM	R/W	0	Monitor sense mode 0 = Off 1 = On
6:4	Unused		-	
3	MSMS4*	R	-	Monitor sense status DAC4 0 = Comparator is inactive. 1 = Comparator is active.
2	MSMS3*	R	-	Monitor sense status DAC3 0 = Comparator is inactive. 1 = Comparator is active.
1	MSMS2	R	-	Monitor sense status DAC2 0 = Comparator is inactive. 1 = Comparator is active.
0	MSMS1	R	-	Monitor sense status DAC1 0 = Comparator is inactive. 1 = Comparator is active.
Registers 0x1C through 0x25 must be initialized to zero.				
Offset 0x26 - WSS1				
7:0	WSSD[7:0]	R/W	-	Wide screen signalling data bits 3:0 = Aspect ratio encoding bits 7:4 = Enhanced services
Offset 0x27 - WSS2				
7	WSSON	R/W	0	Wide screen signalling enable 0 = wss switched off 1 = wss switched on
6	Unused		-	

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
5:0	WSSD[13:8]	R/W	-	Wide screen signalling data bits 13:11 = Reserved bits 10:8 = Subtitles
Offset 0x28 - RTC1/BCTL1				
7	DECFIS	R/W	0	Field sequence detection via RTC 0 = Field sequence as FISE in address 61 1 = Field sequence detection via RTC interface
6	DECCOL	R/W	0	Color detection via RTC interface 0 = Color detection via RTC disabled 1 = Color detection via RTC enabled Note: The RTCE bit must be set to 1 to enable this feature.
5:0	BS	R/W	0x21	Starting point of color burst in clk cycles from Hsync PAL=0x21 NTSC=0x25
Offset 0x29 - BCTL2				
7:6	Unused		-	
5:0	BE	R/W	0x1d	Color burst end point in clk cycles from Hsync PAL = 0x1D NTSC = 0x1D
Offset 0x2A - CGD1				
7:0	CG	R/W	-	Copy guard information bits 7:0 Note: The 14 LSBs of the byte carry the information encoded after the run-in. The 6 MSBs have to carry the CRCC bits in accordance with the definition of the CGMS encoding format.
Offset 0x2B - CGD2				
7:0	CG	R/W	-	Copy guard information bits 15:8 Note: The 14 LSBs of the byte carry the information encoded after the run-in. The 6 MSBs have to carry the CRCC bits in accordance with the definition of the CGMS encoding format.
Offset 0x2C - CGD				
7	CGEN	R/W	0	Copy guard enable 0 = Disabled 1 = Enabled
6:4	Unused		-	
3:0	CG	R/W	-	Copy guard information bits 19:16 Note: The 14 LSBs of the byte carry the information encoded after the run-in. The 6 MSBs have to carry the CRCC bits in accordance with the definition of the CGMS encoding format.
Offset 0x2D - DACCTL Video data path				
7	VBSEN*	R/W	1	DAC3 control 0 = Video dac 3 carries the green channel. 1 = Video dac 3 carries the luminance channel.

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
6	CVBSEN	R/W	1	DAC1 control 0 = Video dac 1carries the luminance channel. 1 = Video dac 1 carries the CVBS channel.
5	CEN*	R/W	1	DAC2 control 0 = Video dac 2 carries the red channel. 1 = Video dac 2 carries the chroma channel.
4:0	Unused		-	
Registers 0x2E– 0x37 must be initialized to zero.				
Offset 0x38 - GAIN_Y *				
7:5	Unused		-	
4:0	GAIN_Y*	R/W	0x1A	Gain adjust for Y component in SD-RGB/YUV data path, two's complement number to adjust the gain from -50% to +50% Yout=Yin x (1+ GAIN_Y/32)
Offset 0x39 - GAIN_UV*				
7:5	Unused		-	
4:0	GAIN_UV*	R/W	0x1A	Gain adjust for U/V components in SD-RGB/YUV data path, two's complement number to adjust the gain from -50% to +50% UVout=UVin x (1+ GAIN_UV/32)
Offset 0x3A - INPCTL				
7	CBENB	R/W	0	Color bar generator 0 = Color bar generation switched off 1 = Color bar generation enabled (SD-CVBS/YC and SD-RGB/YUV modes only)
6	QUALINVERT*	R/W	1	0 = Leave the pixel qualifier untouched. 1 = Invert the incoming pixel qualifier.
5	USE_QUAL*	R/W	0	Use qualifier enable 0 = No qualifier is used, QUALINVERT should be set. 1 = The HSYNC input is used as slice qualifier in interleaved mode.
4	DEDGE	R/W	0	Double edge mode 0 = Double edge mode off; either the interface is running at 2x speed to get interleaved data in or only non-interleaved data streams are accepted. 1 = Input data is latched at positive and negative edge. The SLICE_DIR register determines which data slice goes in which channel.
3	SD_HD*	R/W	1	Video mode switch 0 = HD data path in operation; encoder runs idle. 1 = SD data path in operation; encoder is in CVBS/YC or RGB mode.
2	U2C	R/W	1	0 = Y/R data channel coming from the D1 interface left unchanged 1 = Y/R MSB of data coming from the D1 interface is inverted.
1	M2C	R/W	1	0 = U/G data channel coming from the D1 interface left unchanged 1 = U/G MSB of data coming from the D1 interface is inverted.

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
0	L2C*	R/W	1	0 = V/B data channel coming from the D1 interface left unchanged 1 = V/B MSB of data coming from the D1 interface is inverted.
Registers 0x3B through 0x53 must be initialized to zero.				
Offset 0x54 - VPS1				
7	VPSEN	R/W	0	0 = Video programming system data insertion disabled 1 = Video programming system data insertion enabled
6:0	Unused		-	
Offset 0x55 - VPS2				
7:0	VPSB5	R/W	-	Fifth byte of video programming system data
Offset 0x56 - VPS3				
7:0	VPSB11	R/W	-	11th byte of video programming system data
Offset 0x57 - VPS4				
7:0	VPSB12	R/W	-	12th byte of video programming system data
Offset 0x58 - VPS5				
7:0	VPSB13	R/W	-	13th byte of video programming system data
Offset 0x59 - VPS6				
7:0	VPSB14	R/W	-	14th byte of video programming system data
Offset 0x5A - CHPS				
7:0	CHPS	R/W	0x0	Phase of encoded color subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.
Offset 0x5B, 0x5D(MSB) - GAINU				
7:0	GAINU	R/W	0x7d	Variable gain for Cb signal; input representation is in accordance with CCIR656. This is the digital gain for SD-Data path White to black = 92.5 IRE GAINU can be adjusted in a range from -2.17 x nominal to 2.16 x nominal GAINU=0 (output subcarrier contribution of U = 0) GAINU=0x76 (output subcarrier contribution of U = nominal) White to black = 100 IRE GAINU can be adjusted in a range from -2.05 x nominal to 2.04 x nominal GAINU=0 (output subcarrier contribution of U = 0) GAINU=0x7D (output subcarrier contribution of U = nominal) GAINU=0x6A (nominal Gain for Secam encoding)
Offset 0x5C, 0x5E(MSB) - GAINV				

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
7:0	GAINV	R/W	0xaf	Variable gain for Cr signal; input representation is in accordance with CCIR656. White to black = 92.5 IRE GAINV can be adjusted in a range from -1.55 x nominal to 1.55 x nominal GAINV=0 (output subcarrier contribution of V = 0) GAINV=0xA5 (output subcarrier contribution of V = nominal) White to black = 100 IRE GAINV can be adjusted in a range from -1.46 x nominal to 1.46 x nominal GAINV=0 (output subcarrier contribution of V = 0) GAINV=0xAF (output subcarrier contribution of V = nominal) GAINV=0x7F (nominal Gain for Secam encoding)
Offset 0x5D - BLCKL				
7	GAINU	R/W	0	Bit 8 of register 0x5B
6	DECOE	R/W	0	Odd/even field control via RTC interface 0 = Disabled 1 = Enabled
5:0	BLCKL	R/W	0x33	Variable black level; input representation is in accordance with CCIR656. White to sync = 140 IRE recommended BLCKL=0x3A BLCKL=0 (output black level = 29 IRE) BLCKL=0x3F (output black level = 49 IRE) output black level/IRE=BLCKL x 2/6.29+28.9 White to sync = 143 IRE recommended BLCKL=0x33 BLCKL=0 (output black level = 27 IRE) BLCKL=0x3F (output black level = 47 IRE) output black level/IRE=BLCKL x 2/6.18+26.5
Offset 0x5E - BLNNL				
7	GAINV	R/W	0	Bit 8 of register 0x5C
6	DECPH	R/W	0	Subcarrier phase reset control via RTC interface 0 = Disabled 1 = Enabled
5:0	BLNNL	R/W	0x35	Variable blanking level White to sync = 140 IRE recommended BLCKL=0x2E BLNNL=0 (output black level = 26 IRE) BLNNL=0x3F (output black level = 46 IRE) output black level/IRE=BLCKL x 2/6.29+25.4 White to sync = 143 IRE recommended BLCKL=0x35 BLNNL=0 (output black level = 26 IRE) BLNNL=0x3F (output black level = 46 IRE) output black level/IRE=BLCKL x 2/6.18+25.9

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
Offset 0x5F - BLNVB/CCR				
7:6	CCRS	R/W	0x0	Cross-color reduction filter settings for luminance path 00 = Cross color reduction filter off 01 = Filter is active; transfer characteristic 1 10 = Filter is active; transfer characteristic 2 11 = Filter is active; transfer characteristic 3
5:0	BLNVB	R/W	0x35	Variable blanking level during vertical blanking interval is typically identical to the value of BLNNL.
Offset 0x60 - Must be initialized to zero				
Offset 0x61 - STDCTL				
7:6	Unused		-	
5	INPI	R/W	0	0 = PAL switch phase is nominal. 1 = PAL switch phase is inverted compared to nominal if RTC is enabled.
4	YGS	R/W	0	0 = Luminance gain for white - black 100 IRE for PAL 1 = Luminance gain for white - black 92.5 IRE (for NTSC) including 7.5 IRE set-up of black
3	SECAM	R/W	0	SECAM enable 0 = Secam encoding switched off 1 = Secam encoding switched on (PAL has to be 0)
2	SCBW	R/W	1	0 = Enlarged bandwidth for chrominance encoding 1 = Standard bandwidth for chrominance encoding
1	PAL	R/W	1	0 = NTSC encoding (non alternating V component) 1 = PAL encoding (alternating V component)
0	FISE	R/W	0	0 = 864 total pixel per line for PAL 1 = 858 total pixel per line for NTSC
Offset 0x62 - RTCCTL/BSTA				
7	RTCE	R/W	0	0 = No real time control of generated subcarrier frequency 1 = Real time control of generated subcarrier frequency
6:0	BSTA	R/W	0x2f	Amplitude of color burst; input representation is in accordance with CCIR 601 White to black = 92.5 IRE, burst = 40 IRE, NTSC encoding BSTA 0 to 2.02 x nominal recommended value BSTA = 0x3F White to black = 92.5 IRE, burst = 40 IRE, PAL encoding BSTA 0 to 2.82 x nominal recommended value BSTA = 0x2D White to black = 100 IRE, burst = 40 IRE, NTSC encoding BSTA 0 to 1.90 x nominal recommended value BSTA = 0x43 White to black = 92.5 IRE, burst = 40 IRE, PAL encoding BSTA 0 to 3.02 x nominal recommended value BSTA = 0x2F fixed burst amplitude for SECAM encoding
Offset 0x63– 0x66 - FSC0-FSC3				

Table 29: PNX8510/11 video registers…*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
7:0	0x63=FSC0 0x64=FSC1 0x65=FSC2 0x66=FSC3	R/W	0x2A0 98ACB	ffsc: subcarrier frequency (in multiples of line frequency) fllc: clock frequency (in multiples of line frequency) FSC = round ((ffsc/fllc)x2^32) FSC3 most significant byte FSC0 least significant byte NTSC-M: ffsc 227.5, fllc 1716 -> FSC = 21F07C1F PAL-B/G: ffsc 283.7516, fllc 1728 -> FSC = 2A098ACB SECAM: ffsc 274.304, fllc 1728 -> FSC = 28A33BB2
Offset 0x67 - L21O0				
7:0	L21O0	R/W	0x0	First byte of closed captioning data, odd field
Offset 0x68 - L21O1				
7:0	L21O1	R/W	0x0	Second byte of closed captioning data, odd field
Offset 0x69 - L21E0				
7:0	L21E0	R/W	0x0	First byte of closed captioning data, even field
Offset 0x6A - L21E1				
7:0	L21E1	R/W	0x0	Second byte of closed captioning data, even field
Offset 0x6B - Must be initialized to zero.				
Offset 0x6C - TRGCTL1*				
7:0	HTRIG	R/W	0x01	Sets horizontal trigger phase related to encoder input. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed. Increasing HTRIG decreases delay as of all internally generated timing signals. This register is for the SD path. Reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG=0x398.
Offset 0x6D - TRGCTL2*				
7:5	HTRIG	R/W	0x1	Sets horizontal trigger phase related to encoder input.This register is for the SD path.
4:0	VTRIG	R/W	0x0	Increasing VTRIG decreases delays of all internally generated timing signals measured in half lines. Variation range of VTRIG = 0 to 0x1F
Offset 0x6E - MULTICTL				
7	Unused		-	
6	BLCKON	R/W	0	0 = Encoder in normal operation mode 1 = Output signal is forced to blanking level. This doesn't shutdown the sync and leaves it running.
5:4	PHRES	R/W	0x2	Selects the phase reset mode of the color subcarrier. 00 = No phase reset or reset via RTC 01 = Phase reset every two lines 10 = Reset every eight fields 11 = Reset every four fields

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
3:2	LDEL	R/W	0x0	Selects the luminance delay in reference to the chrominance 00 = No luma delay 01 = 1LLC luma delay 10 = 2LLC luma delay 11 = 3LLC luma delay
1:0	FLC	R/W	0x0	This register is to control the sync. generator Field length control 00 = Interlaced 312.5 lines/field at 50Hz, 262.5 lines/field at 60Hz 01 = Non interlaced 312 lines @50Hz, 262 lines @60Hz 10 = Non interlaced 313 lines @50Hz, 263 lines @60Hz 11 = Non interlaced 313 lines @50Hz, 263 lines @60Hz
Offset 0x6F - TTXCTL				
7:6	CCEN	R/W	0x00	Closed caption enable 00 = Line 21 encoding off 01 = Enables encoding in field 1 (odd). 10 = Enables encoding in field 2 (even). 11 = Enables encoding in both fields.
5	TTXEN	R/W	0	0 = Disables teletext insertion. 1 = Enables teletext insertion.
4:0	SCCLN	R/W	0x11	Selects the actual line where closed caption or extended data are encoded. line = (SCCLN + 4) for M-systems line = (SCCLN +1) for other systems
Offset 0x70 - ADWHS (Horizontal)				
7:0	ADWHS7:0	R/W	0x5a	Active Display Window Horizontal Start bits 7 to 0 Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
Offset 0x71 - ADWHE (Horizontal)				
7:0	ADWHE7:0	R/W	0x5a	Active Display Window Horizontal End bits 7 to 0 Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
Offset 0x72 - ADWHS/E				
7	Unused		-	
6:4	ADWHE10:8	R/W	0x6	Active Display Window Horizontal End bits 10 to 8. Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
3	Unused		-	
2:0	ADWHS10:8	R/W	0x1	Active Display Window Horizontal Start bits 10 to 8 Defines the start of the active TV display portion after the border color. Values above 1715 (FISE=1) or 1727 (FISE=0) are not allowed.
Offset 0x73 - TTXHS				
7:0	TTXHS	R/W	0x42	Start of teletext signal with respect to Horizontal Sync

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
Offset 0x74 - TTXHL/TTXHD				
7:4	TTXHL	R/W	0x5	Length of TTXRQ window; only active at old TTX protocol Note: bit TTXO = 1
3:0	TTXHD	R/W	0x2	Indicates the delay in clock cycles between rising edge of TTXRQ output and valid data at pin TTX.
Offset 0x75 - CSYNCA				
7:3	CSYNCA	R/W	0x0	Advances composite sync against RGB output, adjustable from 0 XTAL clocks to 31 XTAL clocks
2:0	Unused		-	
Offset 0x76 - TTXOVS				
7:0	TTXOVS	R/W	0x5	First line of occurrence of Teletext data in odd field line = (TTXOVS + 4) for M-systems line = (TTXOVE +1) for other systems PAL: TTXOVS = 0x05 NTSC: TTXOVS = 0x06
Offset 0x77 - TTXOVE				
7:0	TTXOVE	R/W	0x16	Last line of occurrence of Teletext data in odd field line = (TTXOVS + 3) for M-systems line = TTXOVE for other systems PAL: TTXOVS = 0x16 NTSC: TTXOVS = 0x10
Offset 0x78 - TTXEVS				
7:0	TTXEVS	R/W	0x4	First line of occurrence of Teletext data in even field line = (TTXOVS + 4) for M-systems line = (TTXOVE + 1) for other systems PAL: TTXOVS = 0x04 NTSC: TTXOVS = 0x05
Offset 0x79 - TTXEVE				
7:0	TTXEVE	R/W	0x16	Last line of occurrence of Teletext data in even field line = (TTXOVS + 3) for M-systems line = TTXOVE for other systems PAL: TTXOVS = 0x16 NTSC: TTXOVS = 0x10
Offset 0x7A - FAL (Vertical Active Size Adjustment)				
7:0	FAL	R/W	0x24	Defines the video vertical position w.r.t vsync. First active line = FAL+4 for M-systems and = FAL+1 for other systems. Measured in lines, FAL = 0 coincides with the first field sync pulse.
Offset 0x7B - LAL (Vertical Active Size Adjustment)				
7:0	LAL	R/W	0x29	Last active line = LAL+3 for M-systems and = FAL for other systems. Measured in lines, LAL = 0 coincides with the first field sync pulse.
Offset 0x7C - TTXCTRL				
7	TTX60	R/W	0	0 = Enables NABTS (FISE=1) or European TTX (FISE=0). 1 = Enables World Standard Teletext 60Hz (FISE=1).

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
6	LAL8	R/W	1	Bit 8 of LAL
5	TTXO	R/W	0	0 =New TTX protocol selected. At each rising edge of TTXRQ a single TTX bit is requested. 1 = Old TTX protocol selected. The encoder provides a window of TTXRQ. The length of the window depends on the chosen TTX standard.
4	FAL8	R/W	0	Bit 8 of FAL
3	TTXEVE8	R/W	0	Bit 8 of TTXEVE
2	TTXOVE8	R/W	0	Bit 8 of TTXOVE
1	TTXEVS8	R/W	0	Bit 8 of TTXEVS
0	TTXOVS8	R/W	0	Bit 8 of TTXOVS
Offset 0x7D - Must be initialized to zero.				
Offset 0x7E - DTTXL				
7:0	DTTXL	R/W	0x00	Individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits. Disabled line =LINExx(50Hz field rate). Bit 7 = Line 12; Bit 0 = Line 5 The mask is only effective if the lines are enabled via TTXOVS/TTXOVE and TTXEVS/TTXEVE.
Offset 0x7F - DTTXL2				
7:0	DTTXL	R/W	0x00	Individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits. Disabled line = LINExx(50Hz field rate) Bit 7 = Line 20; Bit 0 = Line 13 The mask is only effective if the lines are enabled via TTXOVS/TTXOVE and TTXEVS/TTXEVE.
Offset 0x80 - LCNT_ARRAY_LINE*				
7:0	LCNT_ARRAY_LINE	R/W	-	Line count array programming data lower 8 bits
Offset 0x81 - LCNT_ARRAY_LINE*				
7:6	Unused		-	
5:0	LCNT_ARRAY_LINE	R/W	-	Line count array programming data upper 6 bit
Offset 0x82 - LCNT_ARRAY_ADR*				
7:4	Unused		-	
3:0	LCNT_ARRAY_ADR	R/W	-	Line count array programming address Writing to this address initiates the transfer of the data previously written into locations 80 and 81 into an internal register array.
Offset 0x83– 0x85 - LTYPE_ARRAY_LINE*				
7:0	LTYPE_ARRAY_LINE 0x83 -> LSBs 0x85 -> MSBs	R/W	-	Line type array programming data 2:0 = first index ... 23:21 = last index
Offset 0x86 - LTYPE_ARRAY_ADR*				
7:4	Unused		-	

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
3:0	LTYPE_ARRAY_ADR	R/W	-	Line type array programming address Writing to this address initiates the transfer of the data previously written into locations 83 through 85 into an internal register array.
Offset 0x87– 0x8D - LPATT_ARRAY_LINE*				
7:0	LPATT_ARRAY_LINE 0x87 -> LSBs 0x8D -> MSBs	R/W	-	Line pattern array programming data 13:4 = first duration 3:0 = first select, 2:0 = first value index ... 55:46 = last duration 45 = last select, 44:42 = last value index
Offset 0x8E - LPATT_ARRAY_ADR*				
7:3	Unused		-	
2:0	LTYPE_ARRAY_ADR	R/W	-	Line pattern array programming address Writing to this address initiates the transfer of the data previously written into locations 87 through 8D into an internal register array.
Offset 0x8F - Must be initialized to zero.				
Offset 0x90– 0x94 - GPIO5-GPIO1 (0x90=GPIO1 ... 0x94=GPIO5)*				
7	GPIO_IN_EN4	R/W	0	GPIO input enable 4
6	GPIO_IN_EN3	R/W	0	GPIO input enable 3
5	GPIO_IN_EN2	R/W	0	GPIO input enable 2
4	GPIO_IN_EN1	R/W	0	GPIO input enable 1
3	OEN	R/W	1	Output enable (Active Low)
2	STATUS	R/W	0	Write to register sets the GPIO pin if output select is set to 2'b11. Read to register returns the status of the GPIO pin if GPIO_IN_EN4 is set, otherwise it returns 0.
1:0	OUT_SEL	R/W	0	Output selection bits 00 = Selects gpio_out1 01 = Selects gpio_out2 10 = Selects gpio_out3 11 = Selects gpio_out4.
Offset 0x95 - VMUXCTL				
7	8/10-BIT	R/W	1	0 = 8-bit mode 1 =10-bit mode
6	SLICE_MODE	R/W	1	0 = Incoming data stream contains a single D1 stream. 1 = Incoming data stream is in sliced mode.
5	SLICE_DIR	R/W	0	De-slicer control determines where the extracted slice goes. 0: incoming slice 1 == outgoing slice 1 incoming slice 2 == outgoing slice 2 1: incoming slice 1 == outgoing slice 2 incoming slice 2 == outgoing slice 1

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
4:3	SEL	R/W	0x0	Data slice select mode Primary video channel: 00 = Slice 1 primary interface 01 = Slice 2 primary interface 10 = Slice 1 secondary interface 11 = Slice 2 secondary interface Secondary video channel: 00 = Slice 1 secondary interface 01 = Slice 2 secondary interface 10 = Slice 1 primary interface 11 = Slice 2 primary interface
2:0	DEMUX_MODE	R/W	0x0	Output demultiplex mode 000 = yuv422 001 = yuv444 / RGB444 010 = Reserved 011 = yuvhd (double interface mode) 100 = yuv422hd (single interface mode) All other modes are reserved.
Offset 0x96– 0x97 - Must be initialized to zero.				
Offset 0x98 - VALUE_ARRAY_ADR/EVENT_TYPE_PTR*				
7	Unused		-	
6:4	EVENT_TYPE_PTR	R/W	-	HD SYNC generator event type pointer; trigger load value
3	Unused		-	
2:0	VALUE_ARRAY_ADR	R/W	-	Value array programming address Writing to this address initiates the transfer of the data previously written into locations 0xBE through 0xC1 into an internal register array.
Offset 0x99– 0x9A - TRIGGER_LINE*				
7:0	TRIGGER_LINE	R/W	-	This value is used as a line count after trigger. register 0x99 bits 7:0 register 0x9A bits 9:8
Offset 0x9B– 0x9C - TRIGGER_DURATION*				
7:0	TRIGGER_DURATION	R/W	-	This value is used as the duration for a certain value after trigger. register 0x9B bits 7:0 register 0x9C bits 9:8
Offset 0x9D - TRIGGER_PTR*				
7:4	LCNT_PTR_TRIGGER	R/W	-	This value is used as the line count pointer after trigger.
3:2	Unused		-	
1:0	LPATT_PTR_TRIGGER	R/W	-	This value is used as the line pattern pointer after trigger.
Offset 0x9E - BLANK_Y*				
7:0	BLANK_Y	R/W	0x90	Programmable blank level for the R\Y SD-RGB/YUV channel
Offset 0x9F - BLANK_UV*				
7:0	BLANK_UV	R/W	0	Programmable blank level for the UV SD-RGB/YUV channel
Offset 0xA0 - RGB_CTRL*				

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
7:2	Unused		-	
1	DEMOFF	R/W	0	YUV to RGB matrix bypass 0 = matrix enabled 1= matrix bypassed
0	Reserved		-	
Register 0xA1 must be initialized to zero				
Offset 0xA2 - BORDER_Y				
7:0	BORDER_Y	R/W	0x80	Border color Y component for encoder operation mode. This value is R in RGB mode
Offset 0xA3 - BORDER_U				
7:0	BORDER_U	R/W	0x80	Border color U component for encoder operation mode. This value is G in RGB mode
Offset 0xA4 - BORDER_V				
7:0	BORDER_V	R/W	0x80	Border color V component for encoder operation mode. This value is B in RGB mode
Offset 0xA5 - MISCCTRL				
7	Unused		-	
6	M24/30*	W	0	Parallel video input mode select 0 =30 bit parallel video input mode 1 =24 bit parallel video input mode For details about which pins are used in 24 and 30-bit parallel modes, please refer to section 2 table 5. Always reads back '0'.
5	TRIGGER_MODE*	R/W	1	External/embedded trigger selection 0 = External VSYNC/O_E signal triggers the HD-SYNC generator 1 = D1 embedded O_E signal used to trigger the HD-SYNC generator.
4	VMODE*	R/W	1	HD video data path enable 0 = Video demultiplexer bypassed for incoming 24/30-bit full parallel video streams (DEMUX_MODE settings ignored) 1 = Video demultiplexer enabled for HD signals (DEMUX_MODE settings apply)
3	Unused		-	
2	SLEEP	R/W	0	Video DAC sleep mode powers off all analog circuitry but the band gap reference. primary video channel: DAC1-4 secondary video channel: DAC5-6
1	Unused		-	
0	PD	R/W	0	Power down mode for DACs; powers all analog circuitry primary video channel: DAC1-4 secondary video channel: DAC5-6
Offset 0xA6 - HDCTRL				

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
7	Y_TOCO	R/W	0	Y Two's complement <-> binary offset conversion 0 = Data at the output of the HD-data path are left unchanged 1 = MSB of data output of the HD-data path is inverted
6	U_TOCO	R/W	0	U Two's complement <-> binary offset conversion 0 = Data at the output of the HD-data path are left unchanged. 1 = MSB of data output of the HD-data path is inverted.
5	V_TOCO	R/W	0	V Two's complement <-> binary offset conversion 0 = Data at the output of the HD-data path are left unchanged. 1 = MSB of data output of the HD-data path is inverted.
4	Y/R_SYNC_INS_EN	R/W	0	Enables insertion of R/Y sync signals into the component signals. 0 = Embedded sync is disabled. 1 = Embedded sync is enabled.
3	U/G_SYNC_INS_EN	R/W	0	Enables insertion of G/U sync signals into the component signals. 0 = Embedded sync is disabled. 1 = Embedded sync is enabled.
2	V/B_SYNC_INS_EN	R/W	0	Enables insertion of B/V sync signals into the component signals. 0 = Embedded sync is disabled. 1 = Embedded sync is enabled.
1	SYNC_SIG_EN	R/W	0	Sync signal insertion enable 0 = No insertion of HD sync module generated sync signals - the external signals are forwarded to the sync ports. 1 = The insertion of HD sync module generated H-sync, V-sync and Blank signals is enabled. (Note: This disables external sync signals.) H-sync is derived from sync value[0]. V-sync is derived from sync value[1]. C-blank is derived from sync value[2].
0	UPSAMPLE_EN	R/W	0	Enable 422 to 444 up-sampling filter 0 = Filter switched into bypass mode 1 = Filter is active.
Offset 0xA6 - DAC6_ADJ*				
7:5	Unused		-	
4:0	DAC6_ADJ	R/W	0	DAC6 output level coarse adjustment
Offset 0xA7 - DAC5_ADJ*				
7:5	Unused		-	
4:0	DAC5_ADJ	R/W	0	DAC5 output level coarse adjustment
Offset 0xA8 - DACC_ADJ*				
7:4	Unused		-	
3:0	DACC_ADJ	R/W	0	DAC5 and 6 output level fine adjustment
Offset 0xA7 - SYNC_DELAY				
7	VBIPROG		0	0 = Programming via VBI disabled (use this mode for 24-bit parallel mode and any other mode containing non-656 compliant data). 1 = Programming via VBI enabled
6:3	Unused		-	

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
2:0	SYNC_DELAY*		1	Determines the sync-data delay for the incoming data stream and the associated H/V sync and Blank signals.
Offset 0xA8 - BLANK_R/Y - (HD Data Path only)*				
7:0	BLANK_R/Y		0x0	Blank offset for the R/Y LSBs
Offset 0xA9 - BLANK_G/U - (HD Data Path only)*				
7:0	BLANK_G/U		0x0	Blank offset for the G/U LSBs
Offset 0xAA - BLANK_B/V - (HD Data Path only)*				
7:0	BLANK_B/V		0x0	Blank offset for the B/V LSBs
Offset 0xAE - SYNC_HEIGHT1*				
7:0	SYNC_HEIGHT1		-	Sync raster height bits 7:0
Offset 0xAF - SYNC_HEIGHT2*				
7:0	SYNC_HEIGHT2	R/W	-	Sync raster height bits 15:8
Offset 0xB0 - SYNC_WIDTH1*				
7:0	SYNC_WIDTH1	R/W	-	Sync raster width bits 7:0
Offset 0xB1 - SYNC_WIDTH2*				
7:0	SYNC_WIDTH2	R/W	-	Sync raster width bits 15:8
Offset 0xB2 - SYNC_TRIGPOS_Y1*				
7:0	SYNC_TRIGPOS_Y1	R/W	-	y trigger position bits 7:0
Offset 0xB3 - SYNC_TRIGPOS_Y2*				
7:0	SYNC_TRIGPOS_Y2	R/W	-	y trigger position bits 15:8
Offset 0xB4 - SYNC_TRIGPOS_X1*				
7:0	SYNC_TRIGPOS_X1	R/W	-	x trigger position bits 7:0
Offset 0xB5 - SYNC_TRIGPOS_X2*				
7:0	SYNC_TRIGPOS_X2	R/W	-	x trigger position bits 15:8
Offset 0xB6 - SIG1*				
7:0	SIG1	R	-	Bit 7:0 primary video path signature
Offset 0xB7 - SIG2*				
7:0	SIG2	R	-	Bit 15:8 primary video path signature
Offset 0xB8 - SIG3*				
7:0	SIG3	R	-	Bit 7:0 secondary video path signature
Offset 0xB9 - SIG4*				
7:0	SIG4	R		Bit 15:8 secondary video path signature
Offset 0xBA - SIGCTRL*				
7:4	SYNC_CTRL	R/W	0x7	Number of syncs needed to trigger signature analysis [-1]
3	SIG_DONE	R	-	AND combination of signature done for primary and secondary channel
2	SIG_ENABLE	R/W	0	Signature analyzer enable signal 0 = Signature analyzer disabled 1 = Signature analyzer enabled

Table 29: PNX8510/11 video registers *...continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
1:0	SIG_SELECT	R/W	0x0	Video channel select for signature analysis 00 = Video dac 1 and video dac 5 01 = Video dac 2 and video dac 5 10 = Video dac 3 and video dac 6 11 = Video dac 4 and video dac 6
Offset 0xBC - BLANK_MSBs*				
7:6	Unused		-	
5:4	BLANK_R/Y	R/W	-	Blank offset for the HD-R/Y channel MSBs
3:2	BLANK_G/U	R/W	-	Blank offset for the HD-G/U channel MSBs
1:0	BLANK_B/V	R/W	-	Blank offset for the HD-B/V channel MSBs
Offset 0xBE - R/Y VALUE_ARRAY_LINE*				
7:0	R/Y-VALUE_ARRAY_LINE	R/W	-	R/Y Value array programming data register 0xBE bits 7:0 register 0xC1 bits 9:8
Offset 0xBF - G/U VALUE_ARRAY_LINE*				
7:0	G/U-VALUE_ARRAY_LINE	R/W	-	G/U Value array programming data register 0xBF bits 7:0 register 0xC1 bits 9:8
Offset 0xC0 - B/V VALUE_ARRAY_LINE*				
7:0	B/V-VALUE_ARRAY_LINE	R/W	-	B/V Value array programming data register 0xC0 bits 7:0 register 0xC1 bits 9:8
Offset 0xC1 - VALUE_ARRAY_LINE-MSBs*				
7:6	Unused		-	
5:4	R/Y-VALUE_ARRAY_LINE	R/W	-	R/Y Value array programming data MSBs
3:2	G/U-VALUE_ARRAY_LINE	R/W	-	G/U Value array programming data MSBs
1:0	B/V-VALUE_ARRAY_LINE	R/W	-	B/V Value array programming data MSBs
Offset 0xC2 - DAC1_ADJ*				
7:5	Unused		-	
4:0	DAC1_ADJ	R/W	0	DAC1 output level coarse adjustment
Offset 0xC3 - DAC2_ADJ*				
7:5	Unused		-	
4:0	DAC2_ADJ	R/W	0	DAC2 output level coarse adjustment
Offset 0xC4 - DAC3_ADJ*				
7:5	Unused		-	
4:0	DAC3_ADJ	R/W	0	DAC3 output level coarse adjustment
Offset 0xC5 - DAC4_ADJ*.				
7:5	Unused		-	
4:0	DAC4_ADJ	R/W	0	DAC4 output level coarse adjustment
Offset 0xC6 - DACC_ADJ*				
7:4	Unused		-	
3:0	DACC_ADJ	R/W	0	DAC1 to 4 output level fine adjustment

Table 29: PNX8510/11 video registers...*continued*

** indicates not present in secondary video channel*

Bit	Symbol	Access	Value	Description
Offset 0xC7 - HD_GAIN_RY(HD Data Path)*				
7:0	HD_GAIN_R/Y	R/W	0x00	Gain adjust for R/Y component in HD-RGB/YUV data path, two's complement number to adjust the gain from 1-0.5 to 1+-0.5 out=in x (1+ GAIN/256)
Offset 0xC8 - HD_GAIN_GU(HD Data Path)*				
7:0	HD_GAIN_G/U	R/W	0x00	Gain adjust for G/U component in HD-RGB/YUV data path, two's complement number to adjust the gain from 1-0.5 to 1+-0.5 out=in x (1+ GAIN/256)
Offset 0xC9 - HD_GAIN_BV(HD Data Path)*				
7:0	HD_GAIN_B/V	R/W	0x00	Gain adjust for B/V component in HD-RGB/YUV data path, two's complement number to adjust the gain from 1-0.5 to 1+-0.5 out=in x (1+ GAIN/256)

8.2 Audio/Clock Address Space

Table 30: PNX8510/11 Audio/Clock Registers

Bit	Symbol	Access	Value	Description
Offset 0000 - CLK_AUDIO				
7:1	Unused		-	
0	CLK_AUDIO	R/W	0	0 = I^2S is in slave mode. 1 = I^2S is in master mode.
Offset 0001 - CLK_IF Video Interface Clock				
7:5	Unused		-	
4	CLK_IF_DIV8	R/W	0	0 = default (divide by 4). 1 = divide by 8.
3	CLK_IF_DIV6	R/W	0	0 = default (divide by 3). 1 = divide by 6.
2:1	CLK_IF_DIV	R/W	0x0	00 = clk_if is input video clock divide by 1 (feed through). 01 = clk_if is input video clock divide by 2. 10 = clk_if is input video clock divide by 3/6. 11 = clk_if is input video clock divide by 4/8.
0	CLK_IF_EN	R/W	0	0 = Normal functional mode 1 = Set the clock to zero.
Offset 0002 - CLK_PROC_DIV Video Processing Clock				
7:5	Unused		-	
4	CLK_PROC_DIV8	R/W	0	0 = Divide by 4. 1 = Divide by 8.
3	CLK_PROC_DIV6	R/W	0	0 = Default (div.ide by 3). 1 = Divide by 6
2:1	CLK_PROC_DIV	R/W	0x0	00 = clk_proc is input video clock divide by 1 (feed through). 01 = clk_proc is input video clock divide by 2. 10 = clk_proc is input video clock divide by 3/6. 11 = clk_proc is input video clock divide by 4/8.

Table 30: PNX8510/11 Audio/Clock Registers*...continued*

Bit	Symbol	Access	Value	Description
0	CLK_PROC_EN	R/W	0	0 = Normal functional mode 1 = Set the clock to zero.
Offset 00F4 - I2S_SET_REG				
7:4	Unused		-	
3:0	I2S_FORMAT	R/W	0	0000 / Philips I^2S 0001 / LSB justified 16 bits 0010 / LSB justified 18 bits 0011 / LSB justified 20 bits 0100 / MSB 1000 / LSB justified 24 bits All other combinations are reserved for future use.
Offset 00F5(LSBs)– 00FB(MSBs) - FEATURE_REG				
54:47	Unused		-	
46:39	Unused		-	
38:36	Unused		-	
35:33	DE-EMPH_1	R/W	0	De-emphasis Enable the digital de-emphasis filter for this channel. 000 = Other 001 = 32 kHz 010 = 44.1 kHz 011 = 48 kHz 100 = 96 kHz
32	Unused		-	
31	MT1	R/W	0	Mute for channel1 and channel2 inside the interpolator 0 = Mute off 1 = Mute on
30:29	SOUND_FEATURE	R/W	0	Controls the mode of the sound processing filters of Bass Boost and Treble. 00 = Flat 01 = Min 10 = Min 11 = Max
28:21	MASTER_VOL_RIGHT	R/W	0	Master volume control for right channel. Two times this 8-bit value to control the volume attenuation. The range is 0 dB to $-\infty$ dB in steps of 0.25 dB.

Table 30: PNX8510/11 Audio/Clock Registers...*continued*

Bit	Symbol	Access	Value	Description
20:17	BBOOST_RIGHT	R/W	0	Bass-boost for right channel Result is dependent on the sound_feature setting [30:29]. **20:17 Flat Min Max** 0000 0 dB 0 dB 0 dB 0001 0 dB 2 dB 2 dB 0010 0 dB 4 dB 4 dB 0011 0 dB 6 dB 6 dB 0100 0 dB 8 dB 8 dB 0101 0 dB 10 dB 10 dB 0110 0 dB 12 dB 12 dB 0111 0 dB 14 dB 14 dB 1000 0 dB 16 dB 16 dB 1001 0 dB 18 dB 18 dB 1010 0 dB 18 dB 20 dB 1011 0 dB 18 dB 22 dB 1100 0 dB 18 dB 24 dB 1101 0 dB 18 dB 24 dB 1110 0 dB 18 dB 24 dB 1111 0 dB 18 dB 24 dB
16:15	TREBLE_RIGHT	R/W	0	Treble for right channel. Result is dependent on the sound_feature setting [30:29]. **16:15 Flat Min Max** 00 0 dB 0 dB 0 dB 01 0 dB 2 dB 2 dB 10 0 dB 4 dB 4 dB 11 0 dB 6 dB 6 dB
14:7	MASTER_VOL_LEFT	R/W	0	Master volume control for left channel. Two times this 8-bit value to control the volume attenuation. The range is 0 dB to $-\infty$ dB in steps of 0.25 dB.
6:3	BBOOST_LEFT	R/W	0	Bass-boost for left channel Result is dependent on the sound_feature setting [30:29]. (Refer to bboost_right [20:17] above.)
2:1	TREBLE_LEFT	R/W	0	Treble for left channel. Result is dependent on the sound_feature setting [30:29]. **16:15 Flat Min Max** 00 0 dB 0 dB 0 dB 01 0 dB 2 dB 2 dB 10 0 dB 4 dB 4 dB 11 0 dB 6 dB 6 dB
0	MTM	R/W	0	Final Master Mute for the whole interpolator 0 = Mute off 1 = Mute on
Offset 00FC - INTERPLATOR_REG1				
7	SDET_ON	R/W	0	Silence detect enable 0 = Silence detection circuit disabled 1 = Silence detection circuit enabled

Table 30: PNX8510/11 Audio/Clock Registers*...continued*

Bit	Symbol	Access	Value	Description
6	SILENCE_OVERRIDE	R/W	0	Silence override 0 = No override. Audio DAC silence switch setting depends on the silence detector circuit and or on the master_mute status. 1 = Override. The Audio DAC silence switch is activated.
5	FILTER_COMP	R/W	0	Switch between 'flat' (for the Digital Amplifier) or 'compensate' correction filter curve (for the Audio DAC). 0 = Curve for Audio DAC 1 = Curve for Digital Power Amp
4	DA_POL_INV	R/W	0	Select the polarity of the DATA to the Audio DAC = a means to control the output signal polarity. The DC and AC dither which must be added to the noise-shaper input will NOT be inverted when inverting the audio data. 0 = Non inverting data out 1 = Inverting data out
3:2	SD_VALUE	R/W	0	The number of 'zero' samples counted before the silence detector signals whether there has been digital silence: 00 = 3200 samples 01 = 4800 samples 10 = 9600 samples 11 = 19200 samples
1	Unused		-	
0	Unused		-	
Offset 00FD - INTERPOLATOR_REG2				
7:6	Unused		-	
5:4	Unused		-	
3	QUICKMUTE	R/W	0	This is an overriding quickmute on the master channel which mutes the interpolator output signal in 32 samples, using the cosine roll-off coefficients.This overrides the soft mute. 0 = Quick mute is off 1 = Quick mute on
2	MUTEMODE	R/W	0	Mute function via micro controller interface: 0 = Soft mute mode which takes 32x32 samples to mute 1 = Quick mute mode
1	Unused		-	
0	Unused		-	
Offset 00FE - Audio DAC Power On				
7:1	Unused		-	
0	PON	R/W	0	1 = Power on for audio DAC 0 = Power off for audio DAC

9. Video programming examples

Table 31 to Table 44 provide programming examples for setting up a video channel into PAL, NTSC and SECAM modes.

[PNX8510/11_VIDEO] has to be substituted with the appropriate I^2C base address for the primary or secondary video channel.

[PNX8510/11_AUDIO] has to be substituted with the appropriate I^2C base address for the primary or secondary audio channel.

Remark: The RGB and 1080i examples are applicable to the primary video channel.

9.1 NTSC Mode (CVBS/YC 27 MHz YUV422 Interface Mode)

Table 31: PNX8510/11_VIDEO

Offset	Value
bit 7 of 0x27	0x0
bit 7 of 0x54	0x0
bit 6 of 0x2D	0xE0
0x3A	0x48
bit 7 and 6 of 0x5F	0x0
bit 7 of 0x62	0x0
bit 7 of 0x2C	0x0
bit 7, 6, 5 of 0x6F	0x0
0x95	0x80
0x28	0x25
0x29	0x1C
0x5A	0x88
bit 7 of 0x5D & 0x5B	0x86
bit 7 of 0x5E & 0x5C	0xBA
bits [5:0] of 0x5D	0x2A
bits [5:0] of 0x5E	0x2E
bits [5:0] of 0x5F	0x2E
0x61	0x11
0x62	0x45
0x63-0x66	0x21F07C1F
0x6E	0x10
bit 4 of 0x7C & 0x7A	0x000
bit 6 of 0x7C & 0x7B	0x101
bits[2:0] of 0x72 & 0x70	0x102
bits [6:4] of 0x72 & 0x71	0x68C
bits [7:5] of 0x6D & 0x6C	0x0FA
bits [4:0] 0x6D	0x0

Table 32: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

9.2 PAL Mode (CVBS/YC 27 MHz YUV422 Interface Mode)

Table 33: PNX8510/11_VIDEO

Offset	Value
bit 7 of 0x27	0x0
bit 7 of 0x54	0x0
bit 6 of 0x2D	0xE0
0x3A	0x48
bit7and 6 of 0x5F	0x0
bit 7 of 0x62	0x0
bit 7 of 0x2C	0x0
bit 7, 6, 5 of 0x6F	0x0
0x95	0x80
0x28	0x21
0x29	0x1D
0x5A	0x0
bit 7 of 0x5D & 0x5B	0x7D
bit 7 of 0x5E & 0x5C	0xAF
bits [5:0] of 0x5D	0x23
bits [5:0] of 0x5E	0x35
bits [5:0] of 0x5F	0x35
0x61	0x02
0x62	0x2F
0x63-0x66	0x2A098ACB
0x6E	0x20
bit 4 of 0x7C & 0x7A	0x1B
bit 6 of 0x7C & 0x7B	0x130
bits[2:0] of 0x72 & 0x70	0x160
bits [6:4] of 0x72 & 0x71	0x65A
bits [7:5] of 0x6D & 0x6C	0x107
bits [4:0] 0x6D	0x0

Table 34: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

9.3 SECAM (CVBS/YC 27 MHz YUV422 Interface Mode)

Table 35: PNX8510/11_VIDEO

Offset	Value
bit 7 of 0x27	0x0
bit 7 of 0x54	0x0
bit 6 of 0x2D	0xE0
0x3A	0x48
bit 7 and 6 of 0x5F	0x0
bit 7 of 0x62	0x0
bit 7 of 0x2C	0x0
bit 7, 6, 5 of 0x6F	0x0
0x95	0x80
0x28	0x21
0x29	0x1D
0x5A	0x0
bit 7 of 0x5D & 0x5B	0x6A
bit 7 of 0x5E & 0x5C	0x7F
bits [5:0] of 0x5D	0x23
bits [5:0] of 0x5E	0x35
bits [5:0] of 0x5F	0x35
0x61	0x0C
0x62	0x2F
0x63-0x66	0x28A33BB2
0x6E	0x10
bit 4 of 0x7C & 0x7A	0x1B
bit 6 of 0x7C & 0x7B	0x130
bits[2:0] of 0x72 & 0x70	0x160
bits [6:4] of 0x72 & 0x71	0x65A
bits [7:5] of 0x6D & 0x6C	0x107
bits [4:0] 0x6D	0x0

Table 36: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

9.4 NTSC (RGB 27 MHz YUV422 Interface Mode

Table 37: PNX8510/11_VIDEO

Offset	Value
0x27	0x0
0x54	0x0
0x2D	0x00

Table 37: PNX8510/11_VIDEO*...continued*

Offset	Value
0x3A	0x49
0x2C	0x0
0x6F	0x0
0x95	0x80
0x28	0x1D
0x29	0x25
0x5A	0x88
bit 7 of 0x5D & 0x5B	0x86
bit 7 of 0x5E & 0x5C	0xBA
bits [5:0] of 0x5D	0x2A
bits [5:0] of 0x5E	0x2E
bits [5:0] of 0x5F	0x2E
0x61	0x11
0x62	0x45
0x63-0x66	0x21F07C1F
0x6E	0x90
bit 4 of 0x7C & 0x7A	0x000
bit 6 of 0x7C & 0x7B	0x101
bits[2:0] of 0x72 & 0x70	0x102
bits [6:4] of 0x72 & 0x71	0x68C
bits [7:5] of 0x6D & 0x6C	0x0FA
bits [4:0] 0x6D	0x0

Table 38: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

9.5 PAL (RGB 27 MHz YUV422 Interface Mode

Table 39: PNX8510/11_VIDEO

Offset	Value
0x27	0x0
0x54	0x0
0x2D	0x00
0x3A	0x49
0x2C	0x0
0x6F	0x0
0x95	0x80
0x28	0x1D
0x29	0x21
0x5A	0x0

Table 39: PNX8510/11_VIDEO*...continued*

Offset	Value
bit 7 of 0x5D & 0x5B	0x7D
bit 7 of 0x5E & 0x5C	0xAF
bits [5:0] of 0x5D	0x23
bits [5:0] of 0x5E	0x35
bits [5:0] of 0x5F	0x35
0x61	0x02
0x62	0x2F
0x63-0x66	0x2A098ACB
0x6E	0xA0
bit 4 of 0x7C & 0x7A	0x1B
bit 6 of 0x7C & 0x7B	0x130
bits[2:0] of 0x72 & 0x70	0x160
bits [6:4] of 0x72 & 0x71	0x65A
bits [7:5] of 0x6D & 0x6C	0x107
bits [4:0] 0x6D	0x0

Table 40: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

9.6 1080i (74.25 MHz Two Interface 422YUV Mode)

Table 41: PNX8510/11_VIDEO

Offset	Value
0x80	0x05
0x81	0x08
0x82	0x00
0x82	0x01
0x80	0x01
0x81	0x10
0x82	0x01
0x82	0x02
0x80	0x0E
0x81	0x18
0x82	0x02
0x82	0x03
0x80	0x19
0x81	0x06
0x82	0x03
0x82	0x04
0x80	0x05

Table 41: PNX8510/11_VIDEO*...continued*

Offset	Value
0x81	0x18
0x82	0x04
0x82	0x05
0x80	0x01
0x81	0x14
0x82	0x05
0x82	0x06
0x80	0x04
0x81	0x08
0x82	0x06
0x82	0x07
0x80	0x01
0x81	0x0C
0x82	0x07
0x82	0x08
0x80	0x0F
0x81	0x18
0x82	0x08
0x82	0x09
0x80	0x19
0x81	0x06
0x82	0x09
0x82	0x0A
0x80	0x05
0x81	0x18
0x82	0x0A
0x82	0x0B
0x80	0x00
0x81	0x00
0x82	0x0B
0x82	0x0C
0x80	0x00
0x81	0x00
0x82	0x0C
0x82	0x0D
0x80	0x00
0x81	0x00
0x82	0x0D
0x82	0x0E
0x80	0x00
0x81	0x00

Table 41: PNX8510/11_VIDEO*...continued*

Offset	Value
0x82	0x0E
0x82	0x0F
0x83	0x1C
0x84	0x00
0x85	0x00
0x86	0x00
0x86	0x01
0x83	0x14
0x84	0x05
0x85	0x00
0x86	0x01
0x86	0x02
0x83	0x14
0x84	0x03
0x85	0x00
0x86	0x02
0x86	0x03
0x83	0x0C
0x84	0x03
0x85	0x00
0x86	0x03
0x86	0x04
0x83	0x0C
0x84	0x05
0x85	0x00
0x86	0x04
0x86	0x05
0x83	0x2C
0x84	0x00
0x85	0x00
0x86	0x05
0x86	0x06
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x06
0x86	0x07
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x07

Table 41: PNX8510/11_VIDEO*...continued*

Offset	Value
0x86	0x08
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x08
0x86	0x09
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x09
0x86	0x0A
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0A
0x86	0x0B
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0B
0x86	0x0C
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0C
0x86	0x0D
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0D
0x86	0x0E
0x87	0xFB
0x88	0xF6
0x89	0xAE
0x8A	0x00
0x8B	0x00
0x8C	0x00
0x8D	0x00
0x8E	0x00
0x8E	0x01
0x87	0xF8

Table 41: PNX8510/11_VIDEO*...continued*

Offset	Value
0x88	0xF6
0x89	0xAE
0x8A	0x00
0x8B	0x00
0x8C	0x00
0x8D	0x00
0x8E	0x01
0x8E	0x02
0x87	0xBB
0x88	0x83
0x89	0xFD
0x8A	0x6E
0x8B	0xBF
0x8C	0xEF
0x8D	0x0A
0x8E	0x02
0x8E	0x03
0x87	0xB9
0x88	0x82
0x89	0xAE
0x8A	0xB0
0x8B	0x57
0x8C	0x00
0x8D	0x00
0x8E	0x03
0x8E	0x04
0x87	0xBB
0x88	0xC3
0x89	0xFE
0x8A	0xBE
0x8B	0xBF
0x8C	0xEF
0x8D	0x0A
0x8E	0x04
0x8E	0x05
0xBE	0x00
0xBF	0x9C
0xC0	0x6A
0xC1	0x2F
0x98	0x00
0x98	0x01

Table 41: PNX8510/11_VIDEO*...continued*

Offset	Value
0xBE	0x00
0xBF	0x9C
0xC0	0x6A
0xC1	0x2F
0x98	0x01
0x98	0x02
0xBE	0x66
0xBF	0x64
0xC0	0x78
0xC1	0x00
0x98	0x02
0x98	0x03
0xBE	0x33
0xBF	0xD4
0xC0	0xC0
0xC1	0x3A
0x98	0x03
0x98	0x04
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x00
0x98	0x04
0x98	0x05
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x00
0x98	0x05
0x98	0x06
0xBE	0xF6
0xBF	0x14
0xC0	0x23
0xC1	0x30
0x98	0x06
0x98	0x07
0x99	0x03
0x9A	0x00
0x9C	0x00
0x9B	0x02
0x9D	0x11

Table 41: PNX8510/11_VIDEO*...continued*

Offset	Value
0xAE	0x64
0xAF	0x04
0xB0	0x97
0xB1	0x08
0xB4	0x15
0xB5	0x00
0xB2	0x15
0xB3	0x00

Table 42: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

9.7 720p (74.25 MHz Two Interface 422YUV Mode)

Table 43: PNX8510/11_VIDEO

Offset	Value
0x80	0x05
0x81	0x08
0x82	0x00
0x82	0x01
0x80	0x14
0x81	0x0C
0x82	0x01
0x82	0x02
0x80	0x68
0x81	0x05
0x82	0x02
0x82	0x03
0x80	0x68
0x81	0x05
0x82	0x03
0x82	0x04
0x80	0x05
0x81	0x0C
0x82	0x04
0x82	0x05
0x80	0x00
0x81	0x00
0x82	0x05
0x82	0x06

Table 43: PNX8510/11_VIDEO*...continued*

Offset	Value
0x80	0x00
0x81	0x00
0x82	0x06
0x82	0x07
0x80	0x00
0x81	0x00
0x82	0x07
0x82	0x08
0x80	0x00
0x81	0x00
0x82	0x08
0x82	0x09
0x80	0x00
0x81	0x00
0x82	0x09
0x82	0x0A
0x83	0x1C
0x84	0x00
0x85	0x00
0x86	0x00
0x86	0x01
0x83	0x14
0x84	0x00
0x85	0x00
0x86	0x01
0x86	0x02
0x83	0x2C
0x84	0x00
0x85	0x00
0x86	0x02
0x86	0x03
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x03
0x86	0x04
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x04
0x86	0x05

Table 43: PNX8510/11_VIDEO*...continued*

Offset	Value
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x05
0x86	0x06
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x06
0x86	0x07
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x07
0x86	0x08
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x08
0x86	0x09
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x09
0x86	0x0A
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0A
0x86	0x0B
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0B
0x86	0x0C
0x83	0x00
0x84	0x00
0x85	0x00
0x86	0x0C
0x86	0x0D
0x83	0x00

Table 43: PNX8510/11_VIDEO*...continued*

Offset	Value
0x84	0x00
0x85	0x00
0x86	0x0D
0x86	0x0E
0x87	0x00
0x88	0x00
0x89	0x00
0x8A	0x00
0x8B	0x00
0x8C	0x00
0x8D	0x00
0x8E	0x00
0x8E	0x01
0x87	0xA8
0x88	0x2C
0x89	0x2A
0x8A	0xBB
0x8B	0x45
0x8C	0x00
0x8D	0x00
0x8E	0x01
0x8E	0x02
0x87	0x5B
0x88	0x09
0x89	0xFC
0x8A	0x09
0x8B	0x7F
0x8C	0x6E
0x8D	0x11
0x8E	0x02
0x8E	0x03
0x87	0x79
0x88	0x82
0x89	0x9E
0x8A	0xB0
0x8B	0x45
0x8C	0x00
0x8D	0x00
0x8E	0x03
0x8E	0x04
0x87	0x5B

Table 43: PNX8510/11_VIDEO*...continued*

Offset	Value
0x88	0xC9
0x89	0xFE
0x8A	0xB9
0x8B	0x7F
0x8C	0x6E
0x8D	0x11
0x8E	0x04
0x8E	0x05
0x87	0x00
0x88	0x00
0x89	0x00
0x8A	0x00
0x8B	0x00
0x8C	0x00
0x8D	0x00
0x8E	0x05
0x8E	0x06
0x87	0x00
0x88	0x00
0x89	0x00
0x8A	0x00
0x8B	0x00
0x8C	0x00
0x8D	0x00
0x8E	0x06
0x8E	0x07
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x20
0x98	0x00
0x98	0x01
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x20
0x98	0x01
0x98	0x02
0xBE	0xFF
0xBF	0x00
0xC0	0x00

Table 43: PNX8510/11_VIDEO*...continued*

Offset	Value
0xC1	0x10
0x98	0x02
0x98	0x03
0xBE	0x56
0xBF	0x00
0xC0	0x00
0xC1	0x30
0x98	0x03
0x98	0x04
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x00
0x98	0x04
0x98	0x05
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x00
0x98	0x05
0x98	0x06
0xBE	0x00
0xBF	0x00
0xC0	0x00
0xC1	0x00
0x98	0x06
0x98	0x07
0x99	0x03
0x9A	0x00
0x9C	0x00
0x9B	0x02
0x9D	0x11
0xA8	0x80
0xA9	0x00
0xAA	0x00
0xAE	0xED
0xAF	0x02
0xB0	0x71
0xB1	0x06
0xB4	0x20

Table 43: PNX8510/11_VIDEO...*continued*

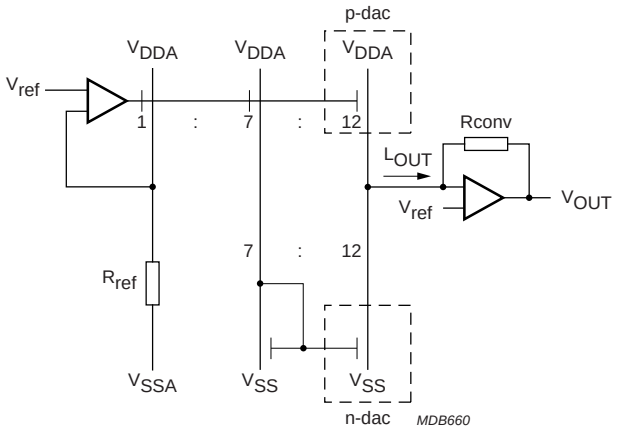
Offset	Value
0xB5	0x70
0xB	0x10
0xB3	0x70

Table 44: PNX8510/11_AUDIO

Offset	Value
0x01	0x0
0x02	0x0

10. Application information

10.1 Audio DAC



$$vout(rms) = \frac{12\alpha Rconv}{1.41Rreg} vref$$

α: max. dig. i/p level

v6.0: Rconv = 247Ω

Rref = 18000Ω

α: -5.67 dB = 0.521

=> vout(rms) = 0.607 vref

Fig 32. Simplified schematic of audio DAC

From the simplified schematic Figure 32, it can be seen that the output voltage swing depends upon:

- the maximum digital input level at low frequencies (α)
- the current mirror gain (ideally 12)
- the ratio of the I/V conversion resistance (Rconv) and the reference resistance (Rref)

This relationship is:

$Vout(rms) = 12 \cdot \alpha/\sqrt{2} \cdot Rconv/Rref \cdot Vref$

The reference resistor is dimensioned to be 18 kΩ. Since the reference voltage Vref is nominally half the supply voltage, the I/V conversion resistor must be dimensioned by:

$$Rconv = Vout(rms)/Vref \cdot \sqrt{2}/(12 \cdot \alpha) \cdot Rref$$

For an rms output voltage of 1000 mV rms, a reference voltage of 1.65 V, a reference resistance of 18 kΩ and a maximum digital input level of 0.521 (-5.67 dB), the I/V conversion resistor should be 2470 Ω.

10.2 DAC reconstruction filter

Figure 33 shows the circuitry for the reconstruction filter of the video D/A converters.

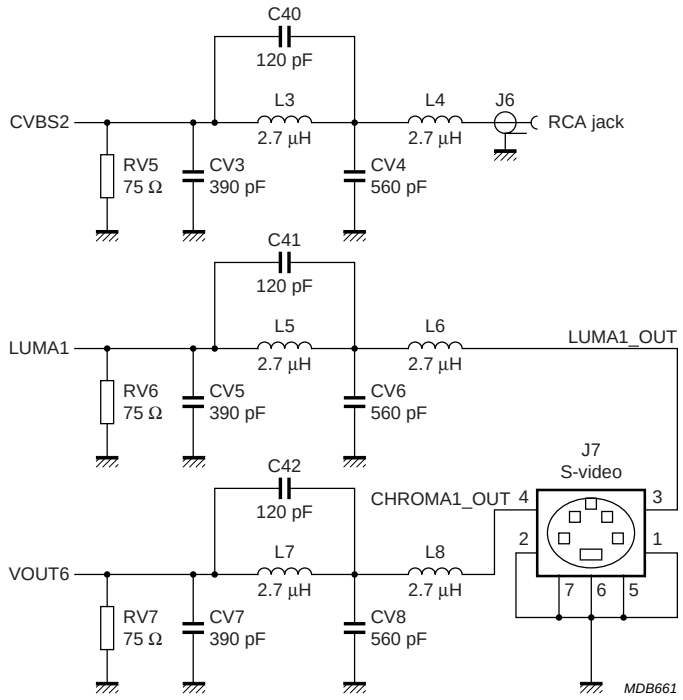


Fig 33. DAC reconstruction filter

10.3 Video DACs of primary and secondary video channels

The video DACs used in both the primary and secondary video channels employ segmented current mode architecture. The programming feature of DACs is valid for both the primary and secondary video channels.

The primary video channel has in its path four DACs: R, G, B and CVBS. The programming option “Fine Adjust” – via the common four bits of I^2C [3:0] – can simultaneously adjust the central output level of all four DACs in a range of ± 7% in 1% increments. Please note the four bits are signed values. Table 45 shows the programming values.

Table 45: Common I²C bits for all DAC devices

(Output Level: Fine Adjustment in 1% Increments)

Bits 3210	Vout
0000	0%
0001	+1%
0010	+2%
0011	+3%
0100	+4%
0101	+5%
0110	+6%
0111	+7%
1000	0%
1001	-1%
1010	-2%
1011	-3%
1100	-4%
1101	-5%
1110	-6%
1111	-7%

The programming option “Coarse Adjust” uses five separate bits [14:10] of I²C to independently adjust the output level of each R, G, B and CVBS DAC between 0.58 V and 1.23 V (in increments of 21 mV, assuming an effective load of 75 Ω / 75 Ω= 37.5 Ω). Note that these five bits are not signed.

Table 46: Separate I²C bits 31x21mV

(Output Level: Coarse Adjustment for each DAC)

Bits 11111 43210	Vout
00000	+0%
00001	+3.6%
00010	+7.2%
00011	+10.7%
00100	+14.3%
00101	+17.9%
00110	+21.5%
00111	+25.0%
01000	+28.6%
01001	+32.2%
01010	+35.8%
01011	+39.4%
01100	+42.9%
01101	+46.5%

Table 46: Separate I²C bits 31x21mV*…continued*
(Output Level: Coarse Adjustment for each DAC)

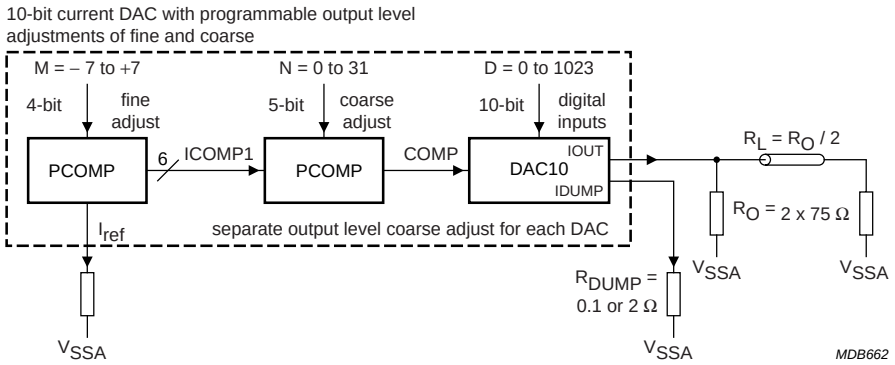
Bits 11111 43210	Vout
01110	+50.1%
01111	+53.7%
10000	+57.3%
10001	+60.8%
10010	+64.4%
10011	+68%
10100	+71.6%
10101	+75.1%
10110	+78.7%
10111	+82.3%
11000	+85.9%
11001	+89.5%
11010	+93.0%
11011	+96.6%
11100	+100.2%
11101	+103.8%
11110	+107.4%
11111	+110.9%

10.3.1 Programming example

Assuming an effective load of 75 Ω / 75 Ω= 37.5 Ω, Rset = 1 kΩ, the coarse bits are set to 0 0 0 0 and the fine adjust bits are set to 0 0 0 0 0. The output will be sitting at the minimum level of
Vout = 0.579 V.

For example, if Vout is set to 1 V, then the fine adjust bits should be set to 0 0 0 0 0 and the coarse adjust bits set to 1 0 1 0 0.

Figure 34 provides an example for calculating the RSet for the video DACs from given output voltage and termination.



RSsetnom = 1 kΩ for RL = 37.5 Ω (double termination) RSetmax = 2 kΩ for RL = 75 Ω
ICOMPn = reference currents for up to 6 DACs.

IOUT + IDUMP = 1023I1 = constant, IDUMP = (1023 - D) I1, VDUMP = IOUT x RL, VOUT = IOUT x RL.

VOUTmin = 15.57 mA x 37.5 Ω = 0.584 V (full-scale, fine adjust = 0%)

VOUTmin = 32.80 mA x 37.5 Ω = 1230 V (full-scale, fine adjust = 0%)

$$\underbrace{\left(IOUT = \left(\frac{VBG}{RS} \times \frac{16.4}{100}\right) \times 1 + \left(\frac{100+M}{100}\right) \cdot \frac{M}{100} \times \frac{28+N}{23 \times 16} \times D\right)}_{I1 = \ LSBcurrent}$$

Fig 34. Video channel DAC programming

10.3.2 Sleep and power down modes

Sleep mode occurs when all current output switches are disabled asynchronously so that no current flows in either Iout or Idump pins i.e., IOUT = IDUMP = 0. Sleep mode allows a rapid recovery from a low power consumption state. Each DAC can be put into sleep mode asynchronously where IOUT = IDUMP = 0, yet still supply current flows to power the bandgap, opmap, and other analog DAC components, including the digital logic.

Powerdown mode occurs when each DAC can be asynchronously put into zero state current so that all current output switches are disabled. This includes current to all analog and digital components of the DAC such as bandgap reference, opmaps, etc. In this mode IDDD = IDDA = 0.

10.4 Device initialization

The PNX8510/11 must be synchronously reset by providing a video clock to both clock inputs (DV_CLK1 and DV_CLK2) before the reset line (RESET_N) is pulled high. This will ensure correct initialization. Failure to follow this sequence may result in no video output from the PNX8510/11, or similar symptoms.

The I^2C bus of the PNX8510/11 is disabled during the reset of the device and the I2C_SDA pin is only released after the reset sequence is complete. This release requires that an audio clock is applied to the I2S_AOS1_CLK, in addition to the video clock applied to DV_CLK1. Therefore, even in applications which do not make use of the audio functionality of the PNX8510/11, it is still necessary to apply a clock to I2S_AOS1_CLK.

11. Limiting values

Table 47: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(ADAC)}$	Digital supply audio		3.15	3.45	V
$V_{DD(VDAC)}$	Digital supply video		3.15	3.45	V
$V_{DDA(VDAC)}$	Analog supply video		3.15	3.45	V
$V_{DDA(ADAC)}$	Analog supply audio		3.15	3.45	V
VIL	Low level input voltage		-0.5	0.8	V
VIH	High level input voltage		2.0	-	V
ILI	Input leakage current		-	1	uA
VIL	Low level input voltage		-0.5	0.3 $V_{DD(I^2C)}$	V
VIH	High level input voltage		0.7 $V_{DD(I^2C)}$	$V_{DD(I^2C)}$+0.3	V

12. Characteristics

Table 48: Electrical characteristics

Range: VDD = 3.0 to 3.6 V; Tamb = 0 to +70°C. In the following table VDD = 3.3; Tamb = 25°C, unless otherwise stated

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
Power Consumption						
SD		RGB/Y-C		1.02	1.15	W
Half HD		YPrPb		1.09	1.26	W
Full HD		YPrPb		1.58	1.97	W
Supply						
$V_{DD(ADAC)}$	Digital supply audio		3.15	3.3	3.45	V
$V_{DD(VDAC)}$	Digital supply video		3.15	3.3	3.45	V
$V_{DDA(VDAC)}$	Analog supply video		3.15	3.3	3.45	V
$V_{DDA(ADAC)}$	Analog supply audio		3.15	3.3	3.45	V
Inputs						
VIL	Low level input voltage		-0.5		0.8	V
VIH	High level input voltage		2.0			V
ILI	Input leakage current		-		1	uA
Ci	Input capacitance	clocks			10	pF
		data			8	pF
		I/Os at high impedance			8	pF
Outputs						
VOL	Low level output voltage	IOL=2mA	-		0.4	V
VOH	High level output voltage	IOH=2mA	2.4		-	V
I^2S bus: SDA, SCL						
VIL	Low level input voltage		-0.5		0.3$V_{DD(I^2C)}$	V
VIH	High level input voltage		0.7$V_{DD(I^2C)}$		$V_{DD(I^2C)}$+0.3	V

Table 48: Electrical characteristics...*continued*

Range: VDD = 3.0 to 3.6 V; Tamb = 0 to +70°C. In the following table VDD = 3.3; Tamb = 25°C, unless otherwise stated

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
VOL	Low level output voltage (SDA)	Iol=3mA	-		0.4	V
Io	Output current	during ACK	3		-	mA
Input Timing						
tsu	Input data setup time		0			ns
thd	Input data hold time		4.5			ns
Data and Reference Signal Output Timing						
GPIOs are for static use only. HSYNC out and VSYNC out are aligned to the analog video data.						
Audio DAC Outputs						
V_{out}	Full scale output voltage [1]			1.0		V_{rms}
V_{com}	Common mode output voltage [2]			1.65		V
R_{load}	Load resistance		4			kΩ
R_{out}, V_{ref}	Equivalent AC resistance seen at VREF terminal			25		kΩ
S/(THD+N)	(THD+N)/S @ 0dB, 1 kHz		88	92		dB
S/N	SNR at digital silence			95		dB(A)
DC Offset Characteristics						
V_{offset}	DC-offset compensation			-43		mV
Video DAC Outputs						
INL	Integral nonlinearity	Static	±0.6			lsb
DN			±0.5			lsb
t_r	Output rise time	Load 37.5 Ω //15pF	2.3			ns
t_f	Output fall time	Load 37.5 Ω //15pF	2.3			ns
f_{clk}	Clock frequency				100	MHz
I_{out}	Output current programming	See Section 10 for application information.				
V_{ref}				1.23		V
t_{det}	Detection threshold (comparator)				100	ns
t_{dos}	Operating to sleep delay				200	ns
t_{dop}	Operating to power down delay				200	ns
t_{dsp}	Sleep to power down delay				200	ns
t_{dso}	Sleep to operating				200	ns
t_{dpo}	Power down to operating delay				200	ns
t_{dps}	Power down to sleep delay				200	ns

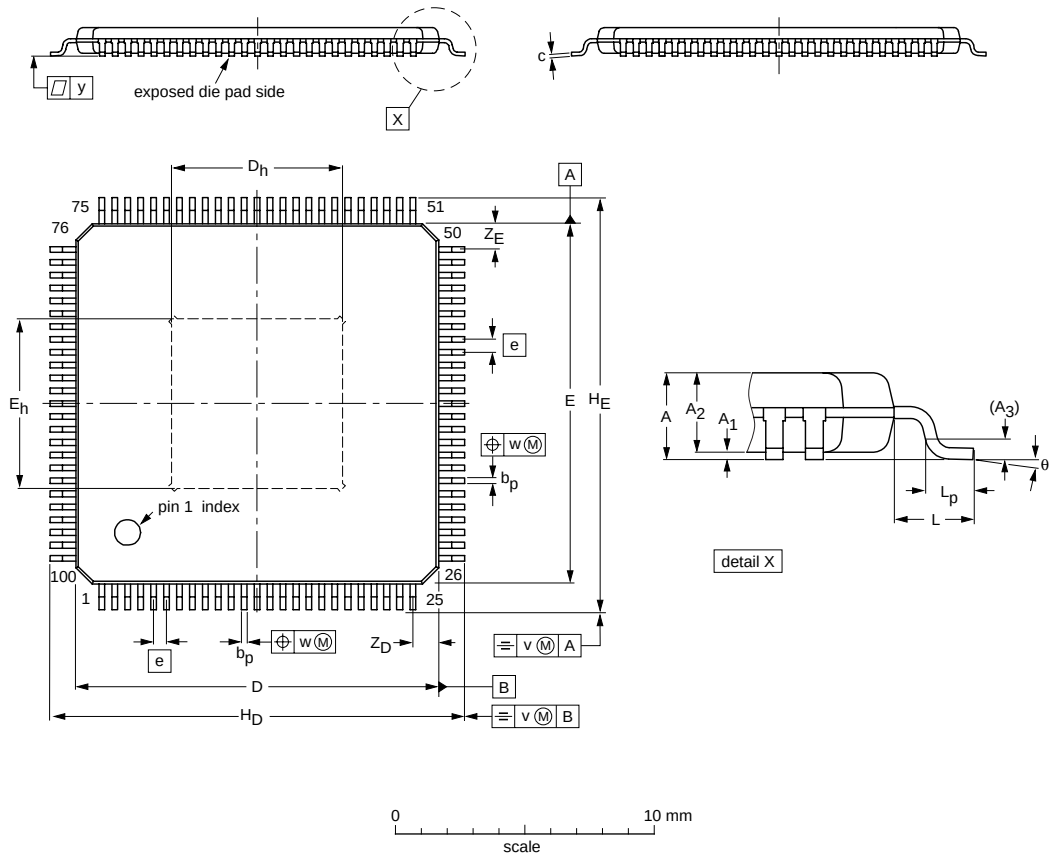
[1] Full scale output voltage is directly proportional to DC voltage at VREF pin (VDDA/2) and maximum digital signal level at low frequencies. Relation: Vout(rms) = α * 1.645 * vref/1.41, α = maximum digital input level at low frequencies.

[2] Common mode output voltage equals VREF=VDDA/2/

13. Package outline

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad

SOT638-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1						~~01-03-30~~ 03-04-07

Fig 35. HTQFP package outline.

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥Š 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Package related soldering information

Table 49: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Hot bar or manual soldering is suitable for PMFP packages.

15. Revision history

Table 50: Revision history

Rev	Date	CPCN	Description
04	**20040112**		Upgraded to Product data (9397 750 12612) Modifcations to: • Section 7.6: **Remark** amended • Section 10.4: added
03	**20030926**		Preliminary data (9397 750 09223). Major updates to docs by Hari Tadepalli of VLSI IC Engineering as requested format upgrade to DVP template. More detail added to: Luminance and Chrominance Processing, Macrovision™ and Programming Interface.
02	**20011008**	**853-2300 27221**	Supersedes initial version of 27 August 2001 (9397 750 08495). The format of this document has been redesigned to comply with Philips Semiconductors' new presentation and information standard.
01	**20010827**		Preliminary release posted on BHS (DVI) Intranet web site

16. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status

17. Definitions

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