ML6401*

8-Bit 20 MSPS A/D Converter

GENERAL DESCRIPTION

The ML6401 is a single-chip 8-bit 20 MSPS BiCMOS Video A/D Converter IC, incorporating a differential input track and hold, clock generation circuitry, and reference voltage.

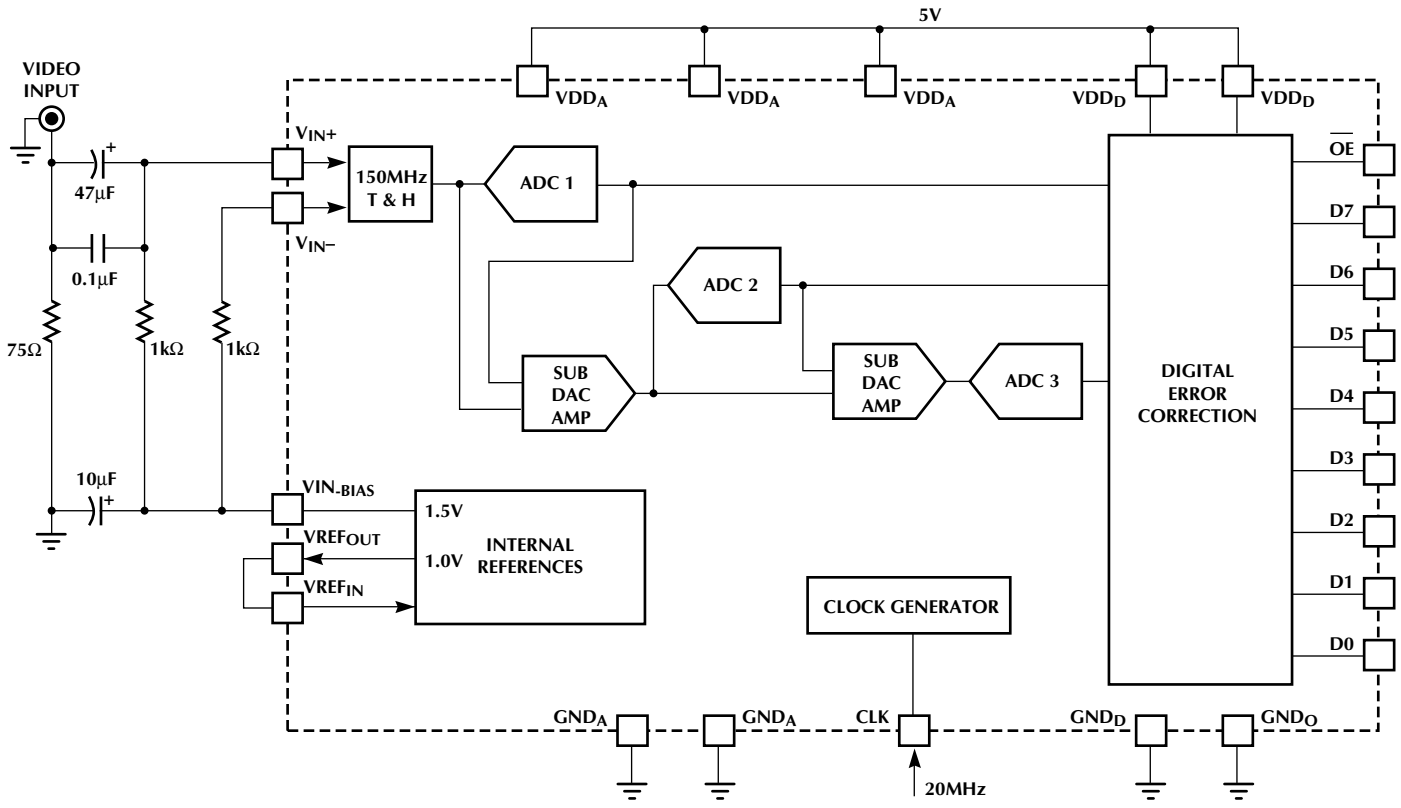
The input track and hold consists of a low (4pF) capacitance input and a fast settling operational amplifier. The A/D conversion is accomplished through a pipeline approach, reducing the number of required comparators and latches. The non-over-lapping clocks required for this architecture are all internally generated. Clock generation circuitry requires only one 50% duty cycle clock input. The use of error correction throughout the A/D converter improves DNL. All bias voltages and currents required by the A/D converter are internally generated. The digital outputs are three-stateable.

FEATURES

- 5.0V ±10% single supply operation
- Internal reference voltage
- Power dissipation less than 200mW typical
- Replaces TMC1175MC20 and AD775JR, functionally compatible to Sony CXD1175AM/AP
- 16-pin reduced pin count packages available: ML6401CS-3
- Low input capacitance track and hold: 4pF
- Onboard non-overlapping clock generation to minimize external components
- Three-state outputs and no missing codes
- 150MHz input track and hold

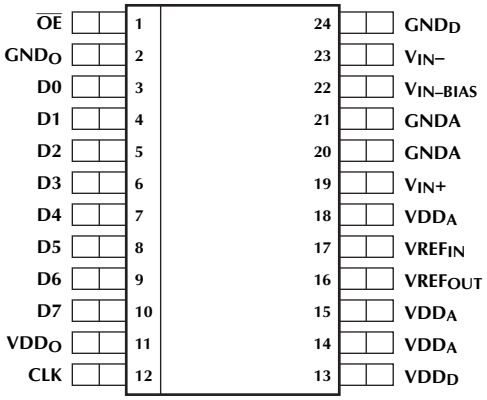
BLOCK DIAGRAM/TYPICAL APPLICATION

*Some Packages Are End Of Life



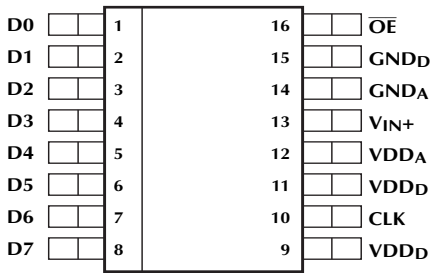
PIN CONFIGURATION

ML6401-1
24-Pin SOIC (S24W)



TOP VIEW

ML6401-3
16-Pin SOIC (S16N)



TOP VIEW

PIN DESCRIPTION (Pin numbers in parentheses are for S16N package)

PIN		NAME	DESCRIPTION
1	(16)	$\overline{OE}$	Output Enable. A logic low signal on this pin enables the outputs.
2		GND_O	Output ground pin.
3	(1)	D0	D0 (LSB) output signal (TTL compatible).
4	(2)	D1	D1 output signal (TTL compatible).
5	(3)	D2	D2 output signal (TTL compatible).
6	(4)	D3	D3 output signal (TTL compatible).
7	(5)	D4	D4 output signal (TTL compatible).
8	(6)	D5	D5 output signal (TTL compatible).
9	(7)	D6	D6 output signal (TTL compatible).
10	(8)	D7	D7 (MSB) output signal (TTL compatible).
11		VDD_O	Output supply pin.
12	(10)	CLK	Clock input pin.
13	(9,11)	VDD_D	Digital supply pin.
14	(12)	VDD_A	Analog supply pin.
15	(12)	VDD_A	Analog supply pin.
16		$VREF_{OUT}$	Full scale reference output. Connect to pin 17 for self bias. (VRTS on 1175) (ML401-1 only)
17		$VREF_{IN}$	Full scale reference input. Connect to pin 16 for self bias. (VRT on 1175) (ML401-1 only)
18	(12)	VDD_A	Analog supply pin.
19	(13)	$V_{IN}+$	Input signal.
20	(14)	GND_A	Analog ground.
21	(14)	GND_A	Analog ground.
22		$V_{IN–BIAS}$	Common mode bias output. Connect to pin 23 for self bias. (VRBS on 1175) (ML401-1 only)
23		$V_{IN}–$	Common mode bias input. Connect to pin 22 for self bias. Drive with the negative input if differential input is being used. (VRB on 1175) (ML401-1 only)
24	(15)	GND_D	Digital Ground.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 55mA
Peak Driver Output Current ..... ±500mA
Analog Inputs ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (soldering, 10 sec) ..... 150°C
Thermal Resistance (θ_{JA})
Plastic DIP ..... 80°C/W
Plastic SOIC ..... 110°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
$T_{PWH(min)} = T_{PWL(min)}$ 25ns

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, C_L = 15pF, V_{CC} = 5V ±10%, T_A = Operating Temperature Range (Note 1).

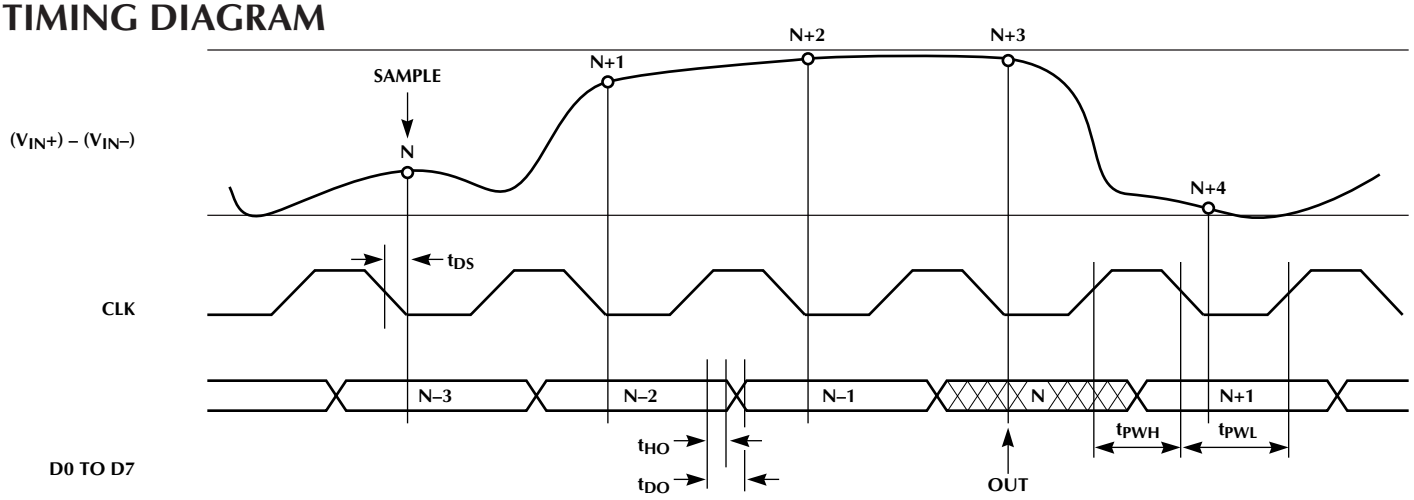
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			8		Bits
Power Dissipation			200	325	mW
Transfer Function					
DC Integral Linearity	f_{CLk} = 15MSPS		±0.8	±1.25	LSB
DC Differential Linearity	f_{CLk} = 15MSPS		±0.6	±1	LSB
AC Integral Linearity	V_{IN} = 2V, 4.4MHz			±2	LSB
Offset Voltage	V_{IN}– = $V_{IN–BIAS}$, $VREF_{OUT}$ = $VREF_{IN}$			±10	LSB
Gain Error	V_{IN}– = $V_{IN–BIAS}$, $VREF_{OUT}$ = $VREF_{IN}$		±2	±5	LSB
Analog Signal Processing					
Differential Gain	V_{IN} = NTSC 40 IRE modulated ramp, f_{CLK} = 14.3 MSPS		1.8		%
Differential Phase	V_{IN} = NTSC 40 IRE modulated ramp, f_{CLK} = 14.3 MSPS		0.9		degree
Signal to Noise Ratio	V_{IN} = 2V, 1MHz, f_{CLK} = 20MHz		48		dB
Distortion			0.18		%
Spurious Free Dynamic Range			58		dB
SIN and Distortion (SINAD)			47		dB
Effective Bits			7.4		bits
Analog Inputs					
Input Voltage	Digital Output = 0, V_{IN}– = $V_{IN–BIAS}$, $VREF_{OUT}$ = $VREF_{IN}$		0.5		V
	Digital Output = 255, V_{IN}– = $V_{IN–BIAS}$, $VREF_{OUT}$ = $VREF_{IN}$		2.5		V
Input Current	f_{CLK} = 20MHz		±20	±30	µA
Input Capacitance	V_{IN} = 2V		4.0		pF
Analog Input Bandwidth			150		MHz
Reference Outputs					
$V_{IN–BIAS}$		1.45	1.5	1.55	V
$VREF_{OUT}$	$IREF_{OUT}$ = 50µA	0.97	1.0	1.03	V
V_{RIN}				±5	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Characteristics					
Maximum CLK Input Frequency		20	25		MHz
Clock Duty Cycle	CLK = 13.5MHz	40		60	%
t_{PWH}	CLK ≤ 20MHz	25			ns
t_{PWL}	CLK ≤ 20MHz	25			ns
Analog To Digital Converter Inputs — CLK					
Low Level Input Voltage	V_{IL}	0		0.8	V
High Level Input Voltage	V_{IH}	2.4		VDD_D	V
Low Level Input Current	V_{IL} = 0.1V	–5		+5	µA
High Level Input Current	$V_{IH} = VDD_D – 0.1V$	–5		+5	µA
Input Capacitance			4.0		pF
Timing — Digital Outputs (C_L = 15pF, I_{OL} = 2mA, R_L = 2kΩ, f_{CLK} = 20MHz)					
Sampling Delay	t_{DS}		5		ns
Output Hold Time	t_{HO}	4	12	10	ns
Output Delay Time	t_{DO}	5	18	30	ns
Three-State Delay Time — Output Enable			10	25	ns
Three-State Delay Time — Output Disable			10	20	ns
Analog To Digital Converter Outputs — Digital					
Low Level Output Voltage	I_{OL} = 2mA	0		0.6	V
High Level Output Voltage	I_{OH} = 2mA	2.4		VCC_O	V
Output Current in Three-State Mode		–20		+20	µA
Supplies					
Analog, Digital & Output Supply Voltage		4.5		5.5	V
Analog Supply Current	Static		26	34	mA
Digital Supply Current	f_{CLK} = 20MHz		10	15	mA
Output Supply Current	f_{CLK} = 20MHz, C_L = 0pF		4	10	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

TIMING DIAGRAM



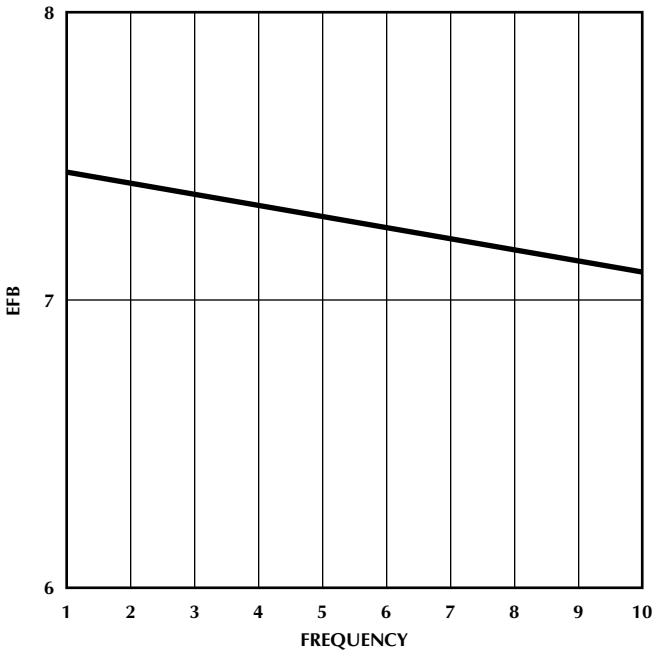
FUNCTIONAL DESCRIPTION

INTRODUCTION

The Micro Linear ML6401 is a single-chip video A/D converter IC which is intended for analog to digital conversion of 2Vp-p signals at rates up to 20MSPS. Incorporating both bias and clock generation, it forms a complete solution for data conversion. The operating power dissipation is typically less than 200mW. The IC is designed to offer low power dissipation and a high level of integration resulting in an optimized solution. The IC consists of an input track and hold, a three stage pipelined A/D converter, digital error correction circuitry, internal dual non-overlapping clock generator, and internal voltage reference.

INPUT TRACK AND HOLD

The input track and hold consists of a differential capacitor feedback amplifier. The input capacitance, including pin protection and transmission gate, is 4pF. The input to the track and hold can be driven differentially, or single-ended. Single-ended operation uses an internal or external reference to bias the negative input. The full scale range can be set externally, or supplied from an internal source. The track and hold samples the input signal during the positive half cycle of the input clock, and holds the last value of V_{IN} during the negative half cycle of the input clock. The settling time of the amplifier is less than 20ns.



Typical Effective Bits versus Input Signal Frequency.

A/D CONVERTER

The A/D conversion is performed via a three stage pipelined architecture. The first two stages quantize their input signal to three bits, then subtract the result from the input and amplify the difference by a factor of four. This creates a residue signal which spans the full scale range of the following converter. The subtraction and amplification is performed via a differential capacitor feedback amplifier, similar to the input track and hold. The third stage quantizes the signal to four bits. One bit from each of the last two stages is used for error correction.

The first stage A/D performs the conversion at the end of the track and hold period, approximately one-half cycle after the input was sampled. The second stage A/D performs the conversion one half cycle later, after the subtraction/amplification of the first stage has settled. The third stage A/D performs the conversion after another one-half cycle delay, when the second stage has settled. Error correction is then performed, and, one clock cycle later, data is transferred to the output latch. This permits the data to be read 3 clocks after the sample was taken.

This technique results in lower input capacitance, lower harmonic distortion, and higher signal to noise ratios than the classical two step parallel technique, providing a greater number of effective bits.

CLOCK GENERATION

The ML6401 typically requires an input clock that if running at 20MHz would have a low time of 25ns, and a high time of 25ns. This input is applied to a clock generation circuit which creates the two non-overlapping clock signals required by the feedback amplifiers.

Pipeline delay is the number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

INPUT COUPLING

The following two figures illustrate two simple means of connecting AC and DC coupled signals into the ML6401-1.

CXD1175 REPLACEMENT

The 24-pin ML6401-1 is pin compatible with the Sony CXD1175 since all features common to both A/D's share common pins. The 24-pin ML6401-1 is not, however, a direct replacement for the CXD1175. The architectural differences between the two parts result in slightly different application circuits only in the area of the reference pins.

The 1175 brings the top and bottom of the reference ladder to external pins (denoted VRT and VRB respectively), and provides two additional pins (VRTS and VRBS) which can be used to bias the ladder. There are three major differences in the use of the 24-pin ML6401-1. First, there is no single resistor ladder which can be brought out to users in order to vary gain and offset. Second, the 24-pin ML6401 cannot handle full scale ranges of VDDA volts. And third, where the 1175 architecture has two voltages (VRT and VRB) which fix the two endpoints of the conversion range (code 255 and code 0), the 24-pin ML6401 has one voltage (VREF) which affects only full scale range (code 255 – code 0) and one voltage (V_{IN}–) which affects only bias (code 128). An internally generated $VREF_{OUT}$ (1 volt) is brought to pin 16 (VRTS of 1175), and an internally generated $V_{IN\text{-}BIAS}$ (1.5 volts) is brought to pin 22 (VRBS of 1175). This allows the following four modes of operation:

1. **CXD1175** — See Figure 3. Connect VRTS to VRT and VRBS to VRB. The ladder will have 2 volts across it (equal to the full scale range), which varies with supply.

   ML6401 — With pin 16 connected to pin 17, and pin 22 connected to pin 23, the A/D will supply internally generated bandgap biases, making full scale range 2 volts and bias (code 128) 1.5 volts. This is a virtual drop in for an 1175 with pins 16 and 17 shorted, and pins 22 and 23 shorted (0.1 volt bias difference).

2. **CXD1175** — See Figure 4. Leave VRTS and VRBS open, and drive VRT and VRB with external voltages. The 1175 spec allows VRT-VRB to equal from 1.8 volts to VDD_A volts. This allows users the flexibility to supply higher quality references (higher precision, lower noise), and change the full scale range of the A/D (these voltages can be varied to effectively implement a VGA). Also, the offset of the A/D can be varied.

   ML6401 — Leave pin 16 and pin 22 open, and drive pin 17 and pin 23 with external voltages. The full scale range will be 2 × pin 17 volts, and the bias (code 128) will occur at pin 23 ±2% volts. The full scale range of the A/D must be kept below 4 volts, but the part is only specified for full scale range of 2 volts.

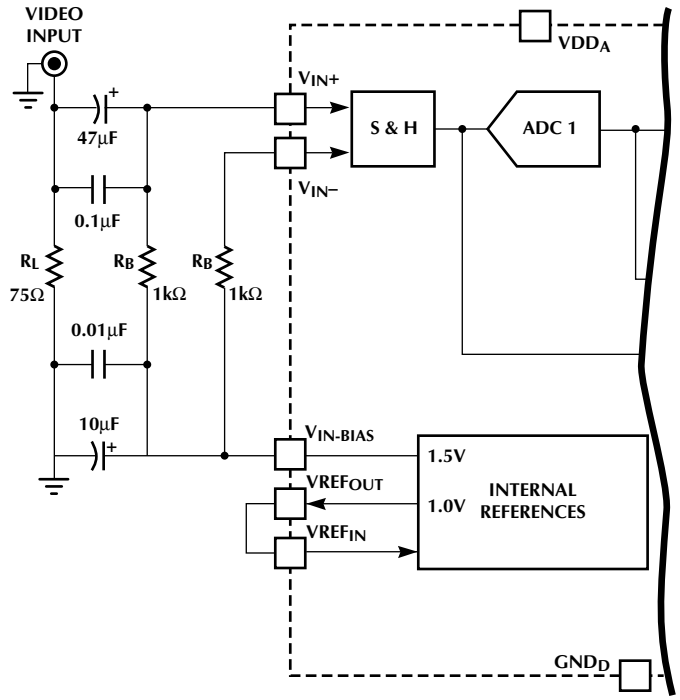


Figure 1. AC Coupled Input, External Resistors Bias the Input.

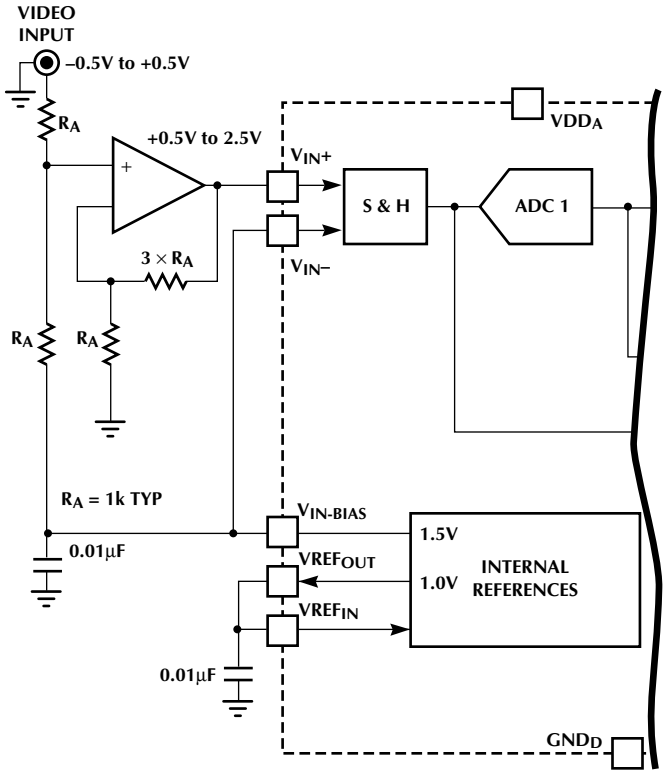
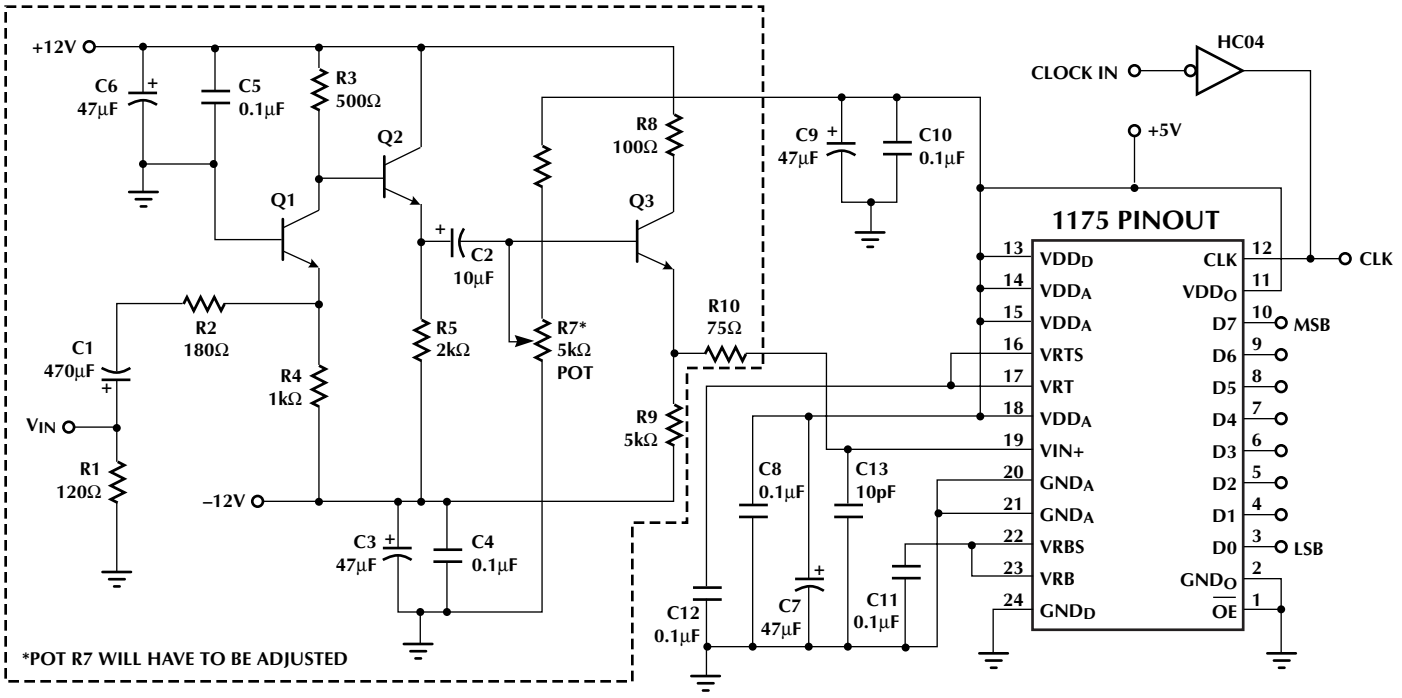


Figure 2. DC Coupled Input.



Note: Circuit in dashed lines is an optional 1175 input network which can be replaced with circuits in Figure 1 or 2.

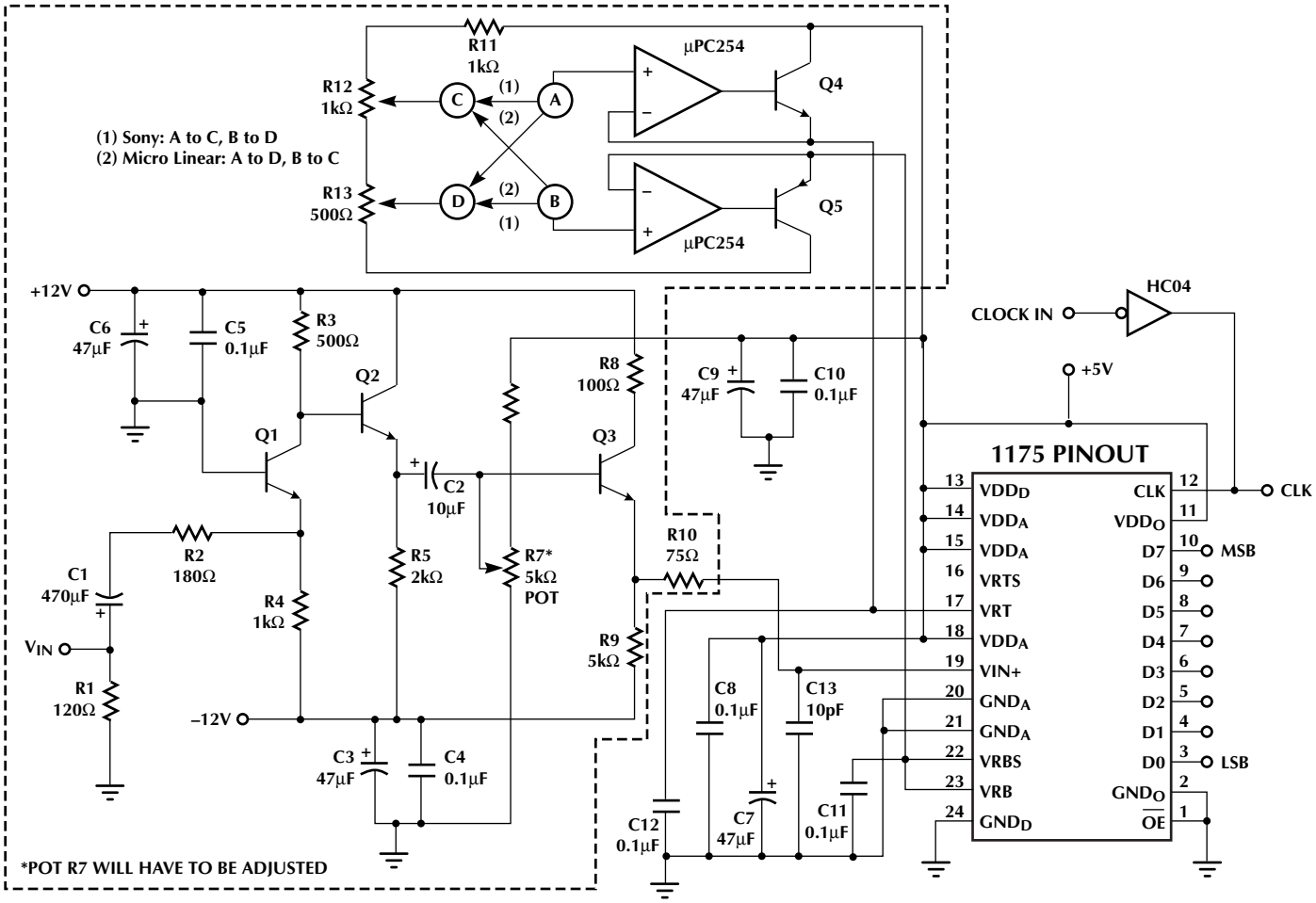
Figure 3. Replacement for 1175.

3. **CXD1175** — Connect VRBS to VRB and leave VRTS open while driving VRT with an external voltage. This allows similar functionality to #2 preceding, but the bias voltage (code 0) will move when the full scale range is changed.

   ML6401 — Open pin 16, drive pin 17 externally, and connect pin 22 to pin 23. The full scale range will be 2 × pin 17 volts, and the bias (code 128) will occur at 1.5 volts (internally generated from bandgap). The full scale range of the A/D must be kept below 4 volts, but the part is only specified for full scale range of 2 volts.

4. **CXD1175** — Connect VRTS to VRT and leave VRBS open while driving VRB with an external voltage. This allows similar functionality to #2 preceding, but the bias voltage (code 0) will move when the full scale range is changed.

   ML6401 — Connect pin 16 to pin 17, open pin 22 and drive pin 23 externally. The full scale range will be 2 volts (internally generated from bandgap), and the bias (code 128) will occur at pin 23 ±2% volts.

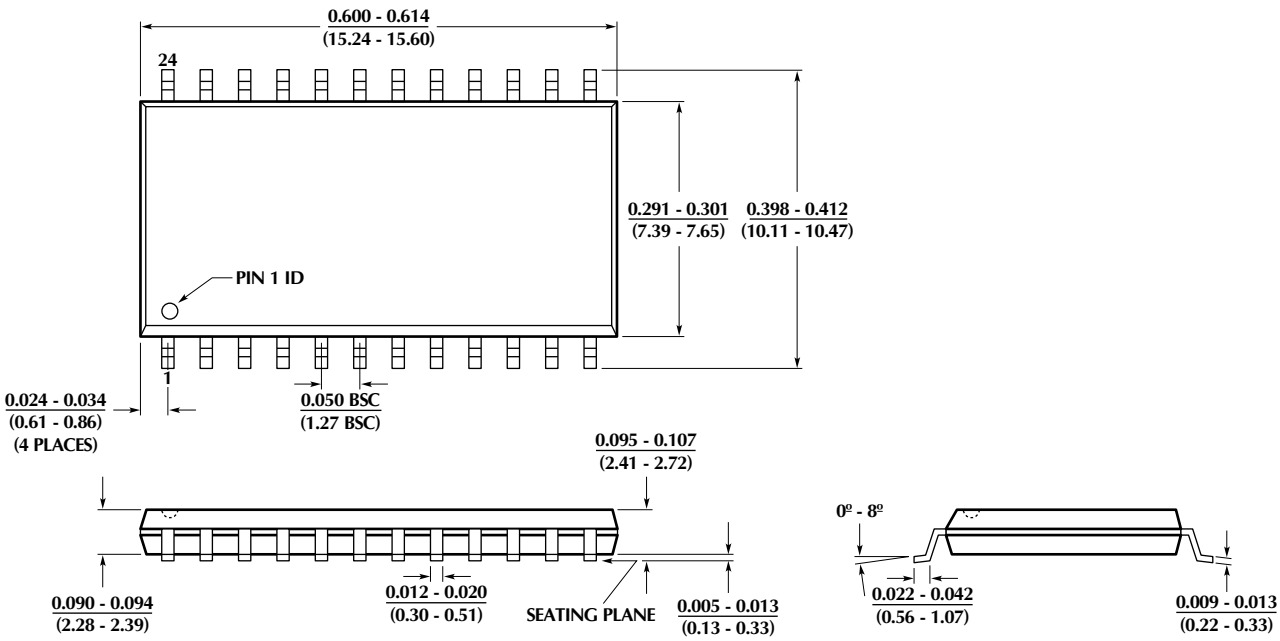


Note: Circuit in dashed lines is an optional 1175 input network which can be replaced with circuits in Figure 1 or 2.

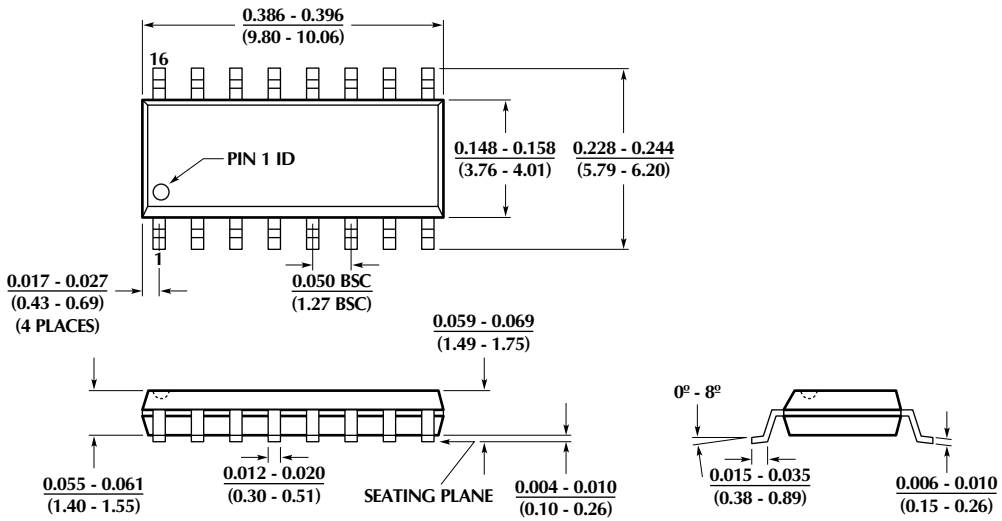
Figure 4. Replacement with Wiring Changes (shown) for the 1175.

PHYSICAL DIMENSIONS inches (millimeters)

Package: S24
24-Pin SOIC



Package: S16N
16-Pin Narrow SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6401CS-1	0°C to 70°C	24-Pin SOIC (S24)
ML6401CS-3	0°C to 70°C	16-Pin SOIC (S16N) (EOL)

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