

MINI ANALOG SERIES**0.5 μ A Rail-to-Rail CMOS OPERATIONAL AMPLIFIER****S-89430A/89431A**

The mini-analog series is a group of ICs that incorporate a general purpose analog circuit in a small package.

The S-89430A/89431A is a CMOS type operational amplifier that feature Rail-to-Rail*¹ I/O and an internal phase compensation circuit, and that can be driven at a lower voltage with lower current consumption than existing bipolar operational amplifiers. These features make this product the ideal solution for small battery-powered portable equipment.

These features enable driving at a lower voltage (from 0.9 V) and with lower current consumption (0.5 μ A)

The S-89430A/89431A is a single operational amplifier.

*1. Rail-to-Rail is a registered trademark of Motorola Inc.

■ Features

- Lower operating voltage than the conventional general-purpose operational amplifiers:

$$V_{DD} = 0.9 \text{ to } 5.5 \text{ V}$$

- Low current consumption: $I_{DD} = 0.5 \mu\text{A}$

- Wide I/O voltage range: $V_{CMR} = V_{SS} \text{ to } V_{DD}$
(Rail-to-Rail)

- Low input offset voltage: 10.0 mV (max.) (S-89430A)
5.0 mV (max.) (S-89431A)

- No external capacitors required for internal phase compensation
- Lead-free products

■ Application

- Cellular phones
- PDAs
- Notebook PCs
- Digital cameras
- Digital video cameras

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
SC-88A	NP005-B	NP005-B	NP005-B
SOT-23-5	MP005-A	MP005-A	MP005-A

■ **Product Name List**

Table 1

Input Offset Voltage	SC-88A (Single)	SOT-23-5 (Single)
$V_{IO} = 10 \text{ mV}$	S-89430ACNC-HBUTFG	S-89430ACMC-HBUT2G
$V_{IO} = 5 \text{ mV}$	S-89431ACNC-HBVTFG	S-89431ACMC-HBVT2G

Remark Delivery form : Taping only

■ **Pin Configuration**

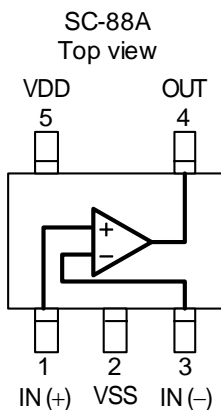


Figure 1

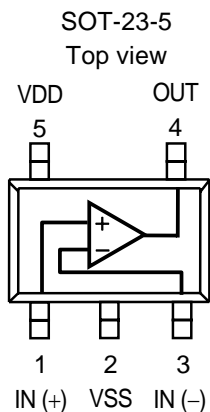


Figure 2

Table 2

Pin No.	Symbol	Description	Internal Equivalent Circuit
1	IN(+)	Non-inverted input pin	Figure 4
2	VSS	GND pin	—
3	IN(-)	Inverted input pin	Figure 4
4	OUT	Output pin	Figure 3
5	VDD	Positive power supply pin	Figure 5

■ Internal Equivalent Circuit

(1) Output pin

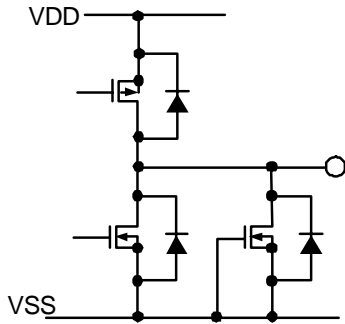


Figure 3

(2) Input pin

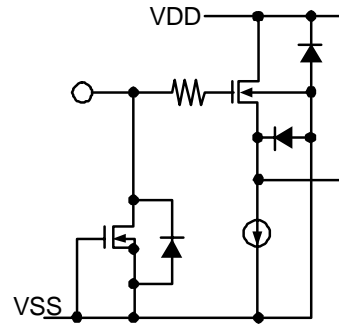


Figure 4

(3) VDD pin

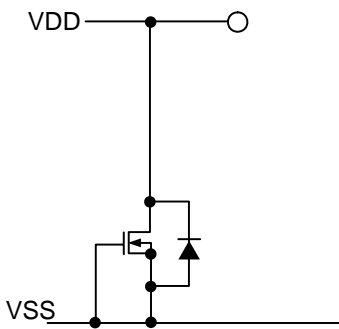


Figure 5

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Power supply voltage		V_{DD}	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Input voltage		V_{IN}	$V_{SS} - 0.3$ to $V_{SS} + 7.0$ (7.0 max.)	V
Output voltage		V_{OUT}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$ (7.0 max.)	V
Differential input voltage		V_{IND}	± 5.5	V
Output pin current		I_{SOURCE}	7.0	mA
		I_{SINK}		
Power dissipation	SC-88A	P_D	200 (When not mounted on board)	mW
			350*1	mW
	SOT-23-5		250 (When not mounted on board)	mW
			600*1	mW
Operating temperature range		T_{opr}	-40 to +85	°C
Storage temperature range		T_{stg}	-55 to +125	°C

*1. When mounted on board
 [Mounted board]

- (1) Board size : 114.3 mm \times 76.2 mm \times t1.6 mm
- (2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

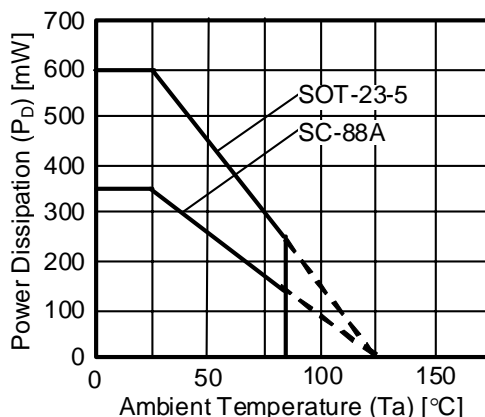


Figure 6 Power Dissipation of Package (When Mounted on Board)

■ Recommended Operating Voltage Range

Table 4

Parameter	Symbol	Range	Unit
Operating power supply voltage range	V_{DD}	0.9 to 5.5	V

■ Electrical Characteristics

1. $V_{DD} = 3.0$ V

Table 5

DC Characteristics ($V_{DD} = 3.0$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit	Measurement Circuit
Current consumption*1	I_{DD}	$V_{CMR} = V_{OUT} = 1.5$ V	—	0.5	0.9	μ A	Figure 12
Input offset voltage	V_{IO}	S-89430A : $V_{CMR} = 1.5$ V	-10	± 5	+10	mV	Figure 8
		S-89431A : $V_{CMR} = 1.5$ V	-5	± 3	+5		
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—	pA	—
Common-mode input voltage range	V_{CMR}	—	0	—	3	V	Figure 9
Voltage gain (open loop)	A_{VOL}	$V_{SS} + 0.1$ V $\leq V_{OUT} \leq V_{DD} - 0.1$ V, $V_{CMR} = 1.5$ V, $R_L = 1$ M Ω	70	80	—	dB	Figure 16
Maximum output swing voltage	V_{OH}	$R_L = 100$ K Ω	2.95	—	—	V	Figure 10
	V_{OL}	$R_L = 100$ K Ω	—	—	0.05		Figure 11
Common-mode input signal rejection ratio	CMRR	$V_{SS} \leq V_{CMR} \leq V_{DD}$	45	65	—	dB	Figure 9
Power supply voltage rejection ratio	PSRR	$V_{DD} = 0.9$ to 5.5 V	70	80	—	dB	Figure 7
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	400	500	—	μ A	Figure 13
		$V_{OUT} = 0$ V	4800	6000	—		
Sink current	I_{SINK}	$V_{OUT} = 0.1$ V	400	550	—	μ A	Figure 14
		$V_{OUT} = V_{DD}$	4800	6000	—		

*1 When the output is saturated on the V_{DD} side, a current consumption of up to 3 to 5 μ A may flow. (Refer to 4. Current consumption vs. Common-mode input voltage characteristics graphs in the characteristics data.)

Table 6

AC Characteristics ($V_{DD} = 3.0$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	$R_L = 1.0$ M Ω , $C_L = 15$ pF (Refer to Figure 15.)	—	5	—	V/ms
Gain-bandwidth product	GBP	$C_L = 0$ pF	—	4.8	—	kHz
Maximum load capacitance	C_L	—	—	47	—	pF

2. $V_{DD} = 1.8$ V

Table 7

DC Characteristics ($V_{DD} = 1.8$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit	Measurement Circuit
Current consumption *1	I_{DD}	$V_{CMR} = V_{OUT} = 0.9$ V	—	0.5	0.9	μ A	Figure 12
Input offset voltage	V_{IO}	S-89430A : $V_{CMR} = 0.9$ V	-10	± 5	+10	mV	Figure 8
		S-89431A : $V_{CMR} = 0.9$ V	-5	± 3	+5		
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—	pA	—
Common-mode input voltage range	V_{CMR}	—	0	—	1.8	V	Figure 9
Voltage gain (open loop)	A_{VOL}	$V_{SS} + 0.1$ V $\leq V_{OUT} \leq V_{DD} - 0.1$ V, $V_{CMR} = 0.9$ V, $R_L = 1$ M Ω	66	75	—	dB	Figure 16
Maximum output swing voltage	V_{OH}	$R_L = 100$ K Ω	1.75	—	—	V	Figure 10
	V_{OL}	$R_L = 100$ K Ω	—	—	0.05		Figure 11
Common-mode input signal rejection ratio	CMRR	$V_{SS} \leq V_{CMR} \leq V_{DD}$	35	55	—	dB	Figure 9
		$V_{SS} \leq V_{CMR} \leq V_{DD} - 0.3$ V	45	60	—		
Power supply voltage rejection ratio	PSRR	$V_{DD} = 0.9$ to 5.5 V	70	80	—	dB	Figure 7
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	220	300	—	μ A	Figure 13
		$V_{OUT} = 0$ V	1200	1800	—		
Sink current	I_{SINK}	$V_{OUT} = 0.1$ V	220	300	—	μ A	Figure 14
		$V_{OUT} = V_{DD}$	1200	1800	—		

*1. When the output is saturated on the V_{DD} side, a current consumption of up to 3 to 5 μ A may flow. (Refer to 4. **Current consumption vs. Common-mode input voltage characteristics** graphs in the characteristics data.)

Table 8

AC Characteristics ($V_{DD} = 1.8$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	$R_L = 1.0$ M Ω , $C_L = 15$ pF (Refer to Figure 15.)	—	4.5	—	V/ms
Gain-bandwidth product	GBP	$C_L = 0$ pF	—	5	—	kHz
Maximum load capacitance	C_L	—	—	47	—	pF

3. $V_{DD} = 0.9$ V

Table 9

DC Characteristics ($V_{DD} = 0.9$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit	Measurement Circuit
Current consumption *1	I_{DD}	$V_{CMR} = V_{OUT} = 0.45$ V	—	0.5	0.9	μ A	Figure 12
Input offset voltage	V_{IO}	S-89430A : $V_{CMR} = 0.45$ V	-10	± 5	+10	mV	Figure 8
		S-89431A : $V_{CMR} = 0.45$ V	-5	± 3	+5		
Input offset current	I_{IO}	—	—	1	—	pA	—
Input bias current	I_{BIAS}	—	—	1	—	pA	—
Common-mode input voltage range	V_{CMR}	—	0	—	0.9	V	Figure 9
Voltage gain (open loop)	A_{VOL}	$V_{SS} + 0.1$ V $\leq V_{OUT} \leq V_{DD} - 0.1$ V, $V_{CMR} = 0.45$ V, $R_L = 1$ M Ω	60	75	—	dB	Figure 16
Maximum output swing voltage	V_{OH}	$R_L = 100$ K Ω	0.85	—	—	V	Figure 10
	V_{OL}	$R_L = 100$ K Ω	—	—	0.05		Figure 11
Common-mode input signal rejection ratio	CMRR	$V_{SS} \leq V_{CMR} \leq V_{DD}$	25	55	—	dB	Figure 9
		$V_{SS} \leq V_{CMR} \leq V_{DD} - 0.35$ V	40	60	—		
Power supply voltage rejection ratio	PSRR	$V_{DD} = 0.9$ to 5.5 V	70	80	—	dB	Figure 7
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.1$ V	25	65	—	μ A	Figure 13
		$V_{OUT} = 0$ V	40	140	—		
Sink current	I_{SINK}	$V_{OUT} = 0.1$ V	10	65	—	μ A	Figure 14
		$V_{OUT} = V_{DD}$	12	120	—		

*1 When the output is saturated on the V_{DD} side, a current consumption of up to 3 to 5 μ A may flow. (Refer to 4. Current consumption vs. Common-mode input voltage characteristics graphs in the characteristics data.)

Table 10

AC Characteristics ($V_{DD} = 0.9$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	$R_L = 1.0$ M Ω , $C_L = 15$ pF (Refer to Figure 15.)	—	4	—	V/ms
Gain-bandwidth product	GBP	$C_L = 0$ pF	—	5	—	kHz
Maximum load capacitance	C_L	—	—	47	—	pF

■ Measurement Circuit

1. Power supply voltage rejection ratio

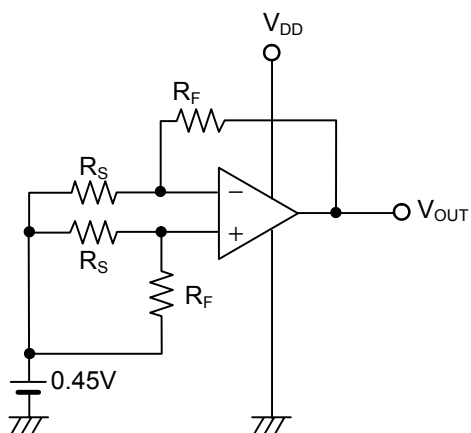


Figure 7

• Power supply voltage rejection ratio (PSRR)

The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD} .

Measurement conditions:

When $V_{DD} = 0.9\text{ V}$: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$

When $V_{DD} = 5.5\text{ V}$: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$\text{PSRR} = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

2. Input offset voltage

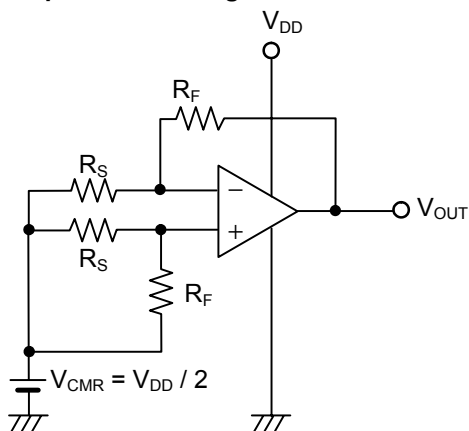


Figure 8

• Input offset voltage (V_{IO})

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

3. Common-mode input signal rejection ratio, common-mode input voltage range

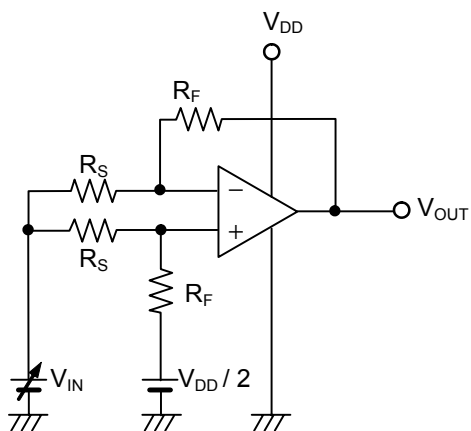


Figure 9

- **Common-mode input signal rejection ratio (CMRR)**
 The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN} .

Measurement conditions:

When $V_{IN} = V_{CMR} \text{ (max.)}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$

When $V_{IN} = V_{CMR} \text{ (min.)}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Common-mode input voltage range (V_{CMR})**
 The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications.

4. Maximum output swing voltage

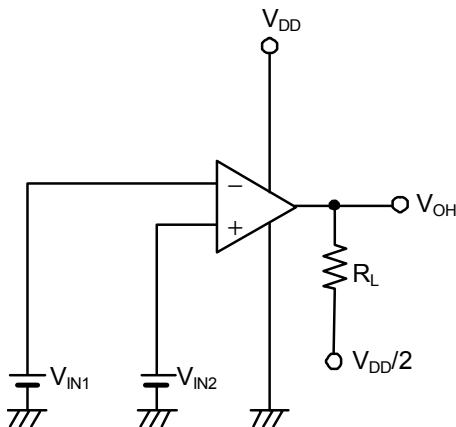


Figure 10

- **Maximum output swing voltage (V_{OH})**

Measurement conditions:

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1V$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1V$$

$$R_L = 100 \text{ K}\Omega$$

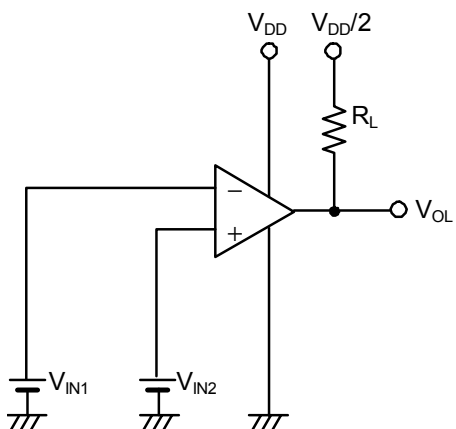


Figure 11

- **Maximum output swing voltage (V_{OL})**

Measurement conditions:

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1V$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1V$$

$$R_L = 100 \text{ K}\Omega$$

5. Current consumption

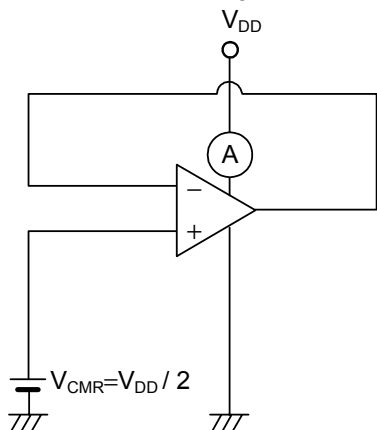


Figure 12

- Current consumption (I_{DD})

6. Source current

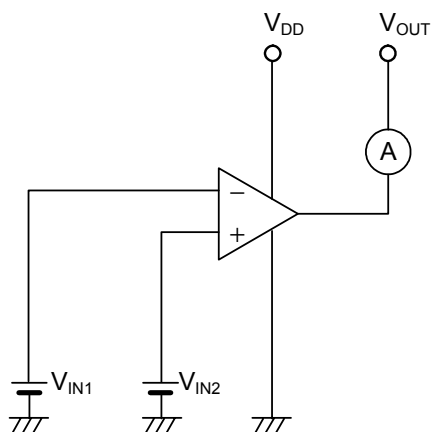


Figure 13

- Source current (I_{SOURCE})
 Measurement conditions:
 $V_{OUT} = V_{DD} - 0.1 \text{ V}$ or $V_{OUT} = 0 \text{ V}$
 $V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$
 $V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$

7. Sink current

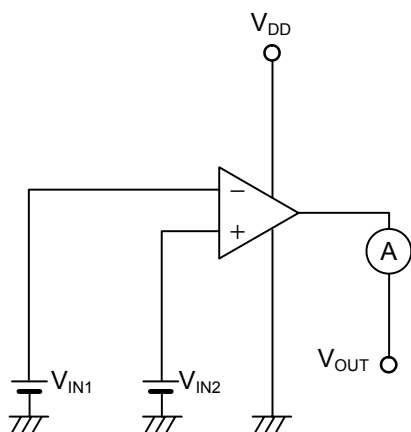


Figure 14

- Sink current (I_{SINK})
 Measurement conditions:
 $V_{OUT} = 0.1 \text{ V}$ or $V_{OUT} = V_{DD}$
 $V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$
 $V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$

8. Slew rate (SR):
 Measured by the voltage follower circuit

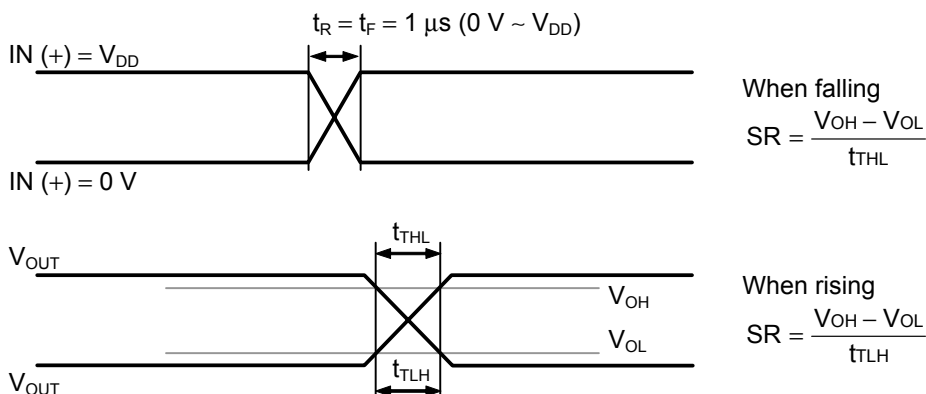


Figure 15

	When $V_{DD}=3.0$ V	When $V_{DD}=1.8$ V	When $V_{DD}=0.9$ V
V_{OH}	2.7 V	1.62 V	0.81 V
V_{OL}	0.3 V	0.18 V	0.09 V

9. Voltage gain (open loop)

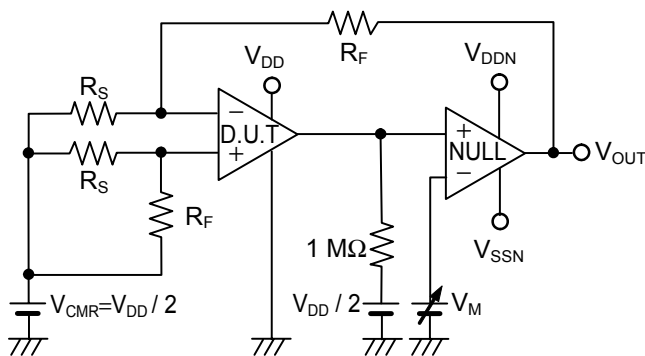


Figure 16

• **Voltage gain (open loop) (A_{VOL})**

The voltage gain (A_{VOL}) can be calculated by the following formula, with the value of V_{OUT} measured at each V_M .

Measurement conditions:

When $V_M = V_{DD} - 0.1$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$

When $V_M = 0.1$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$

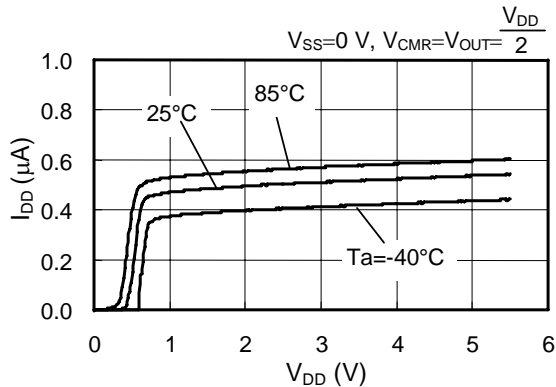
$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

■ **Precaution**

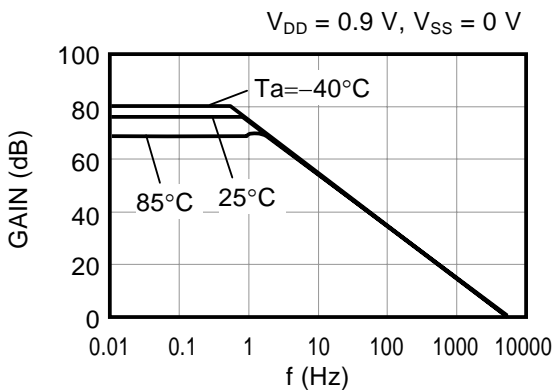
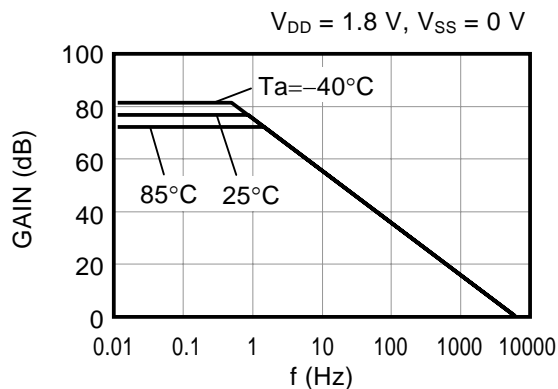
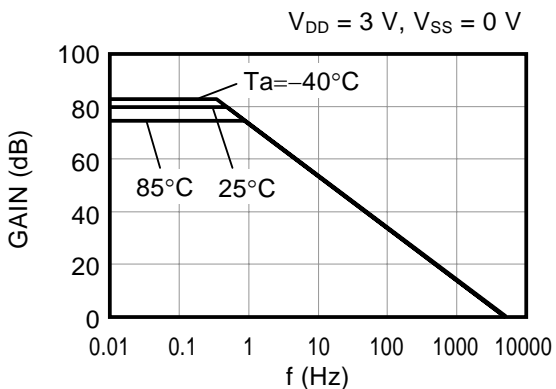
- Note that when the output is saturated on the V_{DD} side, a power supply current of up to 3 to 5 μ A may flow. (Refer to **4. Current consumption vs. Common-mode input voltage characteristics** graphs in the characteristics data)
- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.
- Be sure to use the product with an output current of no more than 7 mA.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Reference Data)

1. Current consumption vs. Power supply voltage

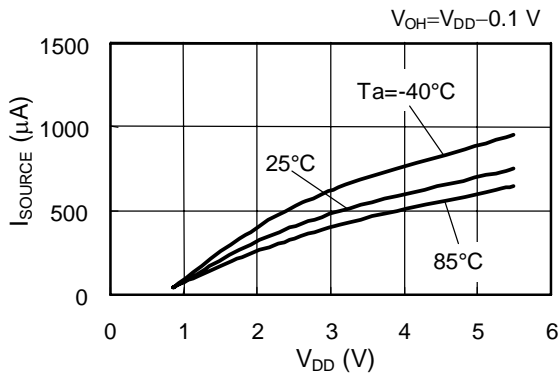


2. Voltage gain vs. Frequency

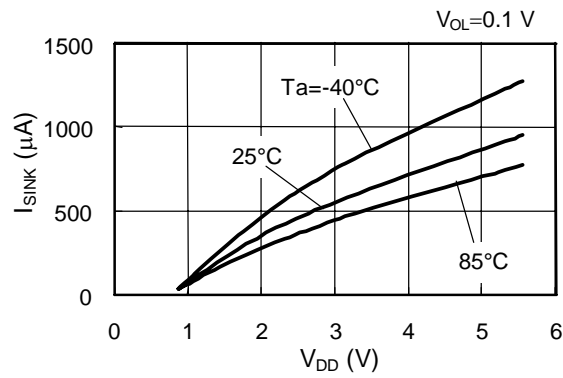


3. Output current

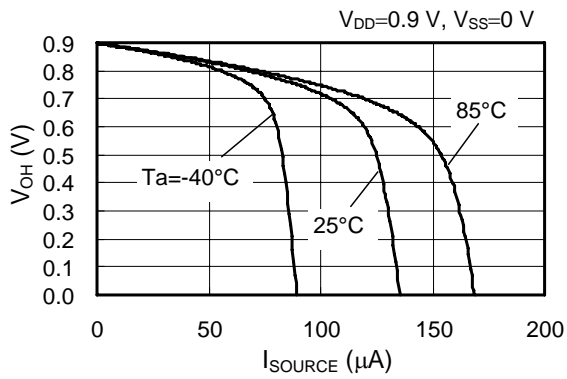
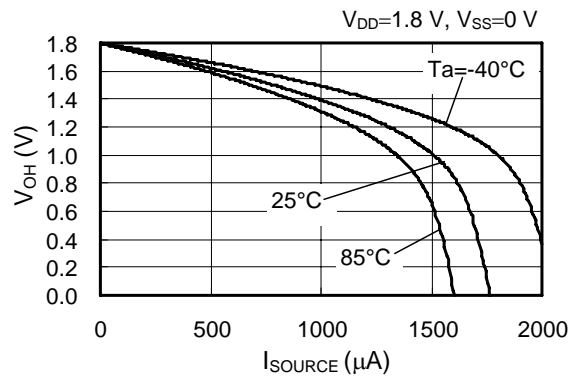
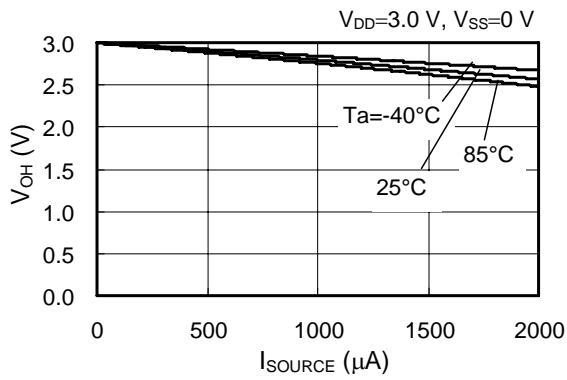
3-1. I_{SOURCE} vs. Power supply voltage



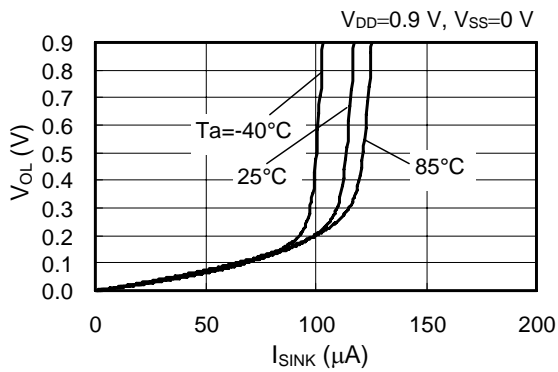
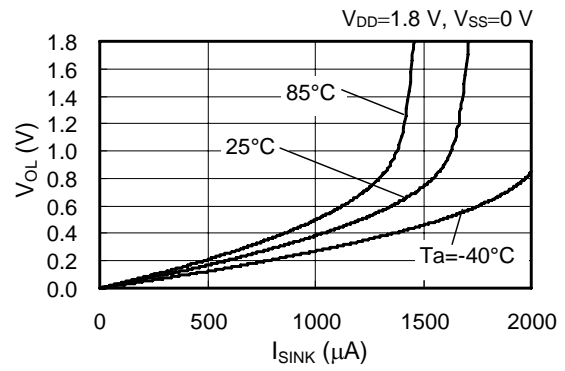
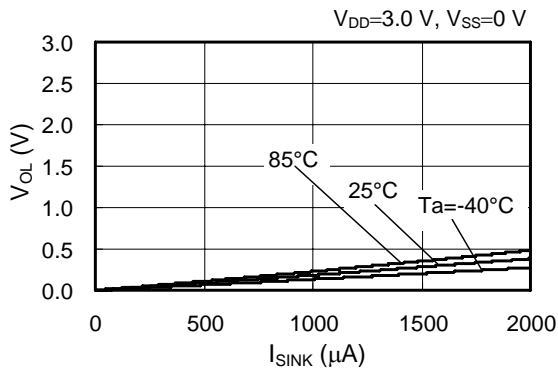
3-2. I_{SINK} vs. Power supply voltage



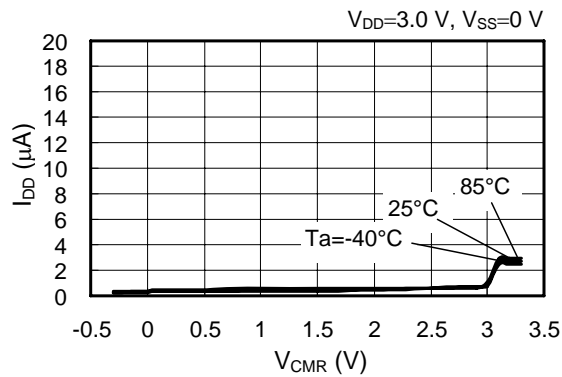
3-3. Output voltage (V_{OH}) vs I_{SOURCE}

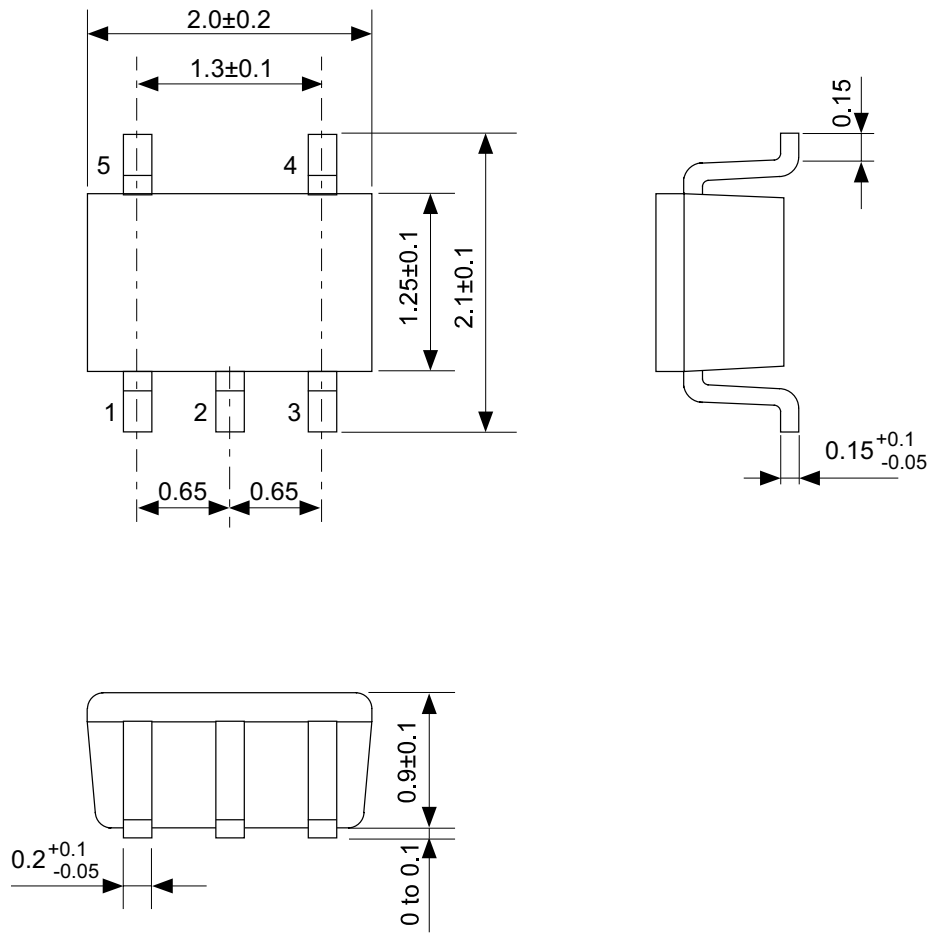


3-4. Output voltage (V_{OL}) vs. I_{SINK}



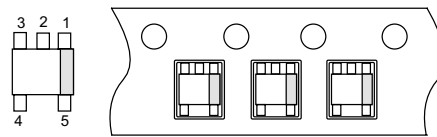
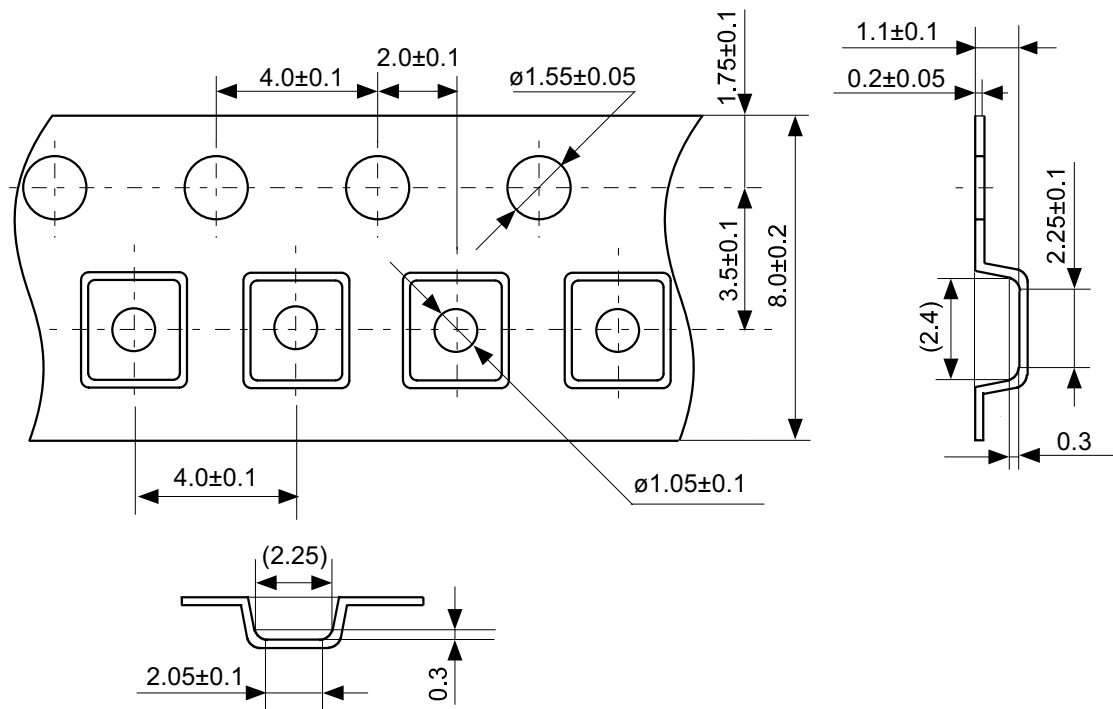
4. Current consumption vs. Common-mode input voltage (voltage follower configuration)





No. NP005-B-P-SD-1.1

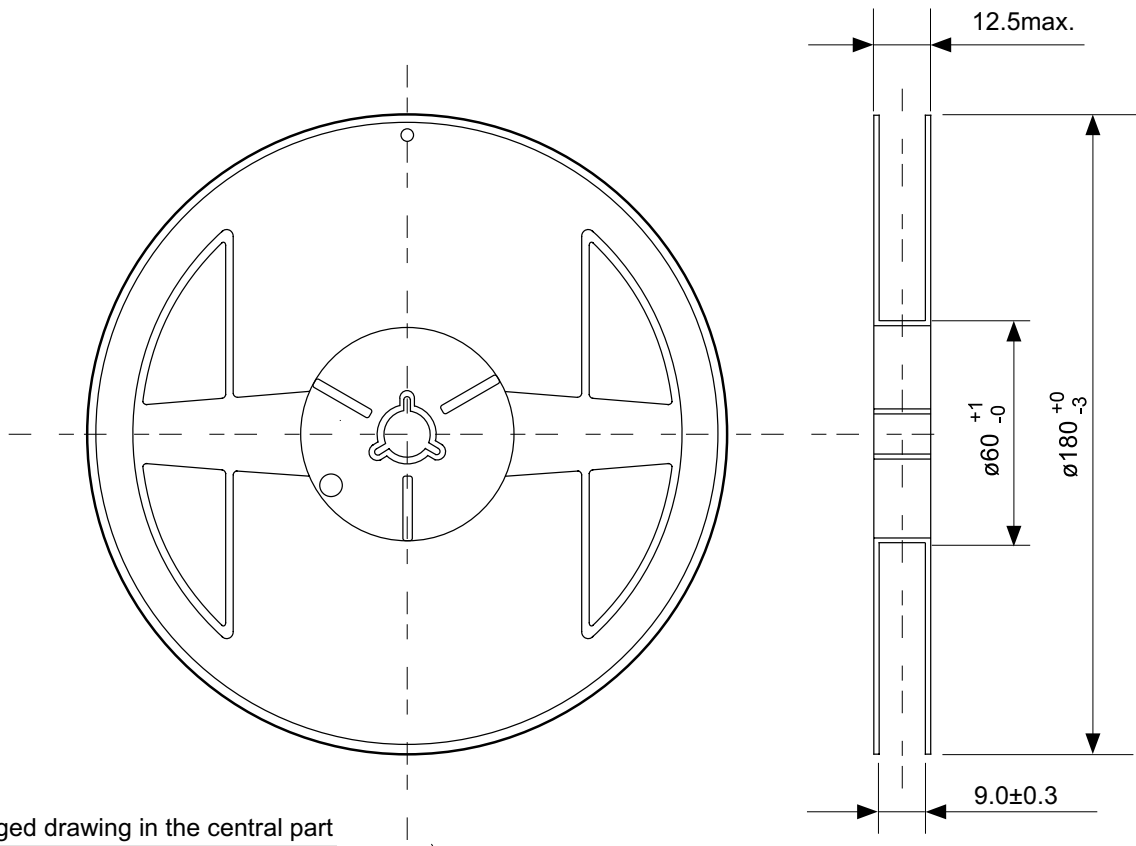
TITLE	SC88A-B-PKG Dimensions
No.	NP005-B-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



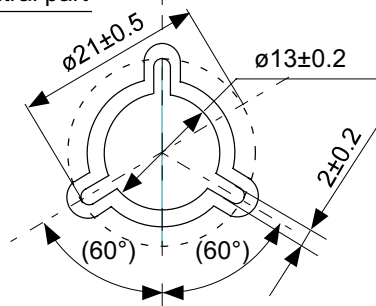
→
Feed direction

No. NP005-B-C-SD-2.0

TITLE	SC88A-B-Carrier Tape
No.	NP005-B-C-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



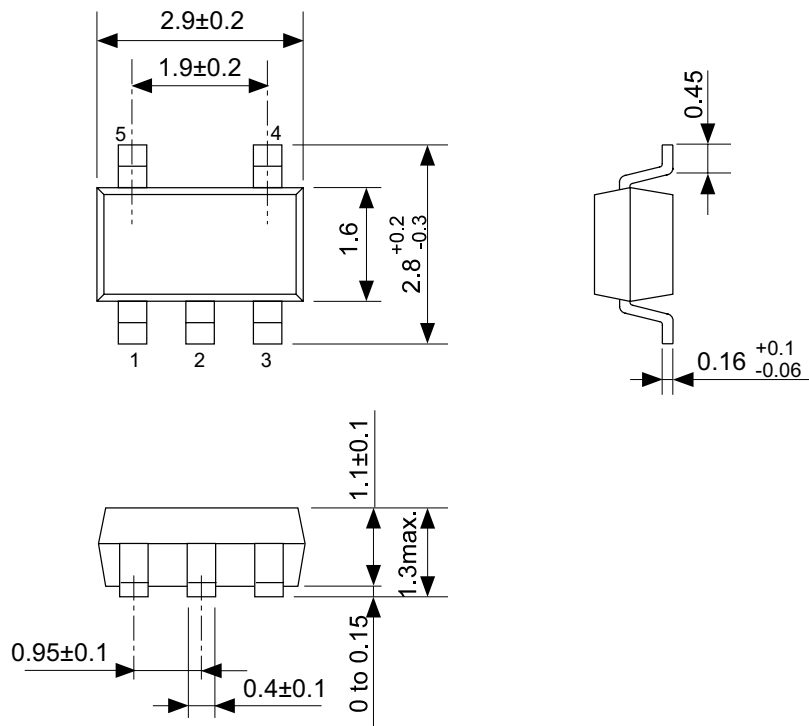
Enlarged drawing in the central part



No. NP005-B-R-SD-2.1

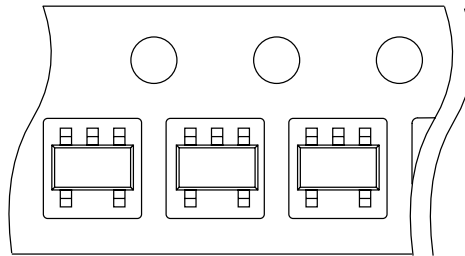
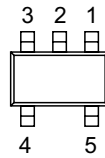
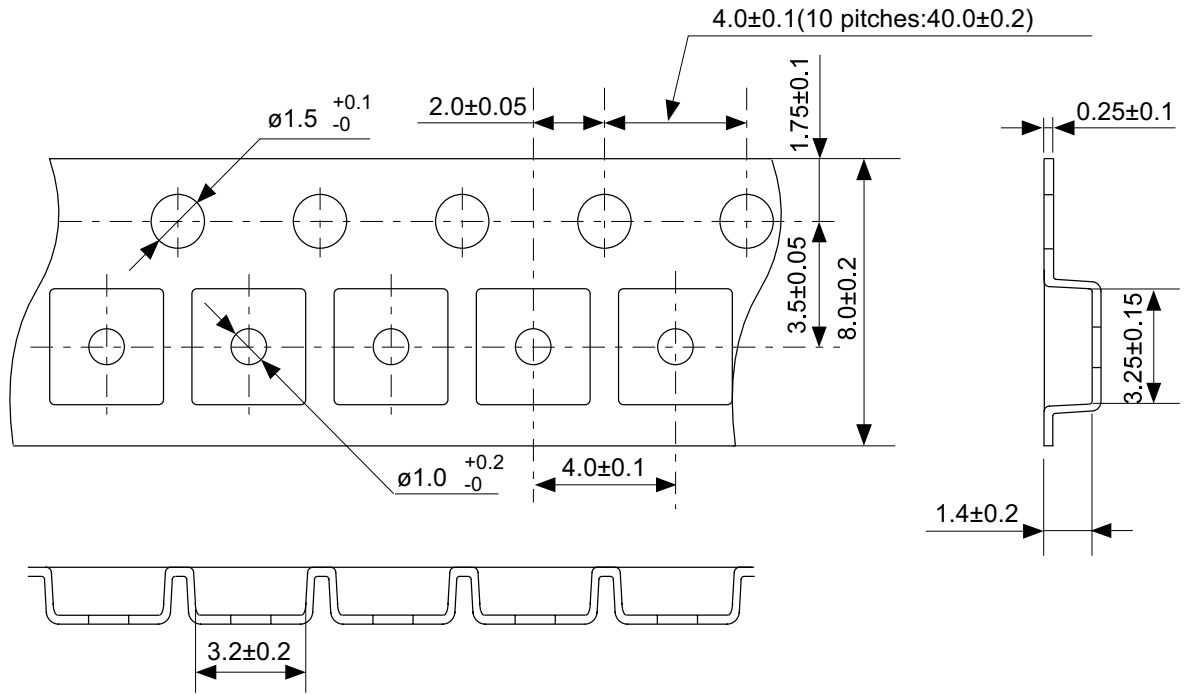
TITLE	SC88A-B-Reel		
No.	NP005-B-R-SD-2.1		
SCALE		QTY.	3000
UNIT	mm		

Seiko Instruments Inc.



No. MP005-A-P-SD-1.2

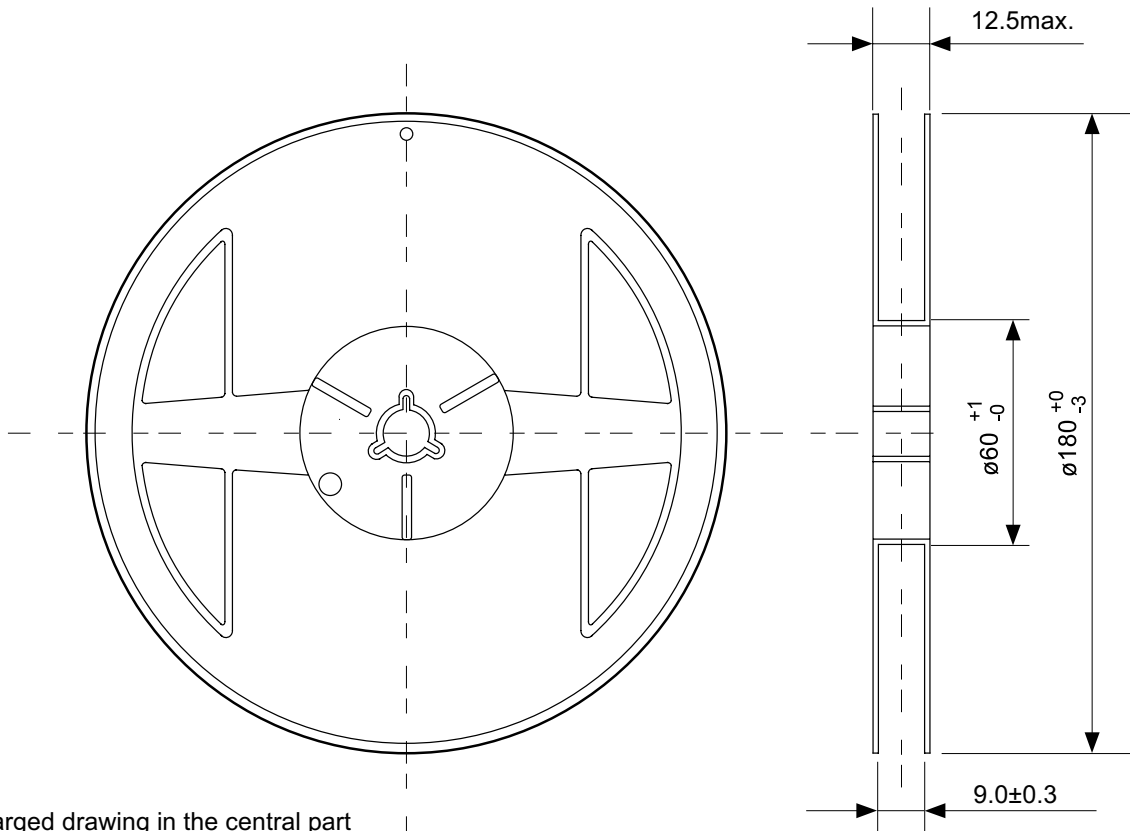
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm
Seiko Instruments Inc.	



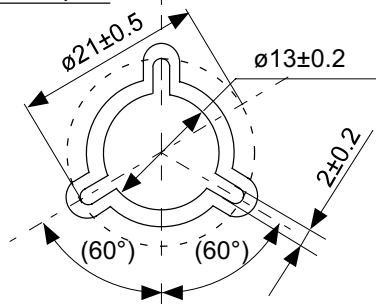
→
Feed direction

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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