May 2005

National Semiconductor

LM3661
450mA Subminiature, Micropower Step-Down DC-DC Converter for Ultra Low-Voltage Circuits

General Description

The LM3661 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Lithium-Ion cell. The device provides two pin-selectable output voltages. See ordering information for a list of voltage options available . This allows adjustment for DSP or CPU voltage options, as well as dynamic output voltage switching for reduced power consumption. Internal synchronous rectification provides high efficiency (92% typ. at 1.35V_{OUT}).

The LM3661 offers superior features and performance for mobile phones and similar portable applications. Pin-selectable PWM and Linear modes provide improved system control for maximizing battery life. During full-load, fixed frequency PWM operation reduces interference in RF and data acquisition applications by minimizing noise harmonics at sensitive IF and sampling frequencies. The SYNC/MODE input allows synchronization of the switching frequency in a range of below 500 kHz to 750 kHz to prevent noise from intermodulation with system frequencies. Linear operation reduces quiescent current to 29 µA (typ.) during system standby for extended battery life, while supplying up to 15 mA. Shutdown turns the device off and reduces battery consumption to 0.5 µA (typ.). This device offers a selectable over Current Limit to protect a variety of inductors.

The LM3661 is available in a 10 pin micro SMD package. This packaging uses National's chip-scale micro SMD technology and offers the smallest possible size. A high (600 kHz) switching frequency allows use of tiny surface-mount components; only three are required—an inductor and two ceramic capacitors.

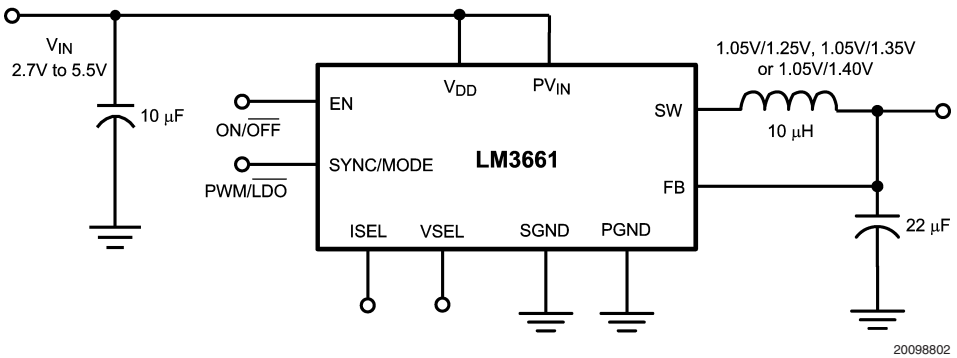
Features

- Operates from a single Li-ION cell
- Pin selectable output voltages
- Pin selectable Inductor Current Limit
- ±3% output voltage precision in PWM mode
- Miniature 10-pin micro SMD package
- Only three tiny surface-mount external components required
- Uses small ceramic capacitors
- 8 mV typ. PWM output voltage ripple
- Internal synchronous rectification for high efficiency (92% at 2.7 V_{IN}, 1.35 V_{OUT})
- 29 µA typ. quiescent current (Linear mode)
- 0.5 µA typ. shutdown current
- SYNC/MODE input for frequency synchronization from 500 kHz to 750 kHz
- Current and Thermal overload protection
- High gain control loop with internal compensation
- Up to 450mA I_{OUT} capability for LM3661-1.35/1.4
- Up to TBDmA I_{OUT} capability for LM3661-1.25

Applications

- Mobile phones
- Hand-Held radios
- Personal Digital Assistants
- Palm-top PC's and Pocket PC's
- Portable Instruments
- Battery Powered Device

Typical Application Circuit



Block Diagram

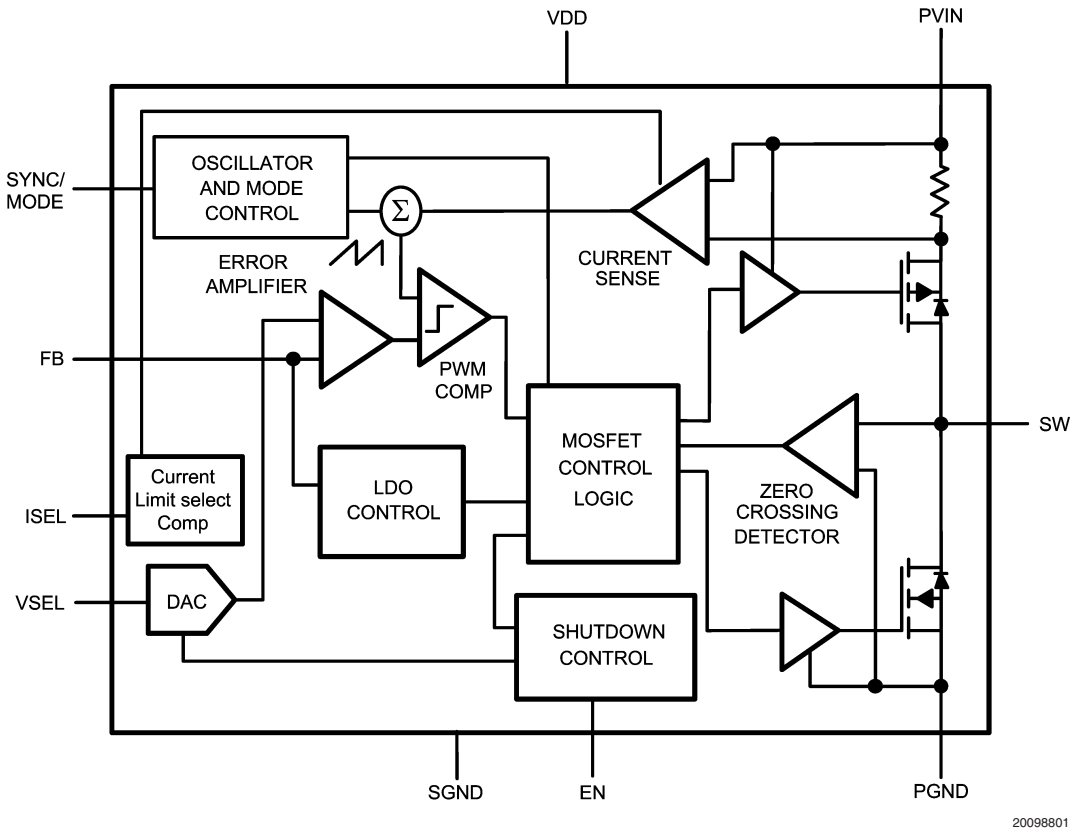
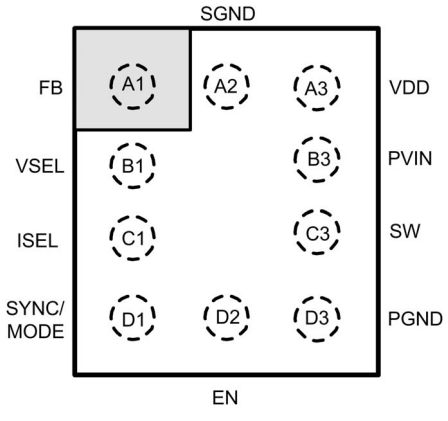


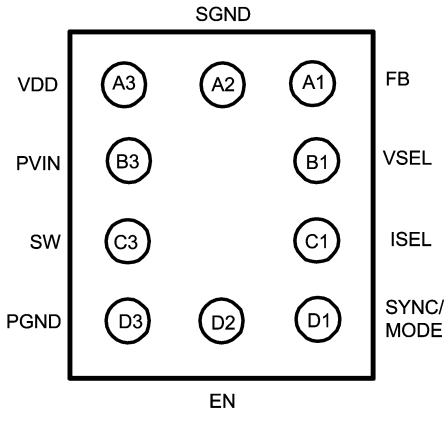
FIGURE 1. Simplified Functional Diagram

Connection Diagrams

10-Bump micro SMD Package



Top View



Bottom View

Ordering Information

Order Number	Output Voltage	Package	NSC Package Marking	Supplied As
LM3661TLX - 1.25	1.05V/1.25V	10Bump Wafer Level Chip Scale (micro SMD)	SHVB	3000 Units, Tape and Reel
LM3661TL - 1.25			SHVB	250 Units, Tape and Reel
LM3661TLX - 1.35	1.05V/1.35V		SDYB	3000 Units, Tape and Reel
LM3661TL - 1.35			SDYB	250 Units, Tape and Reel
LM3661TLX - 1.40	1.05V/1.40V		SHCB	3000 Units, Tape and Reel
LM3661TL - 1.40			SHCB	250 Units, Tape and Reel

Pin Description

Pin Number	Name	Function
A1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor (see Typical Application Circuit)
B1	V_{SEL}	Output Voltage Selection Input. Set this digital input to select the desired output voltage. Set: •V_{SEL} = high programmed ouput voltage •V_{SEL} = low for low programmed output voltage
C1	I_{SEL}	I_{SEL} = High (>1.2V) for set current limit to low value I_{SEL} = Low (GND) for set current limit to high value
D1	SYNC/MODE	Synchronization Input. Use this digital input for frequency selection or modulation control. Set: •SYNC/MODE = high for low-noise 600 kHz PWM mode •SYNC/MODE = low for micropower linear mode •SYNC/MODE = a 500 kHz -750 kHz external oscillator for synchronization to an external clock in PWM mode. The LM3661 synchronizes with the rising edge of the external clock.
D2	EN	Enable Input. It has an internal pull down resistor of 1 Mohms. Set this digital input high for normal operation. For shutdown, set low.
D3	PGND	Power Ground
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the peak current limit.
B3	PV_{IN}	Power Supply Input to the internal PFET switch. Connect to the input filter capacitor (See Typical Application Circuit).

Pin Description (Continued)

Pin Number	Name	Function
A3	V_{DD}	Analog Supply Input.
A2	SGND	Analog and Control Ground.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
PVIN, VDD to SGND	–0.2V to +6V
PGND to SGND	–0.2V to +0.2V
EN, SYNC/MODE, VSEL to SGND	–0.2V to +6V
FB, ISEL, SW	–0.2V to (VDD +0.2V)
Storage Temperature Range	–45˚C to 150˚C
Lead Temperature (Soldering, 10 sec.)	260˚C
Operating Ratings	
Input Voltage Range	2.7V to 5.5V
Operating Temperature	-30˚C to 85˚C
Junction Temperature (Note 3)	–30˚C to +125˚C
Minimum ESD Rating	
(Human Body Model, C = 100 pF, R = 1.5 kΩ)	±2 kV
Thermal properties	
Thermal Resistance (θ_{JA})	170˚C/W

Electrical Characteristics (Note 2)

Specifications with standard typeface are for T_J = 25˚C, and those in **bold face type** apply over the full Operating Temperature Range (T_A = T_J = –30˚C to +85˚C). Unless otherwise specified, PV_{IN} = V_{DD} = EN = SYNC/MODE = V_{SEL} = 3.6V, I_{SEL}= 0V, C_{OUT} = 22 µF.

Symbol	Parameter	Remarks	Min	Typ	Max	Units
$V_{FB, PWM}$	Feedback Voltage, PWM Mode V_{IN} = 2.7V to 5.5V	LM3661TL-1.25, V_{SEL} = 0	**1.019**	1.05	**1.082**	V
		LM3661TL-1.25, V_{SEL}= V_{IN}	**1.213**	1.25	**1.288**	V
		LM3661TL-1.35, V_{SEL} = 0	**1.019**	1.05	**1.082**	V
		LM3661TL-1.35, V_{SEL} = V_{IN}	**1.310**	1.35	**1.391**	V
		LM3661TL-1.40, V_{SEL} = 0	**1.019**	1.05	**1.082**	V
		LM3661TL-1.40, V_{SEL} = V_{IN}	**1.358**	1.40	**1.442**	V
$V_{FB, LINEAR}$	Feedback Voltage, Linear Mode V_{IN}= 2.7V to 5.5V, I_{OUT} = 1mA	LM3661TL-1.25, V_{SEL} = 0	**0.998**	1.05	**1.103**	V
		LM3661TL-1.25, V_{SEL}= V_{IN}	**1.188**	1.25	**1.313**	V
		LM3661TL-1.35, V_{SEL} = 0	**0.998**	1.05	**1.103**	V
		LM3661TL-1.35, V_{SEL} = V_{IN}	**1.283**	1.35	**1.418**	V
		LM3661TL-1.4, V_{SEL}= 0	**0.998**	1.05	**1.103**	V
		LM3661TL-1.4, V_{SEL}= V_{IN}	**1.33**	1.4	**1.47**	V
V_{OVP}	OVP Comparator Hysteresis Voltage (Note 5)	SYNC/MODE = V_{IN} V_{IN} = 2.7V to 5.5V		64	**90**	mV
	OVP Trip point	SYNC/MODE = V_{IN} V_{IN} = 3.6V	**50**	70	**90**	mV
I_{SHDN}	Shutdown Supply Current	EN = 0V		0.5	**5**	µA
$I_{Q,PWM}$	DC Bias Current into V_{DD} (V_{OUT} set to 1.35V)	PWM mode, no switching (SYNC/MODE = V_{DD}, V_{FB}=2V)		425		µA
$I_{Q,LIN}$	DC Bias Current into V_{DD}	No-Load, Linear mode (SYNC/MODE = 0V)		29	**40**	µA
$R_{DSON(P)}$	Pin-pin Resistance for PFET			250		mΩ
$R_{DSON(N)}$	Pin-pin Resistance for NFET			180		mΩ
$I_{lim\_-1.25}$	Switch Peak Current Limit	PWM mode I_{SEL}=V_{IN}, V_{IN} = 2.7V to 4.5V	**TBD**	454	**TBD**	mA
		PWM mode I_{SEL} = 0, V_{IN} = 2.7V to 4.5V	**TBD**	TBD	**TBD**	mA
$I_{lim\_-1.35/-1.4}$	Switch Peak Current Limit	PWM mode I_{SEL}=V_{IN}, V_{IN} = 2.7V to 4.5V	**473**	518	**550**	mA
		PWM mode I_{SEL} = 0, V_{IN} = 2.7V to 4.5V	**565**	615	**650**	mA
I_{lim_LIN}	Max Current in Linear Mode	SYNC/MODE = 0V, FB = 0V V_{IN} = 2.7V to 5.5V	**35**	60	**90**	mA

Electrical Characteristics (Note 2) (Continued)

Specifications with standard typeface are for T_J = 25˚C, and those in **bold face type** apply over the full Operating Temperature Range (T_A = T_J = −30˚C to +85˚C). Unless otherwise specified, PV_{IN} = V_{DD} = EN = SYNC/MODE = V_{SEL} = 3.6V, I_{SEL}= 0V, C_{OUT} = 22 µF.

Symbol	Parameter	Remarks	Min	Typ	Max	Units
$V_{EN,H}$	EN Logic High Input (Note 4)	V_{IN} = 2.7V to 5.5V			**1.2**	V
$V_{EN,L}$	EN Logic Low Input		**0.4**			V
$V_{SYNC/MODE, H}$	SYNC/MODE Logic High Input				**1.2**	V
$V_{SYNC/MODE, L}$	SYNC/MODE Logic Low Input		**0.4**			V
$V_{SEL, H}$	V_{SEL} Logic High Input				**1.2**	V
$V_{SEL, L}$	V_{SEL} Logic Low Input		**0.4**			V
$I_{SEL,H}$	I_{SEL} Logic High Input				**1.2**	V
$I_{SEL, L}$	I_{SEL} Logic Low Input		**0.4**			
R_{EN}	Enable pin input resistance			1		MΩ
f_{SYNC}	SYNC/MODE Clock Frequency Range (Note 6)	V_{IN} = 2.7V to 5.5V	**500**		**750**	kHz
f_{OSC}	Internal Oscillator Frequency	PWM mode (SYNC/MODE = V_{IN}) V_{IN} = 2.7V to 5.5V	**535**	600	**675**	kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Due to the pulsed nature of the testing T_A=T_J for the electrical characteristics table.

Note 3: Thermal shutdown will occur if the junction temperature exceeds 150˚C. This function is only active in PWM mode.

Note 4: The LM3202 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.

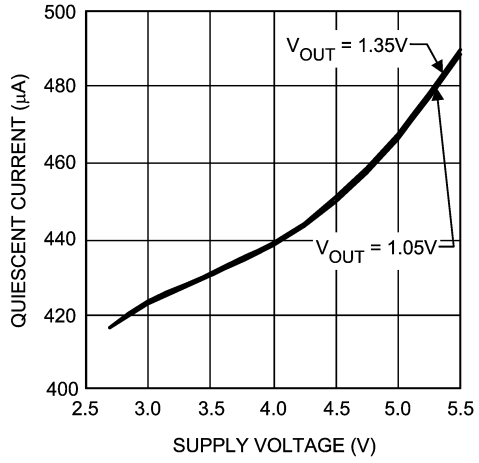
Note 5: The hysteresis voltage is the minimum voltage swing on FB that causes the internal feedback and control circuitry to turn the internal PFET switch on and then off, during test mode.

Note 6: SYNC/MODE driven with an external clock switching between V_{IN} and GND. When an external clock is present at SYNC/MODE, the IC is forced to PWM mode at the external clock frequency.

Typical Performance Characteristics

(Circuit in Fig.2, PV_{IN} = V_{DD} = EN=3.6V, T_A = 25˚C, unless otherwise noted)

Quiescent Supply Current vs. Supply Voltage (PWM MODE)



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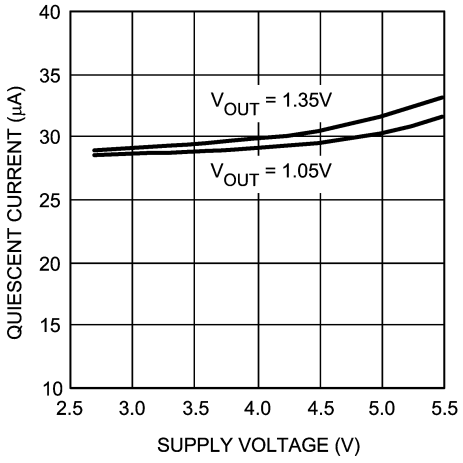
Quiescent Supply Current vs. Supply Voltage (LDO MODE)



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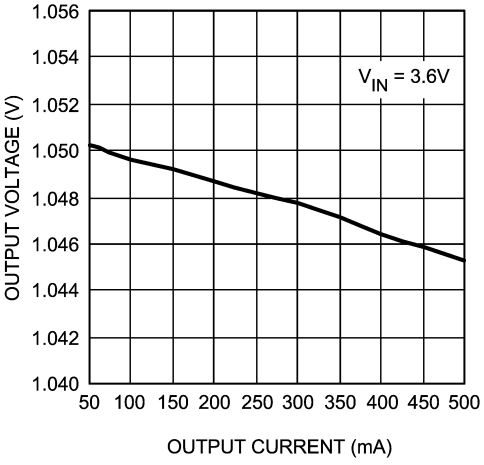
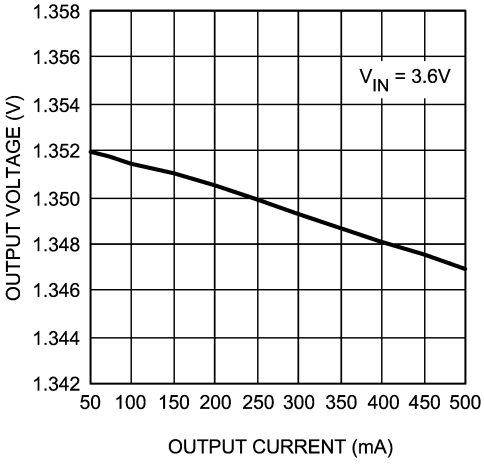
Output Voltage vs. Output Current (PWM MODE, I_{SEL}=L, V_{OUT} = 1.05V)



20098814

Output Voltage vs. Output Current (PWM MODE, I_{SEL}=L, V_{OUT} = 1.35V)



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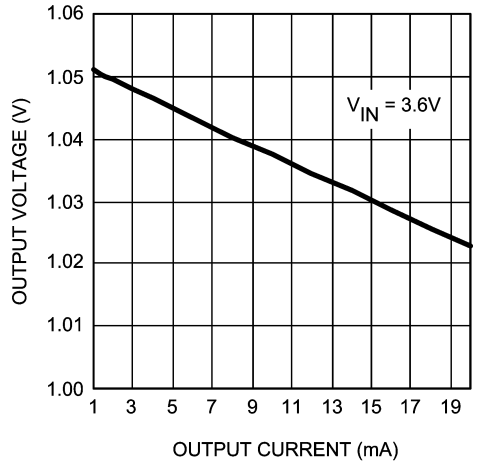
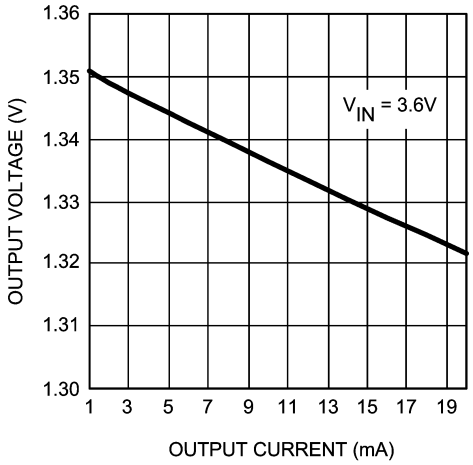
Output Voltage vs. Output Current (LDO MODE, V_{OUT}=1.05V)



20098816

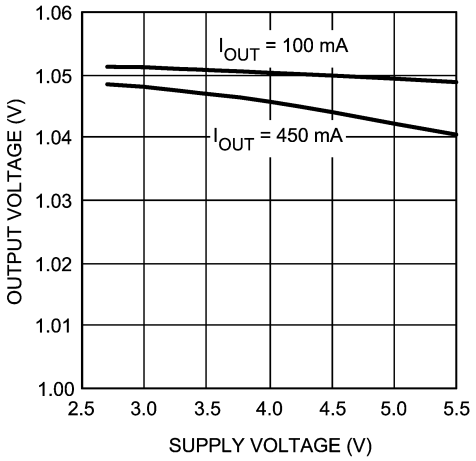
Output Voltage vs. Output Current (LDO MODE, V_{OUT}=1.35V)



20098817

Typical Performance Characteristics (Circuit in Fig.2, PV_{IN} = V_{DD} = EN=3.6V, T_A = 25˚C, unless otherwise noted) (Continued)

Output Voltage vs. Supply Voltage (PWM MODE, I_{SEL} = L, V_{OUT} = 1.05V)



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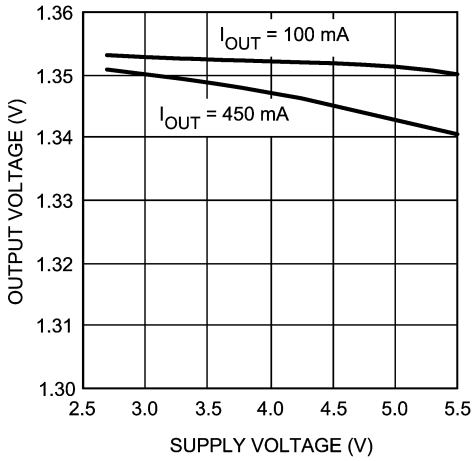
Output Voltage vs. Supply Voltage (PWM MODE, I_{SEL} = L, V_{OUT} = 1.35V)



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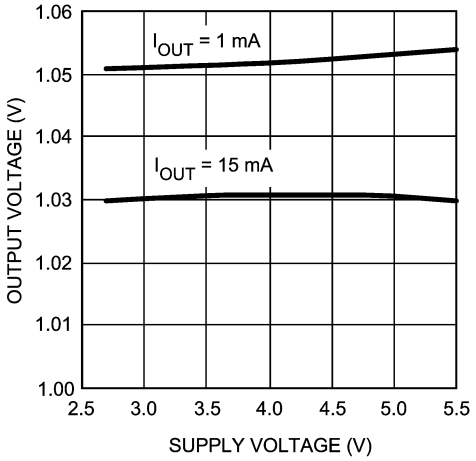
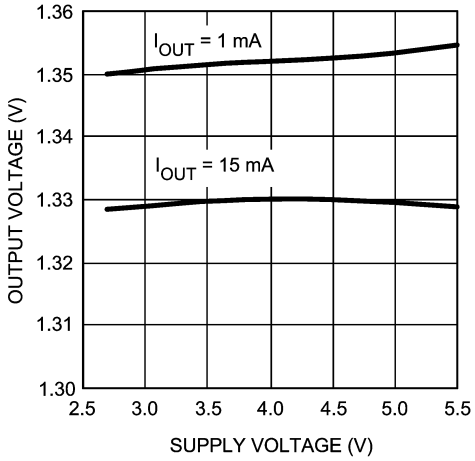
Output Voltage vs. Supply Voltage (LDO MODE, V_{OUT} = 1.05V)



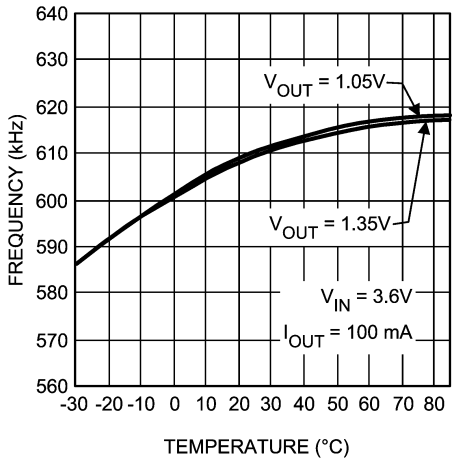
20098848

Output Voltage vs. Supply Voltage (LDO MODE, V_{OUT} = 1.35V)



20098849

Switching Frequency vs. Temperature (PWM MODE, SYNC/MODE = V_{IN})



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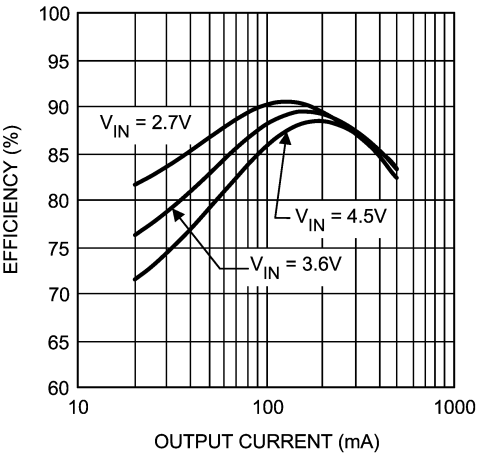
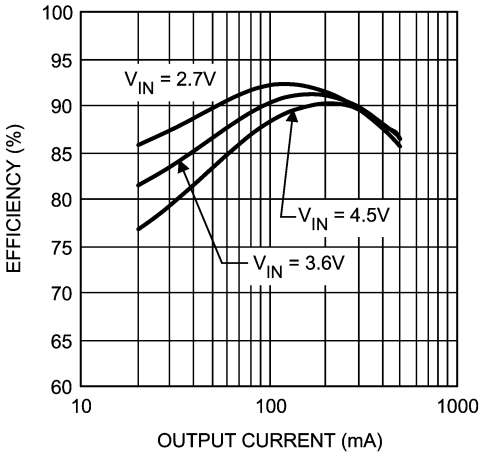
Efficiency vs. Output Current (SYNC/MODE = V_{IN}, V_{OUT} = 1.05V)



20098822

Typical Performance Characteristics (Circuit in Fig.2, PV_{IN} = V_{DD} = EN=3.6V, T_A = 25˚C, unless otherwise noted) (Continued)

Efficiency vs. Output Current
(PWM MODE, I_{SEL} = L, V_{OUT} = 1.35V)



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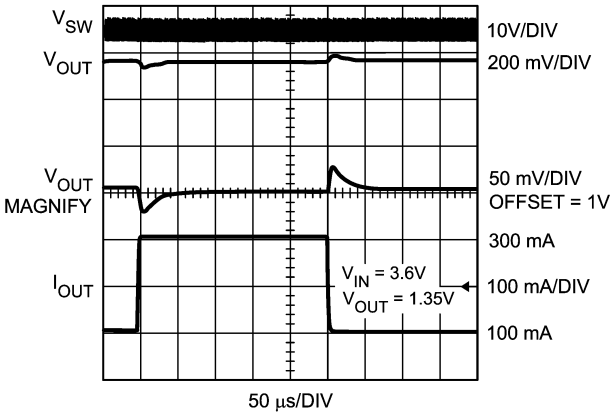
PWM Load Transient Response
(I_{SEL}=L, V_{IN} = 3.6V, V_{OUT} = 1.35V)



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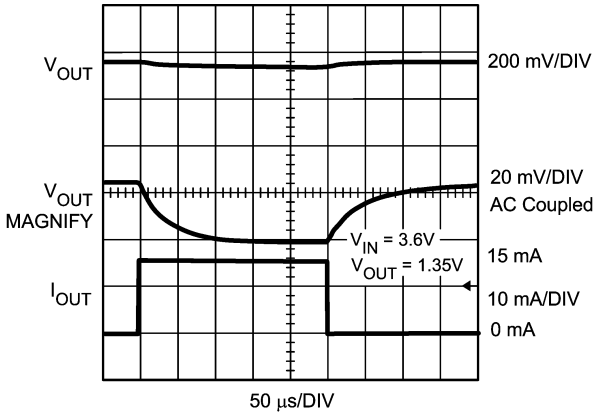
LDO Load Transient Response
(V_{IN} = 3.6V & V_{OUT} = 1.35V)



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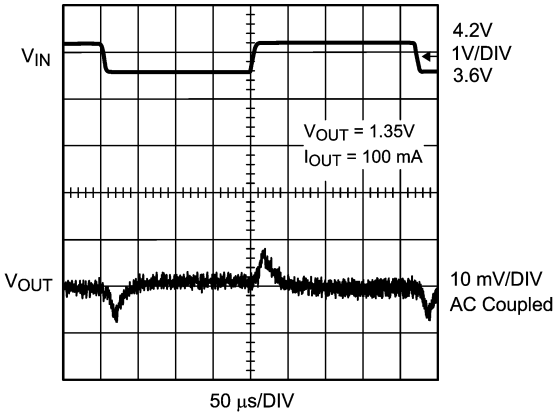
PWM Line Transient Response



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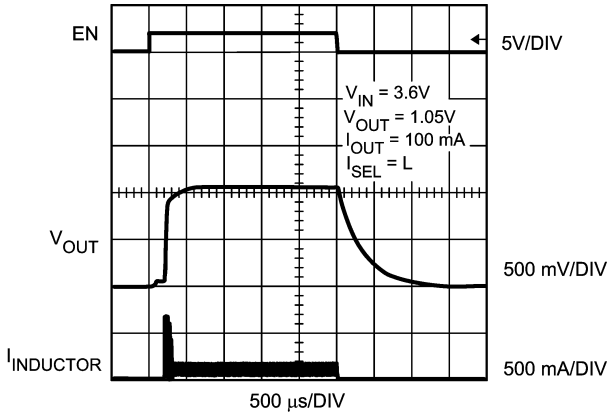
PWM Start-up Respsonse
(V_{IN} = 3.6V & V_{OUT} = 1.05V)



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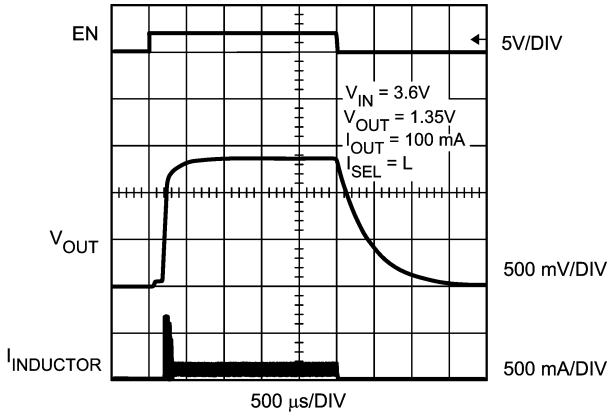
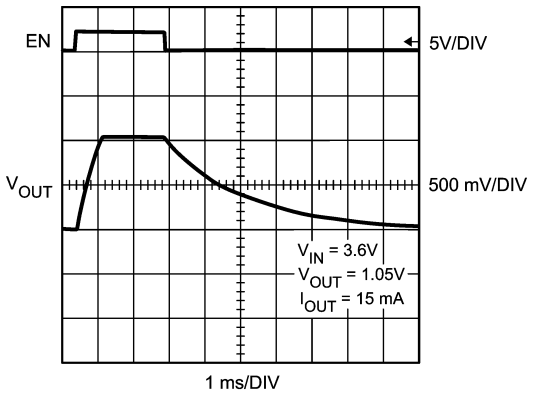
PWM Start-up Respsonse
(V_{IN} = 3.6V & V_{OUT} = 1.35V)



20098826

Typical Performance Characteristics (Circuit in Fig.2, PV_{IN} = V_{DD} = EN=3.6V, T_A = 25˚C, unless otherwise noted) (Continued)

LDO Start-up Respsonse (V_{IN} = 3.6V & V_{OUT} = 1.05V)



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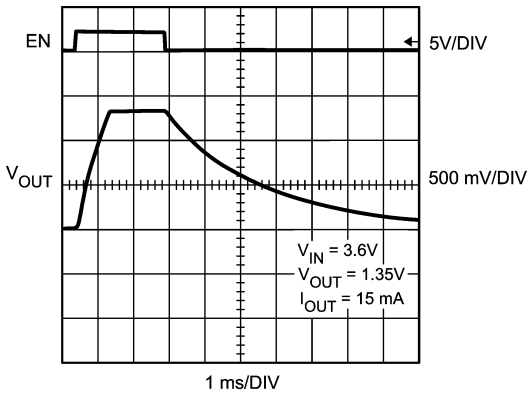
LDO Start-up Respsonse (V_{IN} = 3.6V & V_{OUT} = 1.35V)



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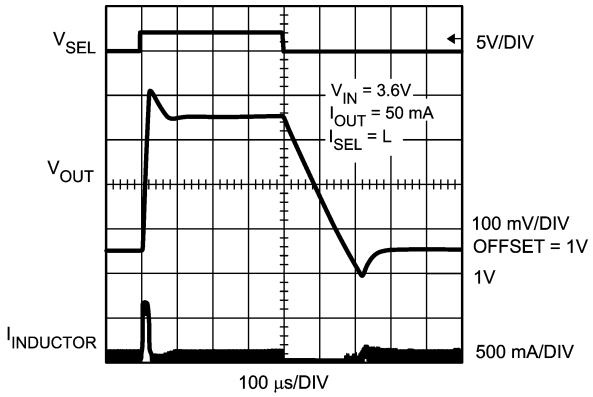
V_{SEL} Transition in PWM Mode (LM3661-1.35)



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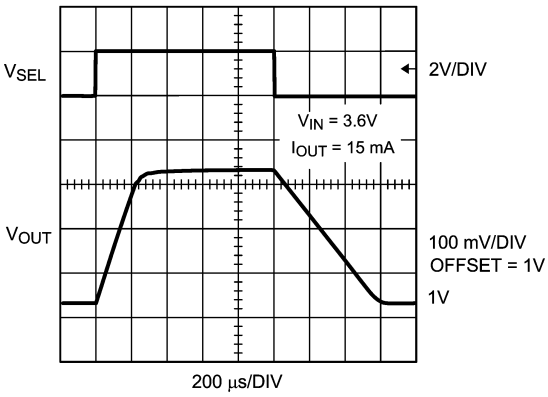
V_{SEL} Transition in LDO Mode (LM3661-1.35)



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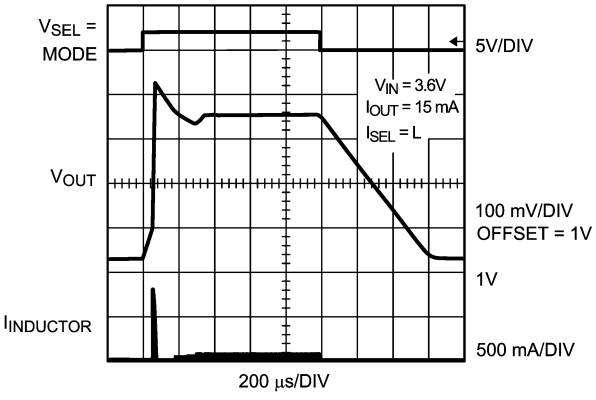
V_{SEL} & SYNC/MODE Transition in PWM Mode



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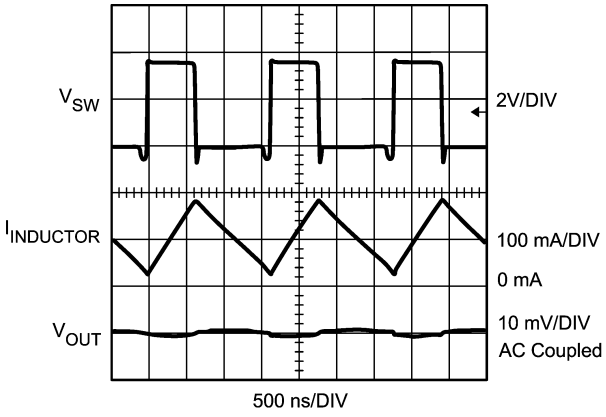
TYP Waveform (PWM Mode, I_{OUT} = 100mA)



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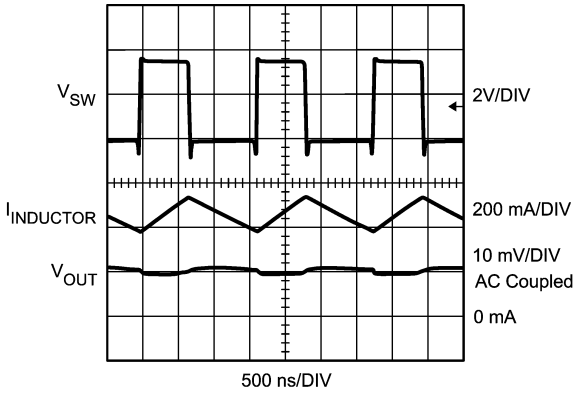
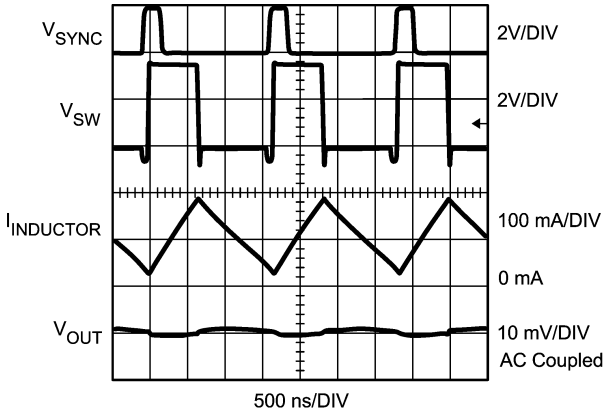
Typical Performance Characteristics (Circuit in Fig.2, PV_{IN} = V_{DD} = EN=3.6V, T_A = 25˚C, unless otherwise noted) (Continued)

TYP Waveform
(PWM Mode, I_{OUT} = 450mA)



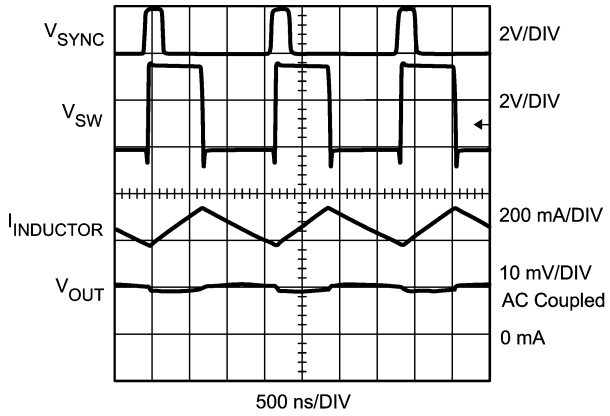
20098830

External SYNC/MODE at 600kHz
(I_{OUT} = 100mA)



20098831

External SYNC/MODE at 600kHz
(I_{OUT} = 450mA)



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Circuit Operation

The LM3661 operates as follows: During the first part of each switching cycle, the control block in the LM3661 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with the slope of $(V_{IN} - V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. In response, the inductor' magnetic field collapse, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope of V_{OUT}/L. If the inductor current reaches zero before the next cycle, the synchronous rectifier is turned off to prevent current reversal. The output filter capacitor stores charge when the inductor current is high, and release it when low, smoothing the voltage across the load.

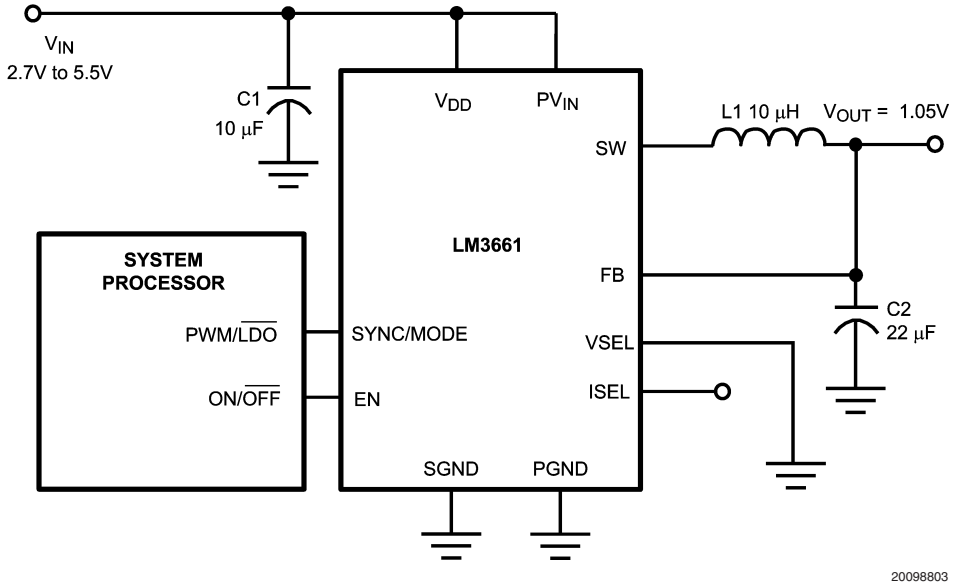


FIGURE 2. Typical Operating Circuit

PWM Operation

The LM3661 can be set to current-mode PWM operation by connecting the SYNC/MODE pin to V_{DD}. While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse-width to control the peak inductor current. This is done by controlling the PFET switch using a flip-flop driven by an oscillator and a comparator that compares a ramp from the current-sense amplifier with an error signal from a voltage-feedback error amplifier. At the beginning of each cycle, the oscillator sets the flip-flop and turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator resets the flip-flop and turns off the PFET switch, ending the first part of the cycle. The NFET synchronous rectifier turns on until the next clock pulse or the inductor current ramps to zero. If an increase in load pulls the output voltage down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET switch. This increases the average current sent to the output and adjusts for the increase in the load. Before going to the PWM comparator, the current sense signal is summed with a slope compensation ramp from the oscillator for stability of the current feedback loop. During the second part of the cycle, a zero crossing detector turns off the NFET synchronous rectifier if the inductor current ramps to zero.

LDO Operation

Connecting the SYNC/MODE pin to GND sets the LM3661 in Linear Mode operation. While in Linear mode (LDO) the device consumes only 29 µA (typ.) quiescent current for system standby operation. It is capable of delivering up to 15 mA. This is done by using an internal pass transistor and an error amplifier to sense the output voltage and maintain the desire output voltage. During LDO mode, the PFET and NFET of the network switch off to reduce quiescent current.

Frequency Synchronization

The SYNC/MODE input can also be used for frequency synchronization. To synchronize the LM3661 to an external clock, supply a digital signal to the SYNC/MODE pin with a voltage swing exceeding 0.4V to 1.2V. During synchronization, the LM3661 initiates cycles on the rising edge of the clock. When synchronized to an external clock, it operates in PWM mode. The device can synchronize to an external clock over frequencies from 500 kHz to 750 kHz. Use the following waveform and duty-cycle guidelines when applying an external clock to the SYNC/MODE pin. The duty cycle can be between 30% and 70%. Clock under/overshoot should be less than 100 mV below GND or above V_{DD}. When applying noisy clock signals, especially sharp edged signals from a long cable during evaluation, terminate the cable at its characteristic impedance; add an RC filter to the SYNC/MODE pin, if necessary, to soften the slew rate and

Frequency Synchronization

(Continued)

over/undershoot. Note that sharp edged signals from a pulse or function generator can develop under/overshoot as high as 10V at the end of an improperly terminated cable.

Over-voltage Protection

The LM3661 has an over-voltage comparator that prevents the output voltage from rising too high when the device is left in PWM mode under low-load conditions. Otherwise, the output voltage could rise out of regulation from the minimum energy transferred per cycle due to about 250 ns minimum on-time of the PFET switch while in PWM mode. When the output voltage rises by 70 mV over its regulation threshold, the OVP comparator inhibits PWM operation to skip pulses until the output voltage returns to the regulation threshold. In over voltage protection, output voltage and ripple increase slightly.

Shutdown Mode

Setting the EN input low, to SGND, places the LM3661 in a 0.5 µA (typ) shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference, control and bias of the LM3661 are turned off. Setting EN high to V_{DD} enables normal operation. While turning on, soft start is activated. EN is a Schmidt trigger digital input with thresholds that are independent of the input voltage at V_{DD}. EN must be set low to turn off the LM3661 during under voltage conditions when the supply is less than the 2.7V minimum operating voltage. The LM3661 is designed for mobile phones and similar applications where power sequencing is determined by the system controller and internal UVLO (Under Voltage Lock Out) circuitry is unnecessary. The LM3661 has no UVLO circuitry. Although the LM3661 exhibits good behavior while enabled at low input voltages, this is not guaranteed.

Start-up

The LM3661 is designed to be started in LDO mode. Under these conditions, the output voltage will increase at a rate determined by the LDO current limit and the output capacitor and load. This ramp time is typically about 600 µs. The LM3661 may be started in PWM mode as well. Under these conditions, the reference voltage for the error amplifier is ramped up time is about 300µs and the output voltage will follow. In this way, the input inrush current and output voltage over shoot can be minimized.

Thermal Shutdown Protection

The LM3661 has thermal shutdown protection in PWM mode to protect from short-term misuse and overload conditions. When the junction temperature exceeds 150˚C, the device shuts down and re-starts in soft start after the temperature drops below 130˚C. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

Current Limiting Protection

A current limit feature allows the LM3661 to protect itself and external components during overload conditions. Current limiting is implemented using an independent internal comparator. In PWM mode, cycle-by-cycle current limiting is normally used. If an excessive load pulls the output voltage down to approximately 0.45V, then the device switches to a timed current limit mode. In timed current limit mode the internal PFET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 2.5 µs to force the instantaneous inductor current to ramp down to a safe value. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

Application Information

PIN SELECTABLE OUTPUT

The LM3661 features pin-selectable output voltage to eliminate the need for external feedback resistors. Select an output voltage of 1.05V or 1.25V/1.35V/1.4V by setting the V_{SEL} pin low or high. V_{SEL} may be set high by connecting to V_{DD} or low by connecting to GND. Alternatively, V_{SEL} may be driven off digitally by a logic gates that provide over 1.2V for high state and less than 0.4V for a low state to ensure valid logic levels. V_{SEL} input has no internal pull down that pulls the input low, this pin must be set to a known state.

Isel Pin

Connecting the I_{SEL} pin high (>1.2V or Vin) sets the internal current limit comparator to low value and low (< 0.4 or GND) to high value. Note that I_{SEL} pin has no internal pull down and this pin must connect to a known state of normal operation.

Table 1 shows selected I_{OUT} capability information.

Table 1. I_{SEL} condition and I_{OUT} capability (Applies to both V_{SEL} = H and V_{SEL} = L)

V_{OUT} option	I_{SEL}	I_{OUT} capability
1.05V/1.25V	H	300mA
1.05V/1.25V	L	TBDmA
1.05V/1.35V	H	350mA
1.05V/1.35V	L	450mA
1.05V/1.40V	H	350mA
1.05V/1.40V	L	450mA

Mode Transition

The LM3661 is designed to operate in two modes, LDO(Low Dropout Regulator) mode for light load (15mA Max.) and PWM Mode (Pulse Width Modulation) . As described in the Device Operation Section, setting the SYNC/MODE pin low yields LDO mode or high yields PWM mode. When mode transitions from LDO to PWM and vice versa, harsh transient conditions such as ramping the output load should be avoided. To maintain a smooth transition, it is recommended to keep the load to a minimum of 3mA or less for about 40us before ramping into heavy load to avoid a large dip at the output. Similarly, the same care must be applied when changing output voltage from 1.05V to 1.25V/1.35V/1.40V and vice versa (setting Vsel pin high or low) during full load. Figure 3 below shows the mode transition from LDO to PWM and PWM to LDO, and the load transient transition from light load to heavy load is delayed by 40µs to allow the PWM loop to respond properly.

Application Information (Continued)

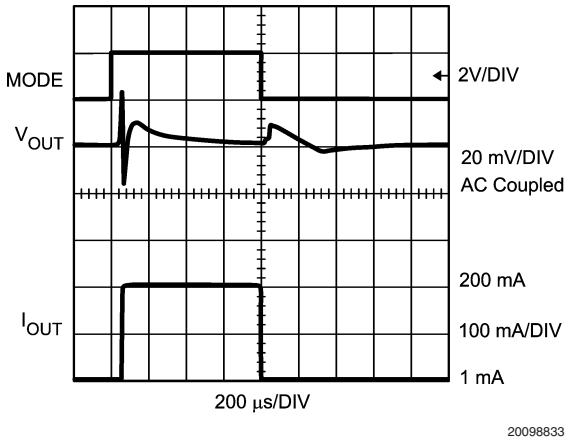


FIGURE 3.

INDUCTOR SELECTION

There are a few things that one must consider when selecting an inductor for an application. They are the inductor DC current rating, inductor ripple current, DC-resistance of the inductor and value of the inductor. The DC current rating of the inductor denotes the maximum current before the inductor core enters saturation. Before selecting the DC current rating of the inductor, an inductor ripple current must be determined using *Equation (1)*. The DC current of the inductor should be the maximum output current of the circuit plus half of the peak to peak current ripple of the inductor using *Equation (2)*.

$$I_{PEAK} = I_O + \frac{1}{2}(\Delta I_L) \quad (1)$$

$$\Delta I_L = \frac{V_I - V_0}{L} \bullet DT = \frac{V_I - V_0}{L} \bullet \frac{V_0}{V_I} \bullet \frac{1}{f} \quad (2)$$

A good estimate for the inductor ripple current would be using a operation condition or assume the inductor ripple current to be about 30% of the maximum output current of the device. Consider the following example for LM3661 (when I_{SEL} = L); a 10 µH, 450 mA load current with 1.4V output operates at 4.5V input and 600kHz in an application, solving for ΔI_L using *Equation (2)* yields ΔI_L = 160 mA. Therefore the maximum peak current (*Equation (1)*) in the application will be 530 mA (I_O + 1/2ΔI_L). Thus, an inductor with DC current rating of 600 mA or higher should suffice for the application when I_{SEL} = L. For a more conservative approach, it is best to select an inductor with a current rating of the maximum switch peak current of the device. Note that If smaller inductor is used in the application, the larger the inductor ripple current (*Equation (1)*). Care must be taken to select the inductor such that the peak current rating of the inductor accounts for minimum inductance and maximum current for the operating condition. *Equation (3)* can be used to calculate the inductor value if the application conditions are known:

$$L = V_0 \left(1 - \frac{V_0}{V_I}\right) \bullet \frac{1}{\Delta I_L f} \quad (3)$$

Where f is the operating frequency, ΔI_L is the inductor current ripple and Vo is the desired output.

Finally, the DC resistance (DCR) of the inductor also affect the overall efficiency of the solution. Lower DCR is recommended for better efficiency in handheld and battery operated applications. Consult inductor manufacture for this specification. Table 2 lists suggested inductors and suppliers.

Table2. Suggested Inductor and Suppliers

Part Number	Vendor	Web
D01608C-103	Coilcraft	www.coilcraft.com
P1174.103T	Pulse	www.pulseeng.com
P0770.103T		
Ell6GM100M	Panasonic	www.panasonic.com

INPUT AND OUTPUT CAPACITOR

The LM3661 is designed for ceramic capacitor for its input and output filters. Ceramic capacitors such as X5R and X7R are recommended to use for input and output filters. These provide an optimal balance between small size, cost, reliability and performance. Do not use Y5V ceramic capacitors as they have poor dielectrics performance over temperature and voltage characteristics for a given value. *Table 2* lists suggested capacitors and suppliers.

A 10 µF input and 22 µF output ceramic capacitors are suggested in figure 2 (Typical application circuit) for optimal performance.

The input filter capacitor supplies current to the PFET switch of the LM3661 in the first part of each cycle and reduces voltage ripple imposed on the input power source. The output filter capacitor smooths out current flow from the inductor and reduce output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR

Application Information (Continued)

to perform these functions. The ESR, or equivalent series resistance, of the filter capacitors is a major factor in voltage ripple. Table 3 lists suggested capacitors suppliers.

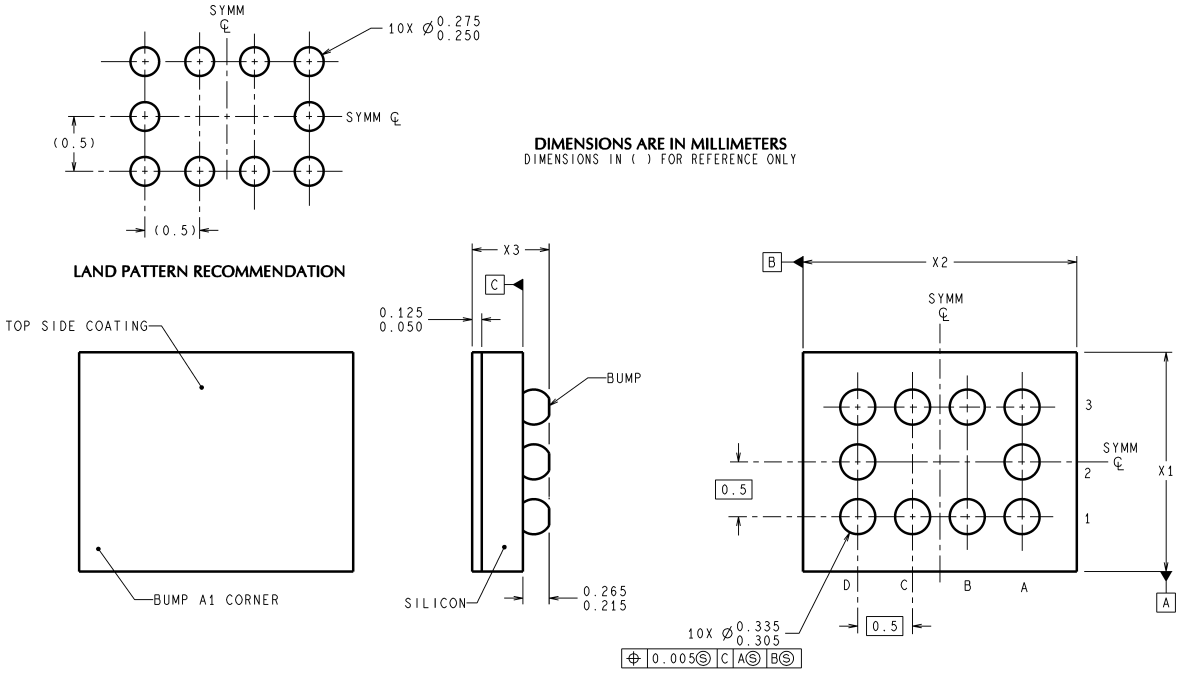
Table 3. Suggested capacitors and Suppliers

Model	Size (EIA)	Vendor
Input Filter Capacitor (10µF, 6.3V, X5R or X7R9		
C2012X5R0J106M	2012 (0805)	TDK
JMK212BJ106MG	2012 (0805)	Taiyo-Yuden
GRM21BR60J106K	2012 (0805)	muRata
Output Filter Capacitor (22µF, 6.3V, X5R or X7R9		
C3225X5R0J226M	3225(1210)	TDK
JMK325BJ226MG	3225(1210)	Taiyo-Yuden
GRM32DR60J226K	3225(1210)	muRata

BOARD LAYOUT CONSIDERATION

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing EMI, ground bounce, and resistive voltage loss in the traces. Below are layout recommendation to maximize device performance: 1) Place the inductor and filter capacitors close together and minimize the traces between components as they carry relatively high switching current and act as antennas. 2) Use wide traces between the power components and for power connections to DC-DC converters circuit. 3) Route noise sensitive traces such as the voltage feedback path away from noisy power components. 4) Connect the ground pins and filter capacitors together via a ground plane to prevent switching current circulating through the ground plane. Additional information regarding Micro SMD package layout can be found in Application note AN-1112.

Physical Dimensions inches (millimeters) unless otherwise noted



TLP10XXX (Rev D)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.

10-Bump micro SMD Package
NS Package Number TLP10QTA
The dimensions for X1, X2 and X3 are as given:
X1 = 1.869 ± 0.030 mm
X2 = 2.428 ± 0.030 mm
X3 = 0.600 ± 0.075 mm

Notes

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Support Center
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Tel: 1-800-272-9959

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