National Semiconductor

PRELIMINARY
August 1985

Quad SPST High Voltage CMOS Analog Switches
LMC13334 4 Normally Open Switches with Disable
LMC13204 4 Normally Open Switches
LMC13335 4 Normally Open Switches with Latches

General Description

These switches utilize National's high voltage epitaxial CMOS process allowing operation to 40V. The analog voltage is allowed to swing over the entire supply range.

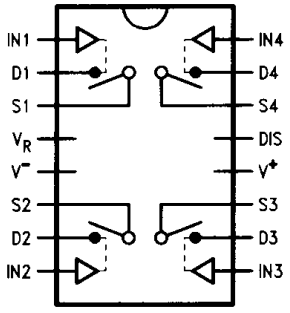
The LMC13334 is pin compatible with the LF13331. The LMC13204 is pin compatible with the LF13202. The LMC13335 is a new latched version.

Features

- R_{ON} = 50Ω (typical)
- TTL compatible inputs
- 5V to 40V operation
- Break-before-make operation

Connection Diagrams (Dual-In-Line Packages) (All switches shown are for Logic "0")

LMC13334



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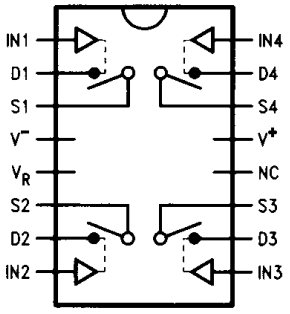
LMC13204



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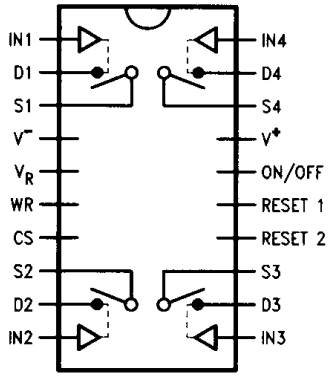
LMC13335



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Test Circuit

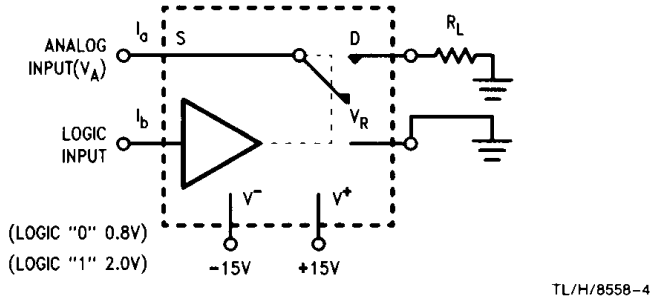

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FIGURE 1. Typical Circuit for One Switch

RRD-B30M75/Printed in U. S. A.

Quad SPST High Voltage CMOS Analog Switches LMC13334/ LMC13204/ LMC13335

Absolute Maximum Ratings (Note 1)

(All voltages referred to V_R)

Positive Supply (V^+)	+22V
Negative Supply (V^-)	−22V
Logic Input Voltage (Note 4)	−0.2V to V^+ + 0.2V
Analog Voltage (Note 4)	V^- − 0.2V to V^+ + 0.2V
Analog Current	20 mA
Power Dissipation	500 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Note 1)

Positive Supply (V^+)	+5V to +20V
Negative Supply (V^-)	0V to −20V
Analog Voltage	V^- to V^+
Temperature Range	−55°C to +125°C

Electrical Characteristics

The following characteristics apply for $V^+ = +15V$, $V^- = -15V$, and $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	Typical (Note 2)	Test Limit (Note 3)	Units
R_{ON}	"ON" Resistance	$V_A = 0, \pm 10V$	50	75	Ω (max)
		$V_A = 0, V^+ = 5V, V^- = 0V$	140		Ω (max)
R_{ON} Match	"ON" Resistance Matching Between Switches	$V_A = 0, \pm 10V$	2	5	Ω (max)
V_A	Analog Voltage Range		±15	±15	V (min)
$I_S(ON) + I_D(ON)$	Leakage Current in ON Condition	$V_S, V_D = \pm 14V$	2	5	nA (max)
$I_S(OFF)$	Source Current in "OFF" Condition	$V_S = \pm 14V$ $V_D = \pm 14V$	2	5	nA (max)
$I_D(OFF)$	Drain Current in "OFF" Condition	$V_D = \pm 14V$ $V_S = \pm 14V$	2	5	nA (max)
V_{IH}	Logical "1" Input Voltage	$V_R = 0$	1.4	2.0	V (min)
V_{IL}	Logical "0" Input Voltage		1.4	0.8	V (max)
I_{IH}	Logical "1" Input Current		0.001	100	nA (max)
I_{IL}	Logical "0" Input Current		30	60	μA (max)
C_S (OFF)	Source Capacitance	$V_A = 0$ Switch Off	10		pF
C_D (OFF)	Drain Capacitance	$V_A = 0$ Switch Off	10		pF
C_S (ON) + C_D (ON)	Active S + D Capacitance	$V_A = 0$ Switch On	55		pF
Iso(OFF)	"OFF" Isolation	$R_L = 1k$ f = 100 kHz	−70		dB
CT	Crosstalk	$R_L = 1k$ f = 100 kHz	−90		dB
I_{V^-}	Negative Supply Current	All Switches Off	0	0.05	mA (max)
I_R	Reference Supply Current	All Switches Off	0.6	1.5	mA (max)
I_{V^+}	Positive Supply Current	All Switches Off	0.7	1.5	mA (max)

Timing Characteristics LMC13335

The following characteristics apply for $V^+ = +15V$, $V^- = -15V$, and $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	Typical (Note 2)	Test Limit (Note 3)	Units
t_{ON}	Delay Time "ON"	$V_S = \pm 10V$	550	850	ns (max)
t_{OFF}	Delay Time "OFF"	$V_S = \pm 10V$	300	650	ns (max)
t_W	Write Pulse Width		260	380	ns (min)
t_{DS}	Data Set Up Time	$t_W = 380$ ns	120	250	ns (min)
t_{DH}	Data Hold Time	$t_W = 380$ ns	120	250	ns (min)
t_{CS}	Control Set Up Time	$t_W = 380$ ns	260	380	ns (min)
t_{CH}	Control Hold Time	$t_W = 380$ ns	0	0	ns (min)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating device beyond its specified operating conditions.

Note 2: Typicals represent the most likely parametric norm.

Note 3: Guaranteed and 100% production tested.

Note 4: When inputs are driven beyond these voltage limits, internal clamp diodes turn on. If the input current is limited to less than 20 mA, the overdrive will not be harmful to the device. The same precautions apply when signals are present while power supplies are off.

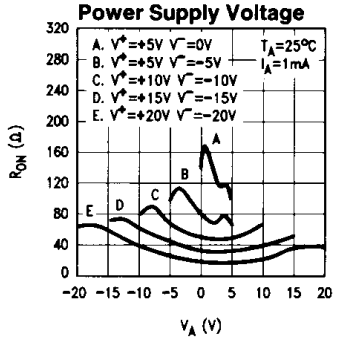
Timing Characteristics LMC 13334/204

The following characteristics apply for $V^+ = +15V$, $V^- = -15V$, and $T_A = 25°C$ unless otherwise specified

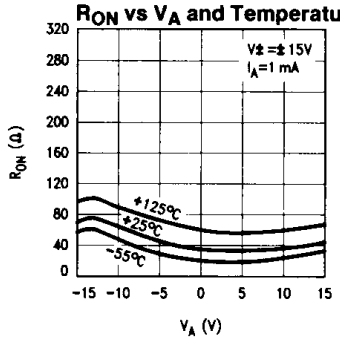
Symbol	Parameter	Conditions	Typical (Note 2)	Test Limit (Note 3)	Units
t_{ON}	Delay Time "ON"	$V_S = \pm 10V$	300	550	ns (max)
t_{OFF}	Delay Time "OFF"	$V_S = \pm 10V$	250	500	ns (max)

Typical Performance Characteristics

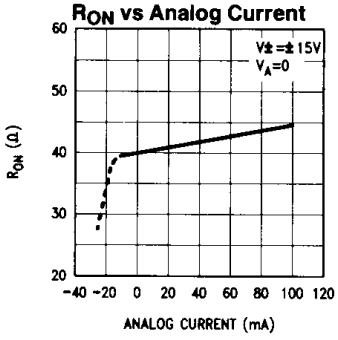
R_{ON} vs V_A and Power Supply Voltage



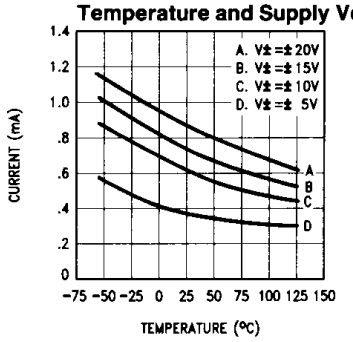
R_{ON} vs V_A and Temperature



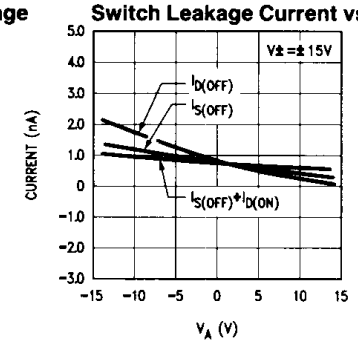
R_{ON} vs Analog Current



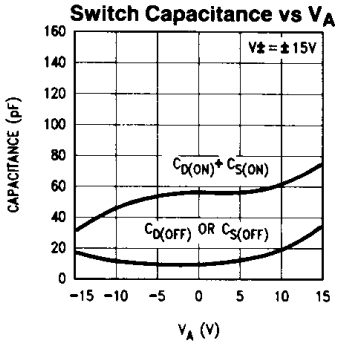
Positive Supply Current vs Temperature and Supply Voltage



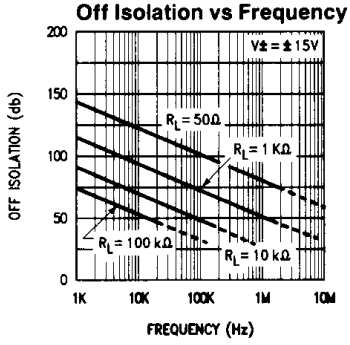
Switch Leakage Current vs V_A



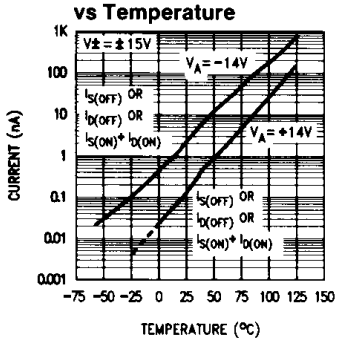
Switch Capacitance vs V_A



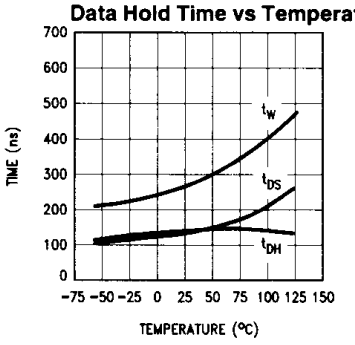
Off Isolation vs Frequency



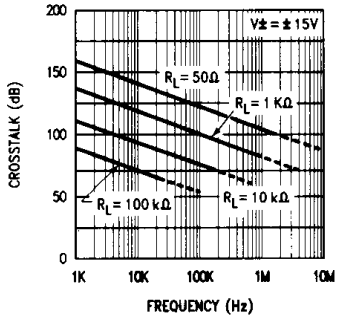
Switch Leakage Current vs Temperature



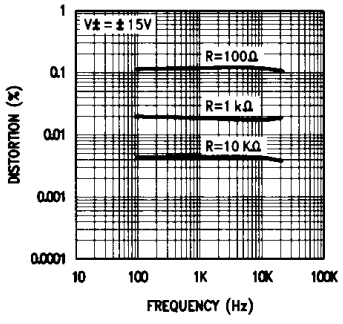
Pulse Width, Data Setup Time & Data Hold Time vs Temperature



Channel to Channel Crosstalk vs Frequency



Total Harmonic Distortion vs Frequency



TL/H/8558–9

Application Hints

GENERAL INFORMATION

These devices are monolithic quad CMOS analog switches with 50Ω typical "ON" resistance and operation on single-ended supply voltages ranging from 5 volts to 20 volts or split supplies up to ±20 volts. The allowable analog signal swing includes the supply voltages, resulting in 6 dB greater signal handling capability than comparable JFET analog switches. Each switch is controlled by TTL or CMOS level signals at its logic input and is designed to turn "OFF" faster than it turns "ON". This helps avoid momentarily connecting two analog signal sources together when switching from one source to the other.

LOGIC INPUTS

The threshold voltage for the logic inputs (IN1 through IN4, $\overline{wr}$, $\overline{cs}$, $\overline{DIS}$, $\overline{Reset1}$, $\overline{Reset2}$, and ON/$\overline{OFF}$) is set using the reference pin (V_R). The threshold will be equal to two diode forward voltages above V_R, or about 1.4V at room temperature, so that if the V_R pin is connected to ground, the logic inputs will be compatible with either TTL or CMOS logic signals. Voltages between V_R and the positive supply may be applied to the logic input with no errors in switch states. Any logic pins left unconnected will float "high". The logic inputs are diode-clamped to V_R, so logic signals should be current-limited to less than 20 mA if they are expected to drop below this voltage. V_R may be set to any voltage between $V^+ - 5V$ and $V^+ - 20V$.

The LMC13335's logic input states may be latched using the $\overline{wr}$ and $\overline{cs}$ pins. If the $\overline{wr}$ and $\overline{cs}$ pins are both low, the data on the logic inputs will be active. Pulling $\overline{cs}$ and/or $\overline{wr}$ high will latch the data on the logic inputs. The ON/$\overline{OFF}$ pin can be used in conjunction with the two Reset pins to either open or close all of the switches regardless of the states of the other control inputs. Pulling either $\overline{Reset1}$, $\overline{Reset2}$, or both pins low will set all the switches in the state dictated by the ON/$\overline{OFF}$ pin (high for ON, low for OFF).

The disable ($\overline{DIS}$) pin on the LMC13334 may be used to turn all of the switches off independent of the logic inputs. To accomplish this, apply a logic "low" voltage to the disable pin. If the disable function is not needed, the disable pin may be left floating.

"ON" RESISTANCE VARIATIONS

As the typical performance curves show, "ON" resistance of the switches is lowest and most nearly constant when the supply voltages are highest. Therefore, when maximum linearity is desired, the supply voltages should be as close to the maximum operating ratings as possible. Variations in R_{on} can also be minimized by keeping the analog voltage swing small.

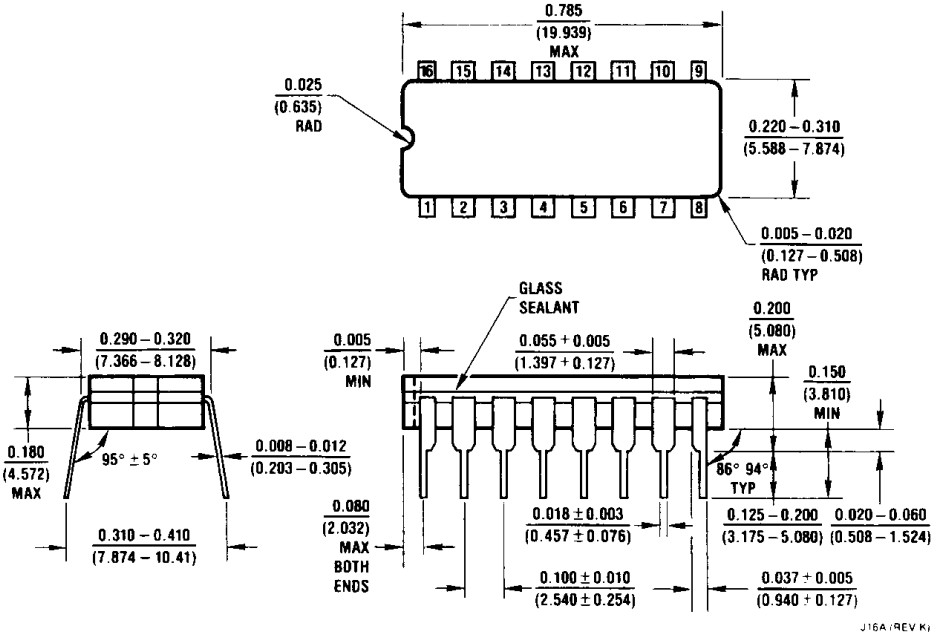
ANALOG VOLTAGE AND CURRENT LIMITATIONS

Analog signal voltages can swing to either supply. If larger signals are expected, they should be current limited to less than 20 mA.

SWITCHING TRANSIENTS

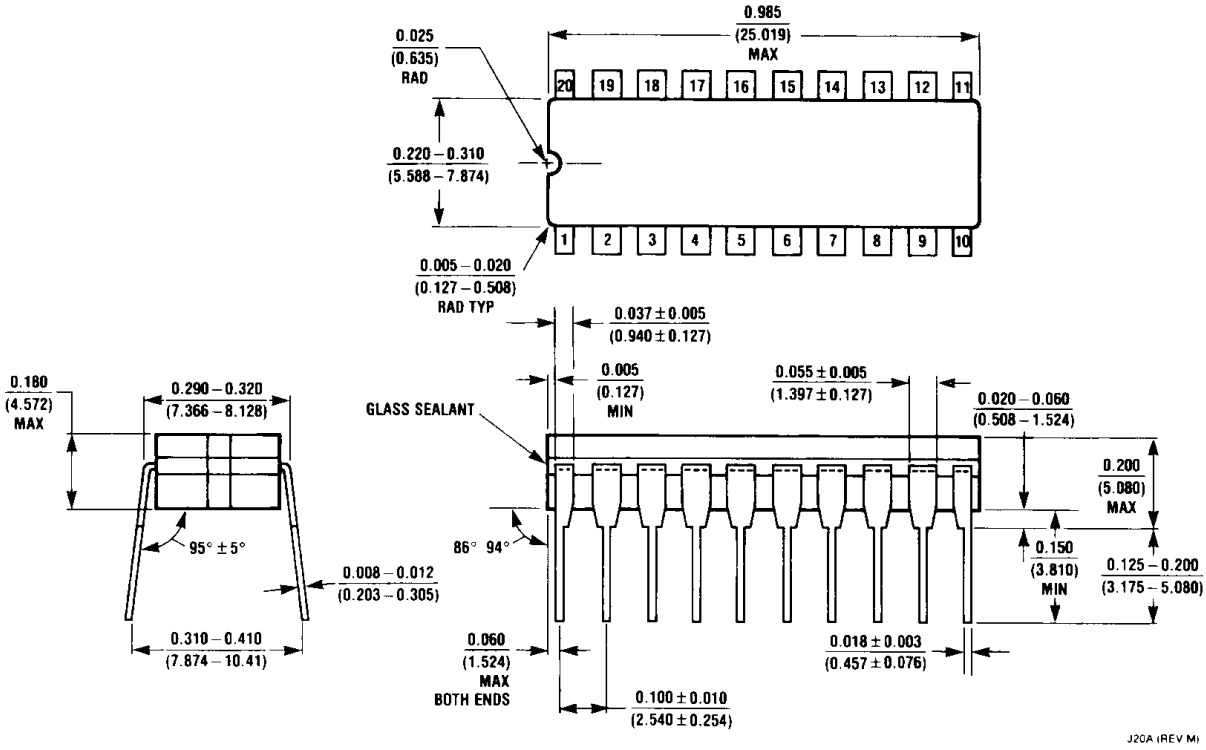
When a switch is turned OFF or ON, transient signals will appear at the load due to injection of charge from the FET gate to the channel. These transients are on the order of 500 mV in amplitude and 100 ns in duration, depending on the load impedance.

Physical Dimensions inches (millimeters)

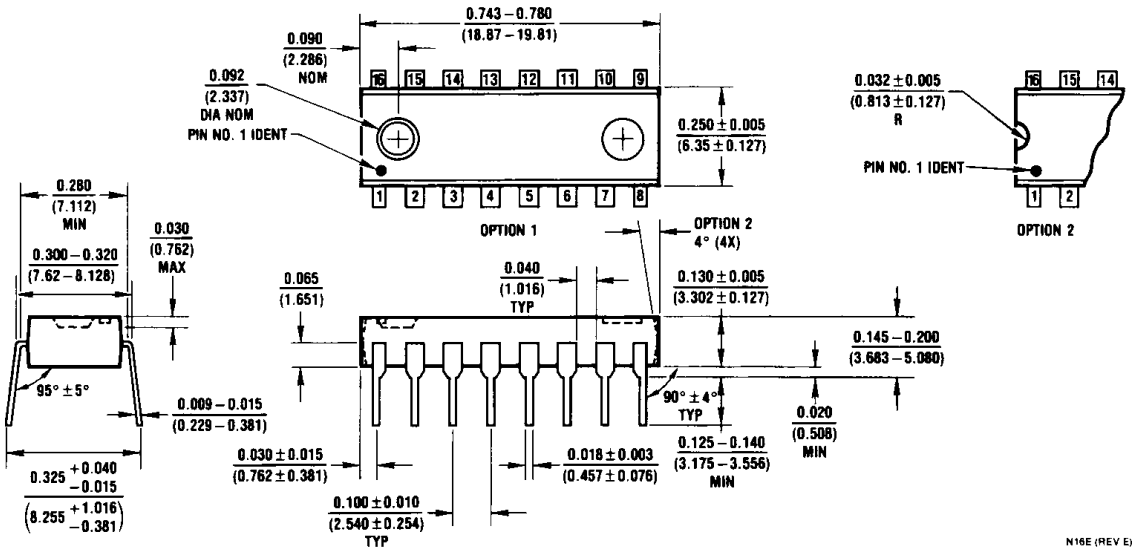


Ceramic Dual-In-Line Package (J)
Order Number LMC13204J, LMC13334J,
NS Package J16A

Physical Dimensions inches (millimeters) (Continued)

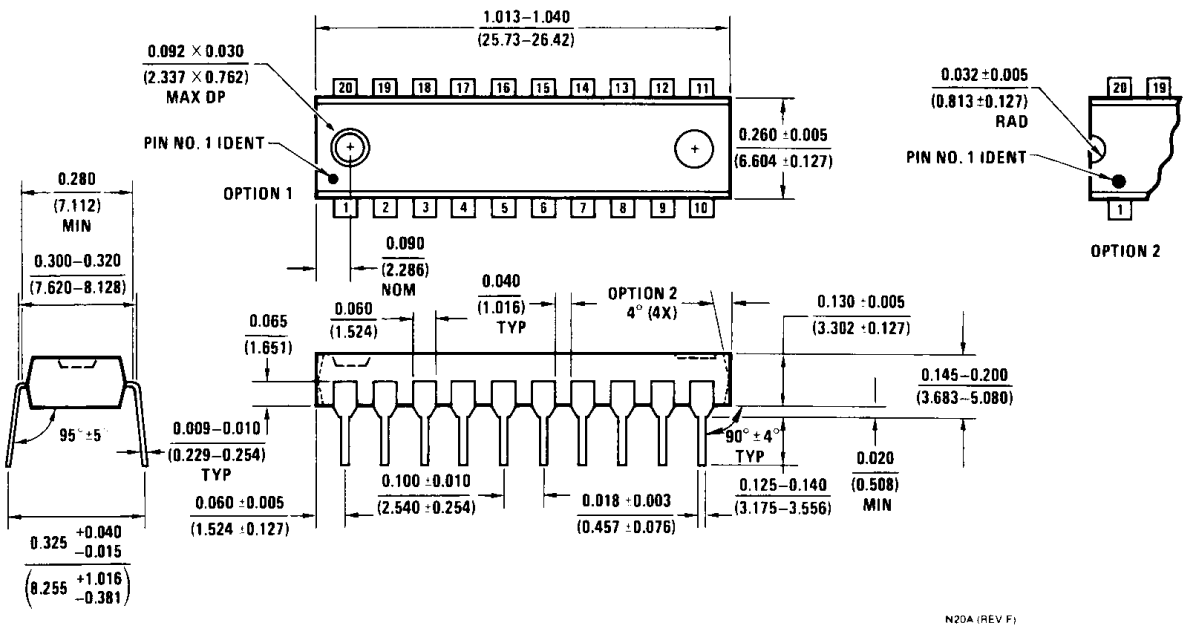


Ceramic Dual-In-Line Package (J)
Order Number LMC13335J
NS Package J20A



Molded Dual-In-Line Package (N)
Order Number LMC13204N, LMC13334N
NS Package N16E

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LMC13335N
NS Package Number N20A

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