National Semiconductor

LH0084/LH0084C Digitally-Programmable-Gain Instrumentation Amplifier

General Description

The LH0084/LH0084C is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

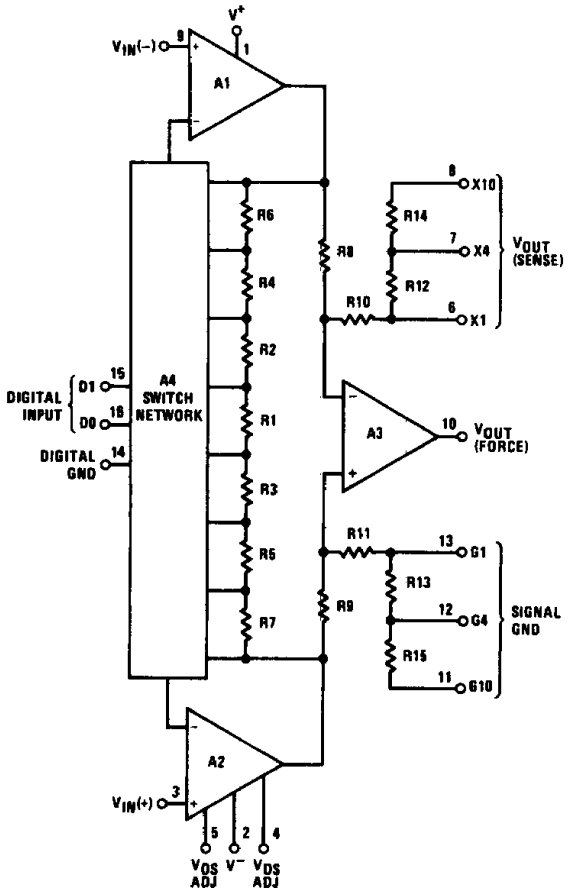
The device exhibits high input impedance, low offset voltage, high PSRR, high speed, and excellent gain accuracy and gain non-linearity.

The LH0084 is guaranteed from −55°C to +125°C. The LH0084C is guaranteed from −25°C to +85°C. Both devices are provided in a hermetically sealed 16-lead dual-in-line metal package.

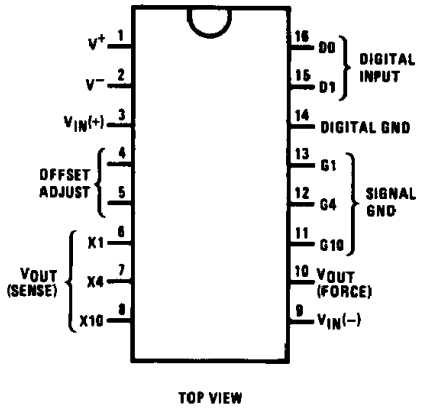
Features

■ Excellent gain accuracy	0.075% max
and low gain non-linearity	0.01% typ
■ Extremely low gain drift	1 ppm/°C typ
	10 ppm/°C max
■ High input impedance	$10^{11}\Omega$typ
■ High PSRR	70 dB min
■ TTL compatible digital inputs	
■ High speed, settling to 0.1%	4 μs max

Simplified Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Case is electrically isolated

Order Number LH0084D or LH0084CD
See NS Package D16D

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage (Note 1)	±18V
Analog Input Voltage (Note 2)	±15V
Differential Input Voltage (Note 2)	±30V
Digital Input Voltage	−4V, +18V
Power Dissipation (Note 5)	2.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0084	−55°C to +125°C
LH0084C	−25°C to +85°C
Lead Temp. (Soldering, 10 seconds)	+260°C
ESD rating to be determined.	

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Symbol	Parameter	Conditions		LH0084 Min	LH0084 Typ	LH0084 Max	LH0084C Min	LH0084C Typ	LH0084C Max	Units
V_{IOS}	Input Offset Voltage		$T_j = 25°C$		0.3	5		0.3	10	mV
						7			13	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Change with Temperature	$R_S = 100\Omega$ $V_{CM} = 0$ (Note 3)			10			10		µV/°C
V_{OOS}	Output Offset Voltage		$T_j = 25°C$		0.6	5		0.6	10	mV
						7			13	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Change with Temperature				20			20		µV/°C
I_B	Input Bias Current (Note 4)		$T_j = 25°C$		150	500		150	500	pA
						500			100	nA
I_{OS}	Input Offset Current		$T_j = 25°C$		50	200		50	200	pA
						200			50	nA
R_{IN}	Input Resistance	Differential			10^{11}			10^{11}		Ω
		Common-Mode			10^{11}			10^{11}		
V_{IN}	Input Voltage Range			±10			±10			V
A_V	Voltage Gain	See Table I			1 2 5 10 20 50 100			1 2 5 10 20 50 100		V/V
	Gain Error	$A_V = 1, 2, 5$	$T_A = 25°C$		0.01	0.075		0.02	0.15	%
		$A_V = 10, 20, 50, 100$			0.02	0.1		0.03	0.2	
		$A_V = 1, 2, 5$			0.02	0.2		0.02	0.2	
		$A_V = 10, 20, 50, 100$			0.03	0.3		0.03	0.3	
	Gain Nonlinearity		$T_A = 25°C$		0.002			0.002		
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient				1	10		1	10	ppm/°C
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_V = 1$	70	80		70	80		dB
			$A_V = 10$	76	94		76	94		
			$A_V = 100$	80	94		80	94		
PSRR	Power Supply Rejection Ratio	$\pm 8V \le V_S \le +18V$	$A_V = 1$	70	84		70	84		dB
			$A_V = 10$	76	92		76	92		
			$A_V = 100$	80	104		80	104		
V_O	Output Voltage Swing	$R_L \ge 10\ k\Omega$		±10	±12		±10	±12		V
I_O	Output Short Circuit Current		$T_A = 25°C$	±5	±18	±40	±5	±18	±40	mA
				±2		±40	±2		±40	

DC Electrical Characteristics (Continued) $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Symbol	Parameter	Conditions	LH0084			LH0084C			Units
			Min	Typ	Max	Min	Typ	Max	
R_O	Output Resistance			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage				0.7			0.7	V
V_{IH}	Digital "1" Input Voltage		2.0			2.0			V
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$		1.5	40		1.5	40	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$		0.01			0.01		μA
V_S	Supply Voltage Range		±8		±18	±8		±18	V
$I_S(+)$	Positive Supply Current	$V_S \le \pm 18V$		12	18		12	26	mA
$I_S(-)$	Negative Supply Current	$V_S \le \pm 18V$		8	12		8	14	mA
P_D	Power Dissipation	$V_S = \pm 15V$		315	450		315	600	mW

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
BW	Bandwidth (*Figure 1*)	Small Signal, −3 dB	$A_V = 1$		3250		kHz
			$A_V = 10$		500		
			$A_V = 100$		350		
		Small Signal, −1%	$A_V = 1$		300		
			$A_V = 10$		75		
			$A_V = 100$		55		
PBW	Power Bandwidth	$V_O = \pm 10V$			200		
SR	Slew Rate			10	13		V/μs
t_s	Settling Time (*Figure 2*) ±0.1%	$\Delta V_o = \pm 20V$	$A_V = 1$		2.3	3.0	μs
			$A_V = 10$		2.7	3.5	
			$A_V = 100$		3.1	4.0	
	Gain Switching Time				3.5		
E_N	Equivalent Input Noise Voltage (*Figure 3*)	BW = 0.1 Hz − 10 Hz	$A_V = 100$		7		μVp-p
		BW = 10 Hz − 10 kHz			1.4		μVrms
I_N	Equivalent Input Noise Current (*Figure 3*)	BW = 10 Hz − 10 kHz			30		pArms

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection section under Applications Information.

Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: These parameters are specified at junction temperature, T_J. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient.

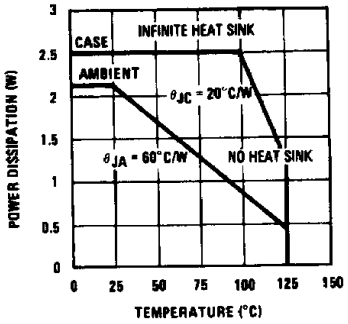
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Note 5: See Typical Performance Characteristics for Thermal Resistance Information.

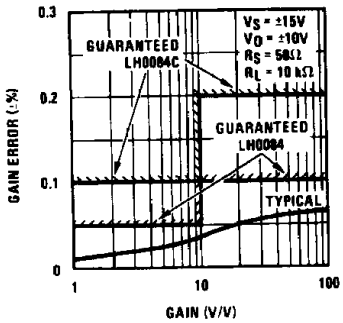
Note 6: Refer to RETS0084D for LH0084D military specifications.

Typical Performance Characteristics

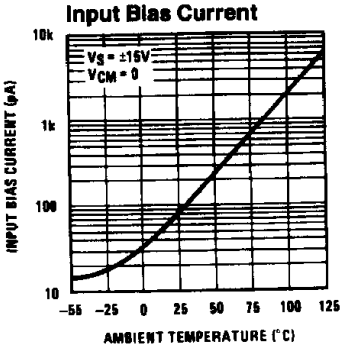
Power Dissipation



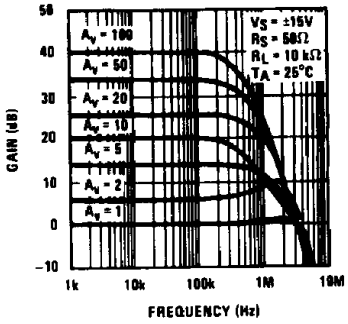
Gain Accuracy



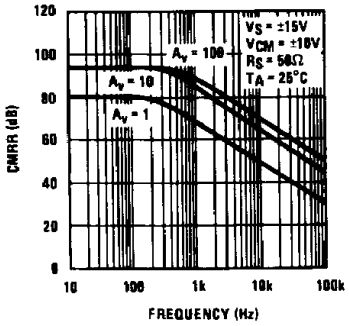
Input Bias Current



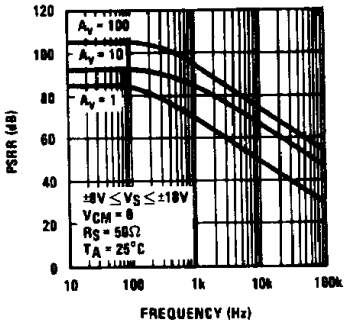
Small Signal Frequency Response



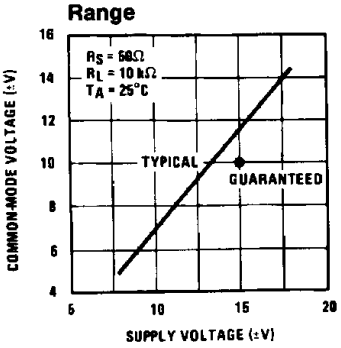
Common-Mode Rejection



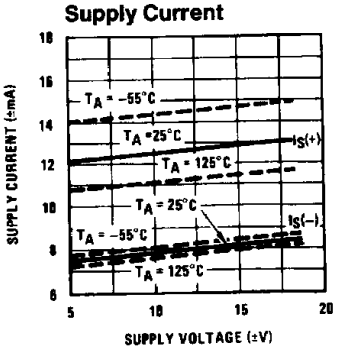
Power Supply Rejection



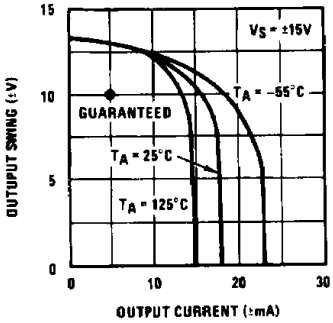
Input Common-Mode Range



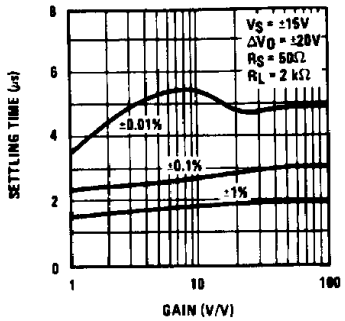
Supply Current



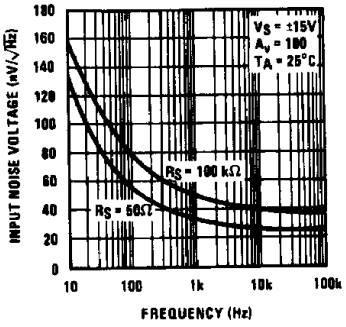
Output Swing



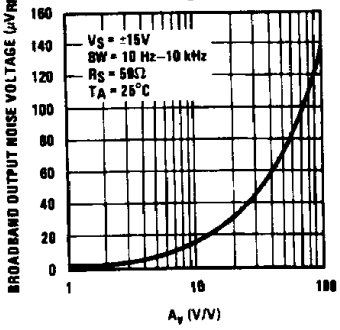
Settling Time



Equivalent Input Noise Voltage (Includes Source-Resistance Noise)



Broadband Output Noise Voltage



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AC Test Circuits

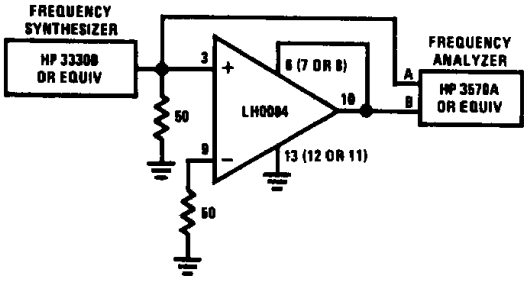


FIGURE 1. Frequency Response Measurement Circuit

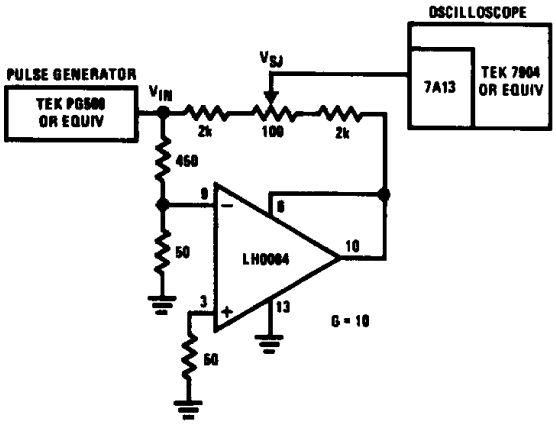
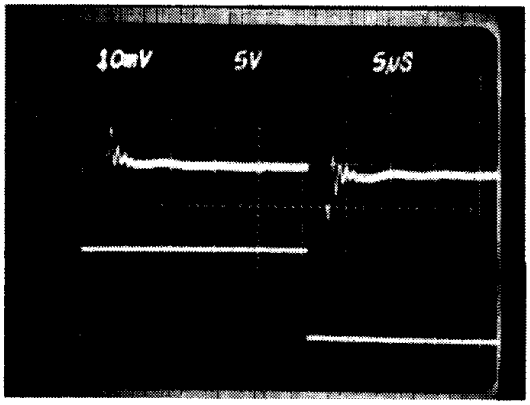


FIGURE 2. Settling Time Measurement Circuit

Settling Time



$A_V = 10$ Input Stage

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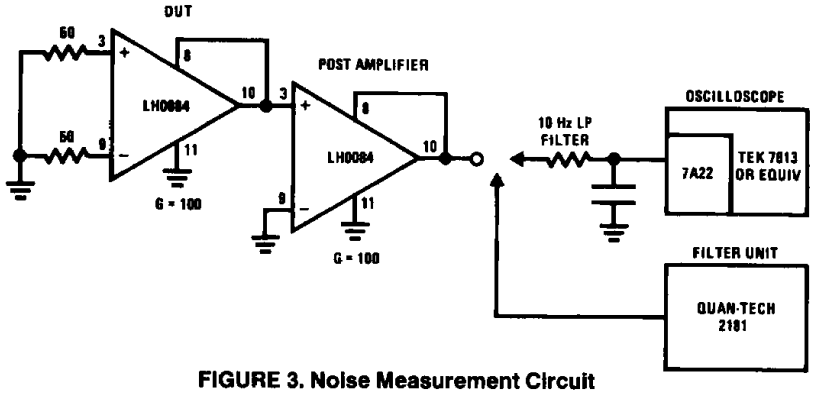

FIGURE 3. Noise Measurement Circuit

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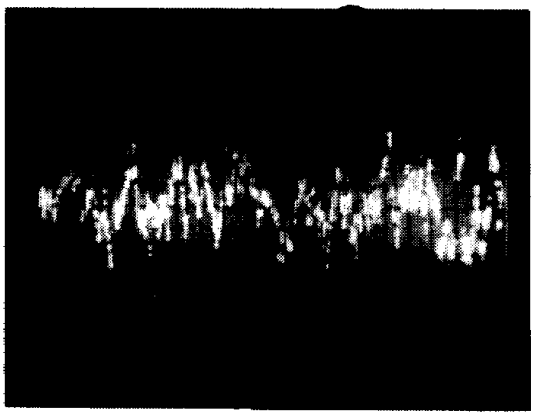
Wideband Noise



$R_S = 50\Omega$ Bandwidth 0.1 Hz to 10 Hz
1μV/Division Vertical 5 Seconds/Division Horizontal

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Applications Information

THEORY OF OPERATION

The LH0084 is a digitally-programmable-gain true-instrumentation amplifier composed of a variable-gain voltage-follower input stage (A1 and A2), followed by a differential output stage (A3). The schematic is shown in *Figure 4*.

The input stage contains matched high-speed FET-input op amps (A1 and A2). A high-stability temperature-compensated resistor network (R1 through R7) controls feedback ratios at the inverting inputs of op amps A1 and A2 via FET switches S1A–S4A and S1B–S4B. Since the FET switches are in series with the op amp input impedance their resistance match and temperature drift do not degrade the gain accuracy of the instrumentation amplifier. The FET switches are controlled through a 1-of-4 decoder and switch driver, by the logic levels applied at the digital input terminals D1 and D0 and set the gain of the input stage as shown in Table I.

If, for example, D1 is High (≥2.0V) and D0 is Low (≤0.7V), FET switch pair S3A and S3B will be closed (and all remaining switches open). The input stage gain, $A_{V(1)}$, can then be shown to be:

$$A_{V(1)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)}$$

$$= 1 + \frac{R4 + R5 + R6 + R7}{R1 + R2 + R3}$$

$$= 1 + \frac{6k + 6k + 10k + 10k}{4k + 2k + 2k}$$

$$= 5$$

Schematic Diagram

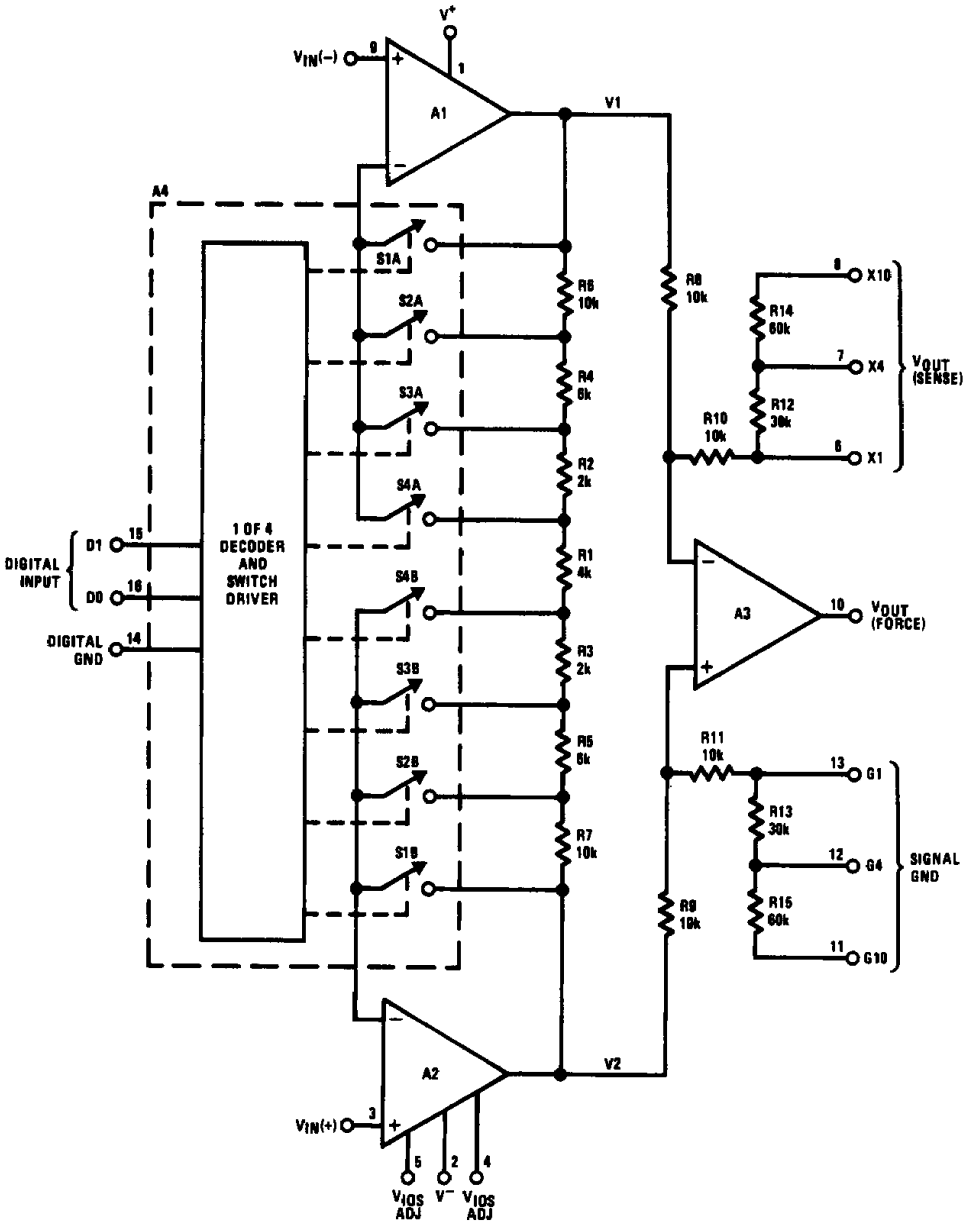

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FIGURE 4

Applications Information (Continued)

TABLE I. Gain Truth Table and Connection Table

Digital Inputs		1st Stage Gain	Pin Connections	2nd Stage Gain	Overall Gain
D1	D0	$A_{V(1)}$		$A_{V(2)}$	A_V
0	0	1	6-10, 13-GND	1	1
0	1	2			2
1	0	5			5
1	1	10			10
0	0	1	7–10, 12-GND	4	4
0	1	2			8
1	0	5			20
1	1	10			40
0	0	1	8–10, 11-GND	10	10
0	1	2			20
1	0	5			50
1	1	10			100

The output stage, consisting of op amp A3 and resistors R8 through R15, converts the voltage difference at the output of the input stage, V2 minus V1, to a single-ended output. For increased flexibility of the LH0084, the output stage gain is pin-strappable by selecting R10, R10+R12, or R10+R12+R14 as feedback resistor for A3. The ratios of these resistors to the differential stage input resistor R3 are kept very accurate to maintain the excellent overall gain accuracy of the device. The output stage gain, $A_{V(2)}$, is equal to the feedback resistance divided by the input resistance. Thus with, for example, Pin 7 wired to Pin 10, that gain would be:

$$A_{V(2)} = \frac{V_{OUT}}{V2-V1} = \frac{R10+R12}{R8} = \frac{10K+30K}{10k} \quad (2)$$

To preserve the high common-mode rejection ratio of the output stage, the ground sense resistor, R11, R11+R13 or R11+R13+R15, must match the feedback resistor used.

The overall gain of the LH0084 is therefore:

$$A_V = \frac{V_{OUT}}{V_{IN}(+)-V_{IN}(-)} = \frac{V2-V1}{V_{IN}(+)-V_{IN}(-)} \bullet \frac{V_{OUT}}{V2-V1} = A_{V(1)} \bullet A_{V(2)} \quad (3)$$

The different gains available are in the range of 1 through 100 and are summarized in Table I.

POWER SUPPLY CONNECTIONS

Proper power supply connections are shown in *Figure 5*. The power supplies should be bypassed to ground as close as possible to device supply pins. For optimum high speed performance V^+ and V^- should be decoupled with a 0.01 μF ceramic disc in parallel with a 1 μF electrolytic capacitor.

The two ground pins, analog and digital grounds, should be connected together as close to the device as possible, preferably with a ground plane underneath the device. If this is not possible, the grounds should be connected together locally with back-to-back diodes and hard-wired together offboard. If a ground reference offset is used, it must be low impedance compared to the ground sense resistance to avoid CMRR degradation.

Care must be taken in the supply power-on sequence. The LH0084 may suffer irreversible damage if the V^+ supply is applied prior to the powering on the V^- supply. In most applications using dual tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in *Figure 5*.

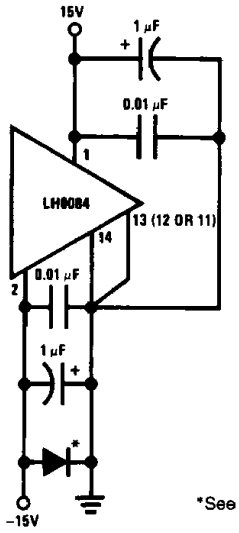

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FIGURE 5. Power Supply Connections

Applications Information (Continued)

SIGNAL CONNECTIONS

The input signals should be connected as shown in *Figure 6*. To minimize errors, $R_S(+)$, $R_S(-)$ and R_{CM} should be kept as small as possible.

The output connections are also shown in *Figure 6*. The feedback leads should be kept short as should the ground sense in order to minimize lead resistance and parasitic capacitance.

OFFSET AND GAIN ADJUSTMENTS

Special care must be taken when using external offset adjustment. Since the LH0084 is a 2-stage amplifier with each stage contributing offset errors, and the amplifier presumably is used at several different gains, it is important to realize that the offsets of both the 1st and the 2nd stages must be nulled to maintain zero offset referred to output (RTO) at all gain settings.

In general, it is recommended that the input stage offset (V_{IOS}) be adjusted with a potentiometer as shown in *Figure 7*. The output stage offset (V_{OOS}) is ideally adjusted at a subsequent gain stage (i.e. sample-and-hold or A-to-D converter), but if this is impractical, it may also be done as shown in *Figure 7*.

Recommended offset adjust procedure is as follows: Initially set both pots to center positions and short both inputs of the LH0084 to ground.

a) Set the input stage gain to 1 (pull D1 and D0 low). Measure the output voltage, V_{OUT1}.

b) Set the input stage gain to 10 (pull D1 and D0 high). Measure the new output voltage, V_{OUT2}.

c) Calculate the portion of V_{OUT2} contributed by the output stage offset per the equation:

$$V_{OOS} = \frac{1}{9}(10 \bullet V_{OUT1} - V_{OUT2}) \quad (4)$$

d) While maintaining an input stage gain of 10, adjust the input offset voltage (V_{IOS}) potentiometer until the output voltage is equal to the voltage calculated in Equation (4).

e) Change the input back to a gain of 1 and adjust the output offset voltage (V_{OOS}) potentiometer until the output voltage is zero.

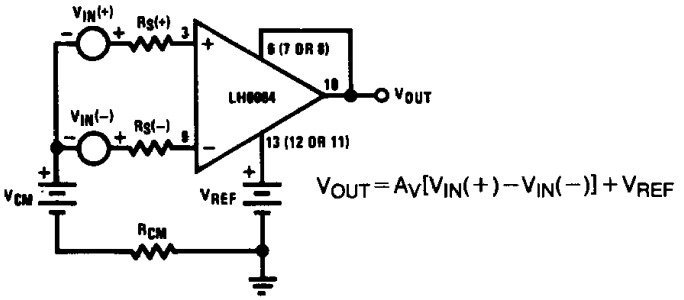

FIGURE 6. Signal Connections

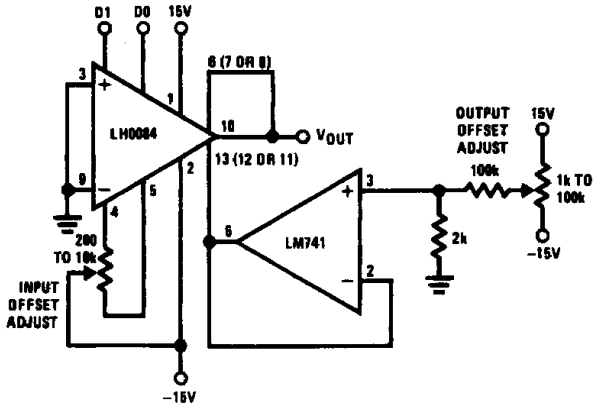

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FIGURE 7. Offset Adjust Circuit

Applications Information (Continued)

An alternate offset adjust scheme is shown in *Figure 8*. The offset should be rezeroed after each time the gain is changed or when the op amp integrator drift warrants a new zero pulse. An additional advantage of this adjustment technique is that it can also be used to cancel out offset voltage drift and common-mode voltage error contributions.

External gain adjustment is generally discouraged since gain accuracy can be optimized for one gain setting only. If gain adjustment is required, however, it should be done at a subsequent gain stage.

LOGIC CONNECTIONS

The digital inputs D1 and D0 are referenced to the digital ground. The device interfaces directly to TTL and, with pull-down resistors, to CMOS.

Interfacing with microprocessors will usually require a latch. A circuit using full 6-bit wide address decode and write strobe is shown in *Figure 9*.

REMOTE OUTPUT SENSE

The feedback resistors of the LH0084 can be connected directly at the load in order to eliminate errors due to lead resistance *(Figure 10)*.

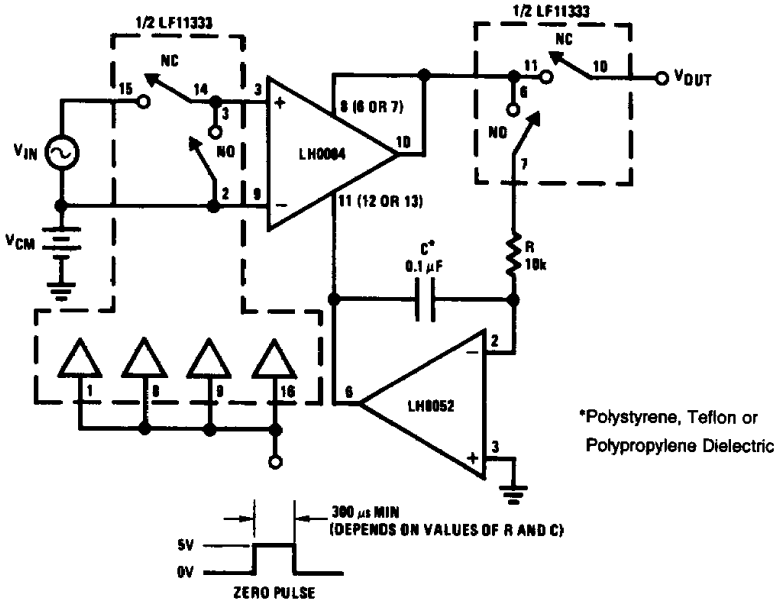

FIGURE 8. Auto Zero Circuit

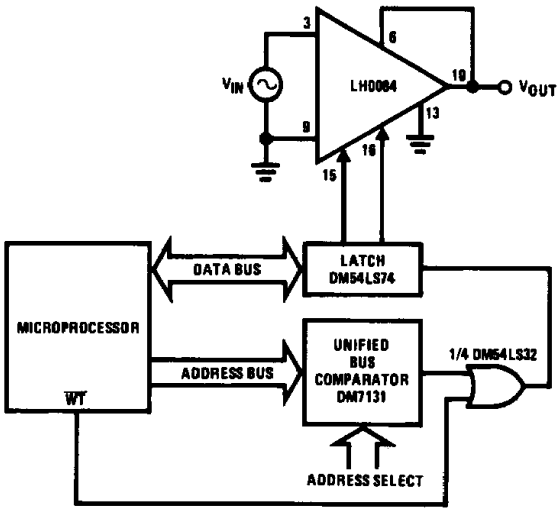

FIGURE 9. Typical Microprocessor Interface

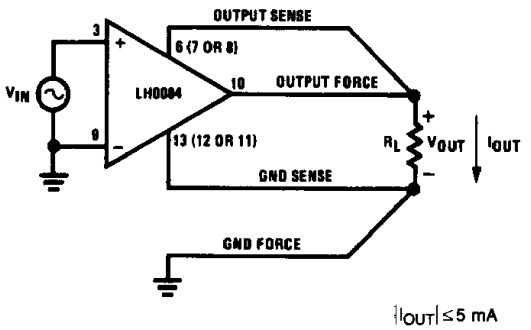

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FIGURE 10. Remote Sense Connection

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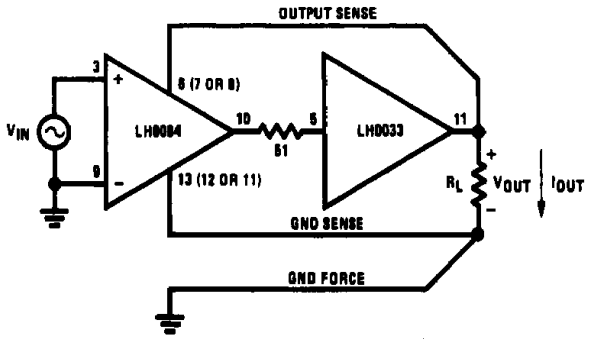
Applications Information (Continued)

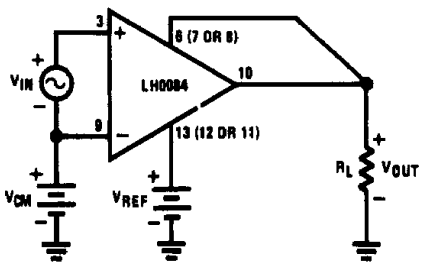
Also, a unity gain buffer, such as the LH0033, may be included in the feedback loop for increased current drive capability as shown in *Figure 11*.

The output sense feature can also be used in other ways such as output offset, *Figure 12*, or current source output, *Figure 13*.



$|I_{OUT}| \leq 90$ mA

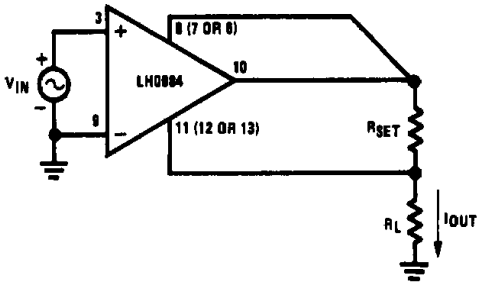
FIGURE 11. Buffered Output Connection



$V_{OUT} A_V \cdot V_{IN} + V_{REF}$

$|V_{OUT}| \leq 10V$

FIGURE 12. Output Offset Connection



$$I_{OUT} = \frac{A_V \cdot V_{IN}}{R_{SET}}$$

$|I_{OUT}| \leq 5$ mA

$|I_{OUT}(R_L + R_{SET})| \leq 10V$

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FIGURE 13. Output Current Source Connection

Applications

The LH0084 is ideal for application in increased dynamic range A-to-D converters, test systems, process control, and multi-channel data acquisition system. *Figure 14* shows the device used in a typical data acquisition system.

A software offset and gain error correction scheme is shown in *Figure 15*. By first selecting a multiplexer input connected to analog ground, and then selecting a channel connected to a reference of known value, the overall system gain and offset errors can be calculated. For all subsequent readings, offset and gain corrections can be made mathematically by solving a simple first-order equation in software.

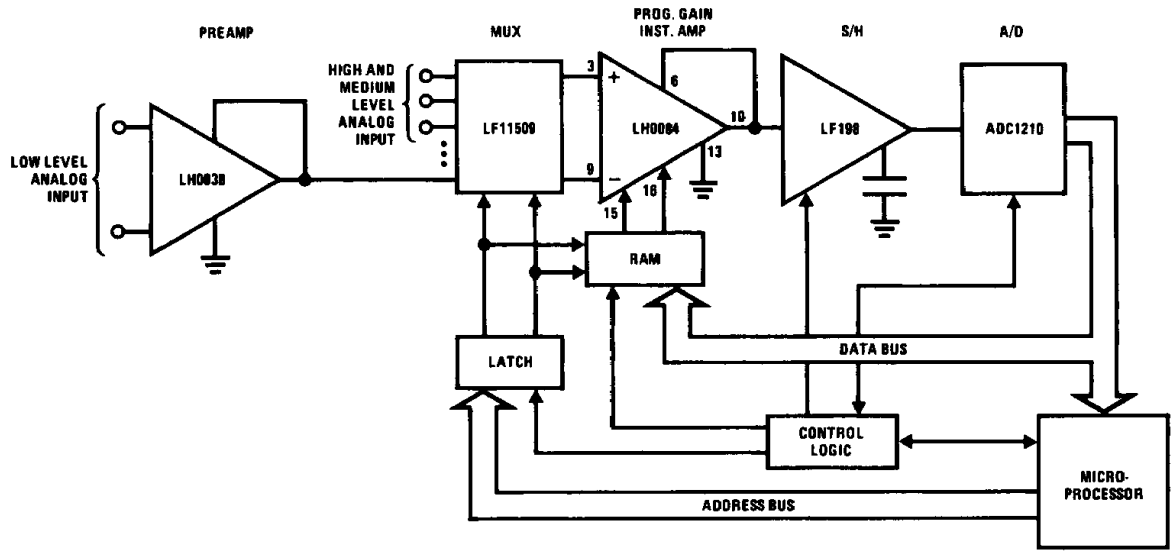

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FIGURE 14. Typical Data Acquisition System

Applications (Continued)

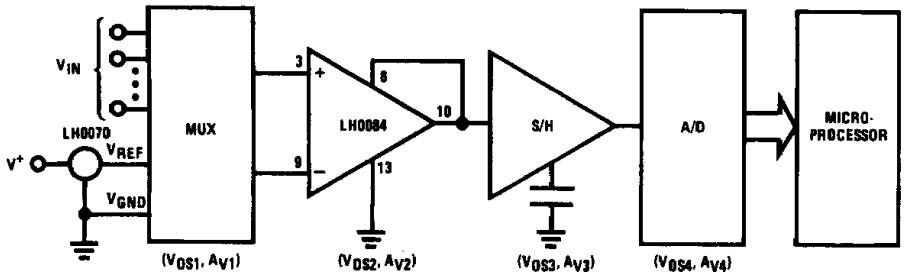

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FIGURE 15. Software System Offset and Gain Calibration Circuit

Definition of Terms

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the output of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and using the following equation:

$$V_{IOS}=\frac{1}{9}\left(V_{OS}|_{A_V=10}-V_{OS}|_{A_V=1}\right)$$

where:

$V_{OS}|_{A_V=10}$ = Overall offset (RTO) for $A_V=10$

$V_{OS}|_{A_V=1}$ = Overall offset (RTO) for $A_V=1$

Input Offset Current, I_{OS}: The difference in the currents into the 2 analog input terminals at 0V.

Input Bias Current, I_B: The average of the currents into the 2 analog input terminals at 0V.

Input Resistance, R_{IN}: Common-mode input resistance is the change in input voltage range divided by the change in input bias current with both analog inputs at the same voltage. Differential input resistance is the change in input voltage at one input terminal divided by the change in input current at the other input terminal which is kept still at 0V.

Input Voltage Range, V_{IN}: The voltage range for which the device is operational.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the change in input offset voltage over this range.

Power Supply Rejection Ratio, PSRR: The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

Voltage Gain, A_V: The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full-scale (10V for operation with ±15V supply). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage for the output to be forced to 0V. V_{OOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and applying the following equation:

$$V_{OOS}=\frac{1}{9}\left(10 \bullet V_{OS}|_{A_V=1}-V_{OS}|_{A_V=10}\right)$$

where:

$V_{OS}|_{A_V=1}$ = Overall offset (RTO) for $A_V=1$

$V_{OS}|_{A_V=10}$ = Overall offset (RTO) for $A_V=10$

Offset Voltage (Referred to Output), $V_{OS(RTO)}$: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input offset voltage, V_{IOS}, and output offset voltage, V_{OOS}, and is a function of amplifier gain. The overall offset voltage is given by:

$$V_{OS(RTO)}=A_{V(2)}(A_{V(1)}\ V_{IOS}+V_{OOS})$$

where:

V_{IOS} = Input offset voltage

V_{OOS} = Output stage offset voltage

$A_{V(1)}$ = Input state gain

$A_{V(2)}$ = Output stage gain

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Definition of Terms (Continued)

Output Voltage Swing, V_O: The peak output voltage swing referenced to ground into specified load.

Output Short-Circuit Current, I_O: The current supplied by the device with the output connected directly to ground.

Output Resistance, r_o: The ratio of change in output voltage to change in output current around zero output.

Supply Voltage Range, V_s: The supply voltage range for which the device is operational.

Supply Current, I_s: The current required from the supply to operate the device with zero load and with the analog as well as the digital inputs at 0V.

Power Dissipation, P_D: The power dissipated in the device with zero load and with the analog as well as the digital inputs at 0V.

Digital "1" Input Voltage, V_{IH}: Minimum voltage required at the digital input to guarantee a high logic state.

Digital "0" Input Voltage, V_{IL}: Maximum voltage required at the digital input to guarantee a low logic state.

Digital "1" Input Current, I_{IH}: The current into a digital input at specified logic level.

Digital "0" Input Current, I_{IL}: The current into a digital input at specified logic level.

Average Input Offset Voltage Drift, $\Delta V_{IOS}/\Delta T$: The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Output Offset Voltage Drift, $\Delta V_{OOS}/\Delta T$: The ratio of output offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Gain Temperature Coefficient, $\Delta A_V/\Delta T$: The ratio of change in gain from 25°C to either temperature extreme divided by the temperature range.

Small Signal Bandwidth, BW: The frequency at which the device gain changes from the low frequency gain by a specified amount.

Power Bandwidth, PBW: Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

Slew Rate, SR: The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

Settling Time, t_s: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

Equivalent Input Noise Voltage, E_N: The rms of peak noise voltage referred to the input (RTI) over a specified frequency band.

Equivalent Input Noise Current, I_N: The rms of peak noise current referred to the input (RTI) over a specified frequency band.