

DATA SHEET

SA57026

300 mA LDO with ON/OFF control and independent delayed RESET function

Product data
Supersedes data of 2001 Oct 03

2003 Oct 13

300 mA LDO with ON/OFF control and independent delayed RESET function

SA57026

GENERAL DESCRIPTION

The SA57026 has an extremely precise fixed output with a typical accuracy of $\pm 2\%$. It is designed to provide very low dropout and low noise in CD-ROM drives, battery-operated systems, and portable computers applications. This regulator consists of an internal voltage reference, an error amplifier, a driver with current limiter, and a thermal shut-down mechanism.

An Active-LOW $\overline{\text{RESET}}$ is asserted when the detected voltage (V_{DET}) falls below the reset voltage threshold. The $\overline{\text{RESET}}$ output remains low for 30 μs (typical) when zero capacitance connected to Cd pin. The reset time delay can be adjusted by replacing capacitance values from Cd pin to Ground.

The device is available in the 7-pin small outline package (SOP002).

FEATURES

- Very low dropout voltage: 500 mV typ. ($I_{\text{out}} = 50 \text{ mA}$)
- High precision output voltage: $\pm 2\%$
- Output current capacity: 300 mA
- Low noise: 40 mV_{rms} typ. @ 20 Hz to 80 KHz and for $C_n = 10 \text{ nF}$
- Extremely good line regulation: 10 mV typical
- Extremely good load regulation: 20 mV typical
- Low temperature drift co-efficient to V_{out} : $\pm 100 \text{ ppm}/^\circ\text{C}$
- Internal current limit and thermal shut-down circuits
- Adjustment-free reset detection voltage: 4.2 V typ.
- Delay time can be adjusted by external capacitor
- Wide operating temperature range: -40°C to $+85^\circ\text{C}$

APPLICATIONS

- CD-ROM drives
- Electronic notebooks, PDAs and palmtop computers
- Cameras, VCRs and camcorders
- PCMCIA cards
- Modems
- Battery-operated or hand-held instruments

BLOCK DIAGRAM

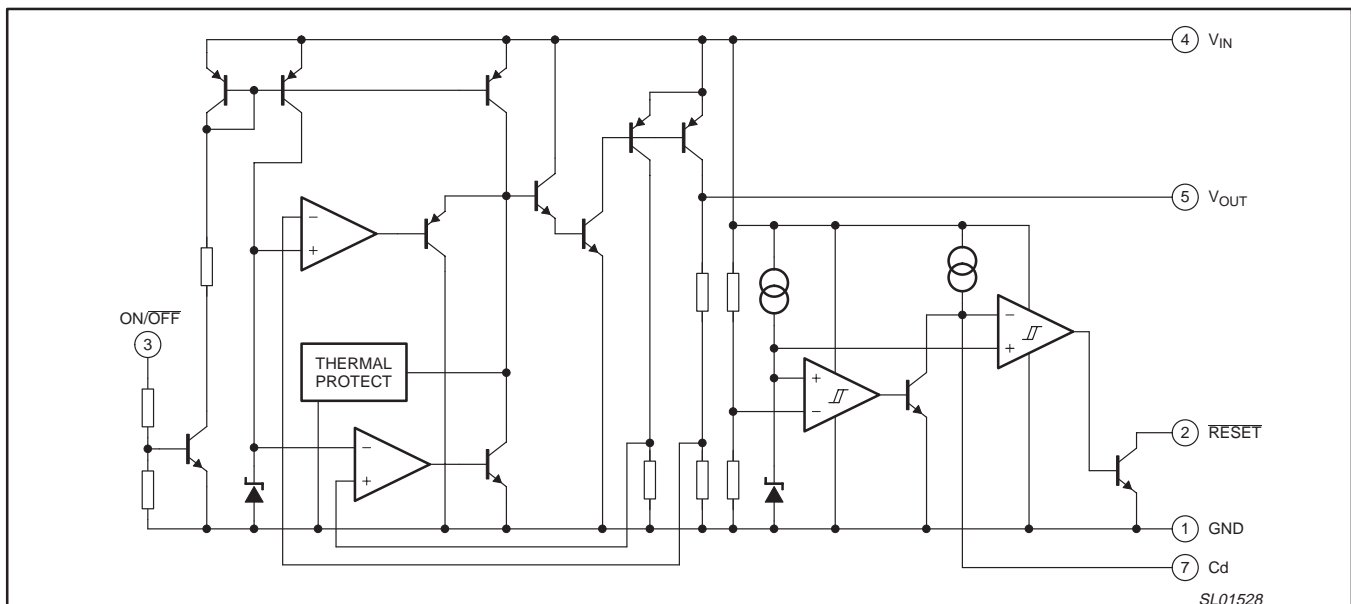


Figure 1. Block diagram.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	DESCRIPTION	VERSION	
SA57026	small outline 7-pin surface mount (see dimensional drawing)	SOP002	-40 to +85 °C

NOTE:

The device has two reset threshold options.

XX	Output voltage (Typ.)	Reset threshold (Typ.)
SA57026D	3.3 V	4.20 V
SA57026F	3.3 V	3.90 V

Part number marking

Part number	Marking
SA57026DD	A L U
SA57026FD	A L V

PIN CONFIGURATION

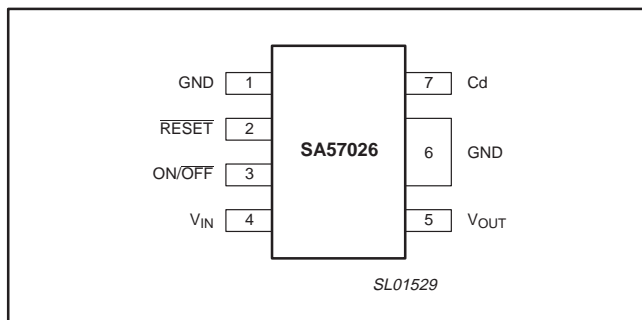


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	Ground.
2	RESET	RESET signal output pin. The output remains low while V_{DET} is below the reset voltage threshold, and for an external set time delay Cd pin after V_{DET} rises above reset threshold.
3	ON/OFF	Output voltage on/off control pin. Connect to V_{IN} if not used. ON/OFF = LOW: Voltage output (Pin 5) OFF ON/OFF = HIGH: Voltage output (Pin 5) ON
4	V_{IN}	Voltage supply input pin.
5	V_{OUT}	Regulated voltage output pin.
6	GND	Ground pin and heat sink.
7	Cd	Reset delay time capacitor pin. RESET pin output delay time can be set by capacitance connected to the Cd pin. $t_{PLH} = 100000 \times C$ t_{PLH} : transmission delay time (s). C: capacitor value (F).

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{IN}	Supply voltage	-0.3	+10	V
I_{OUT}	Output current	0	400	mA
T_{oper}	Operating temperature	-40	+85	°C
T_{stg}	Storage temperature	-40	+125	°C
P_D	Power dissipation (Note 1)	-	800	mW

NOTE:

1. When mounted on a 25 × 40 × 1 mm glass epoxy board.

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ELECTRICAL CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{ON/OFF} = 1.6\text{ V}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{ccq1}	No-load input current 1	$V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ mA}$	–	3	8	mA
I_{ccq2}	No-load input current 2	$V_{IN} = 4\text{ V}$; $I_{OUT} = 0\text{ mA}$	–	4	–	mA
I_{ccq3}	Input current (OFF)	$V_{IN} = 5\text{ V}$; $V_{ON/OFF} = 0.4\text{ V}$	–	250	–	μA
Regulator						
V_{OUT}	Output voltage	$V_{IN} = 5\text{ V}$; $I_{OUT} = 30\text{ mA}$ SA57026D SA57025F	3.25 3.25	3.30 3.30	3.35 3.35	V V
V_{IO}	Input/output differential voltage	$V_{IN} = 3.2\text{ V}$; $I_{OUT} = 150\text{ mA}$	–	0.15	0.3	V
V_1	Line regulation	$V_{IN} = 4.4\text{ to }5.5\text{ V}$; $I_{OUT} = 30\text{ mA}$	–	10	20	mV
V_2	Load regulation	$V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ to }300\text{ mA}$	–	20	120	mV
$\Delta V_{OUT}/\Delta T$	V_{OUT} Temperature coefficient (Note 1)	$T_j = -20\text{ to }+85\text{ }^{\circ}\text{C}$; $V_{IN} = 5\text{ V}$	–	100	–	ppm/ $^{\circ}\text{C}$
RR	Ripple rejection (Note 1)	$V_{IN} = 5\text{ V}$; $f = 120\text{ Hz}$; $V_{ripple} = 1\text{ V}_{p-p}$; $I_{OUT} = 30\text{ mA}$	–	50	80	dB
V_n	Output noise voltage (Note 1)	$V_{IN} = 5\text{ V}$; $f = 20\text{ to }80\text{ kHz}$; $V_{ripple} = 1\text{ V}_{p-p}$; $I_{OUT} = 30\text{ mA}$	–	40	120	μV_{rms}
I_{ON}	ON/OFF terminal current	$V_{ON/OFF} = 1.6\text{ V}$	–	5	10	μA
$V_{th(H)}$	HIGH threshold voltage		1.6	–	$V_{IN}+0.3$	V
$V_{th(L)}$	LOW threshold voltage		–0.3	–	0.4	V
Reset						
V_{DET}	Detection voltage	$V_{IN} = \text{HIGH-to-LOW}$ SA57026D SA57025F	4.11 3.81	4.20 3.90	4.29 3.99	V V
$\Delta V_S/\Delta T$	V_S temperature coefficient (Note 1)	$T_j = -20\text{ to }+85\text{ }^{\circ}\text{C}$	–	100	–	ppm/ $^{\circ}\text{C}$
ΔV_S	Hysteresis voltage	$V_{IN} = \text{HIGH-to-LOW-to-HIGH}$	100	–	200	mV
V_{OL}	LOW-level output voltage	$V_{IN} = 3.9\text{ V}$; $R_L = 4.7\text{ k}\Omega$	–	100	200	mV
I_{LO}	Output leakage current	$V_{IN} = 5\text{ V}$	–	–	± 0.1	μA
I_{OL1}	LOW-level output current 1	$V_{IN} = 3.9\text{ V}$; $R_L = 0\text{ }\Omega$	5	–	–	mA
I_{OL2}	LOW-level output current 2 (Note 1)	$V_{IN} = 3.9\text{ V}$; $R_L = 0\text{ }\Omega$; $T_{amb} = -20\text{ to }+80\text{ }^{\circ}\text{C}$	3	–	–	mA
t_{PLH}	LOW-to-HIGH transmission delay time (Note 1)	$C_d = 0.0\text{ }\mu\text{F}$	–	30	90	μs
t_{PLH1}	Reset delay time	$V_{IN} = 4\text{ V to }5\text{ V}$; $C_d = 0.1\text{ }\mu\text{F}$	5	10	20	ms
t_{PHL}	HIGH-to-LOW transmission delay time (Note 1)		–	30	90	μs
V_{OPL}	Threshold operating voltage	$V_{OL} = 0.4\text{ V}$	–	0.65	0.85	V

NOTE:

- The parameter is guaranteed by design.

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APPLICATION INFORMATION

Input capacitor

An input capacitor of $\geq 1 \mu\text{F}$ is required to eliminate the AC coupling noise. This capacitor must be located as close as possible to V_{IN} or GND pin (not more than 1 cm) and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitor will work.

Output capacitor

Phase compensation is made for securing stable operation, even if the load current varies. For this reason, an output capacitor with good frequency characteristics is needed. Set it as close to the circuit as possible, with wires as short as possible.

The value of the output capacitance has to be at least $47 \mu\text{F}$ connected from V_{OUT} to GND. When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

ON/OFF

The regulator is fully enabled when a logic HIGH is applied to this input. The regulator enters shutdown when a logic LOW is applied to this input. During shutdown, regulator output voltage falls to zero, RESET remains valid and supply current is reduced to $5 \mu\text{A}$ (typ). If the function is not to be used, the ON/OFF pin should be tied to V_{IN} .

RESET output

The SA57066 has an Active-LOW RESET output. The RESET output is driven Active-LOW within $30 \mu\text{s}$ typical (when C_d is zero capacitance). The time delay can be adjusted up to 10ms typical (when C_d is $0.1 \mu\text{F}$) of V_{DET} falling through the reset voltage threshold. RESET is maintained Active-HIGH after V_{DET} rises above the reset threshold.

RESET output delay operation with an external capacitor from Cd pin to GND

When the supply voltage crosses the release voltage (V_{DET}) from a low value to a value higher than the released voltage (V_{DET}), the Cd pin voltage starts to increase (charges up the external capacitor). While the RESET output remains at LOW state condition until the Cd pin voltage reaches the threshold operating voltage (V_{OPL}) 0.4V typical; after that, the RESET output is reversed to HIGH state condition.

The transmission delay time (t_{PLH}) can be set with the capacitance Cd of an external capacitor as shown in Equation (1):

$$t_{\text{PLH}} = 10^6 \times C \tag{Eqn. (1)}$$

(Time is expressed in seconds; capacitance in Farads.)

PCB layout

The component placement around the LDO should be done carefully to achieve good dynamic line and load response. The input and noise capacitors should be kept close to the LDO.

The rise in junction temperature depends on how efficiently the heat is carried away from the junction to ambient. The junction to lead thermal impedance is a characteristic of the package and fixed. The thermal impedance between lead to ambient can be reduced by increasing the copper area on the PCB. Increase the input, output and ground trace area to reduce the junction-to-ambient impedance.

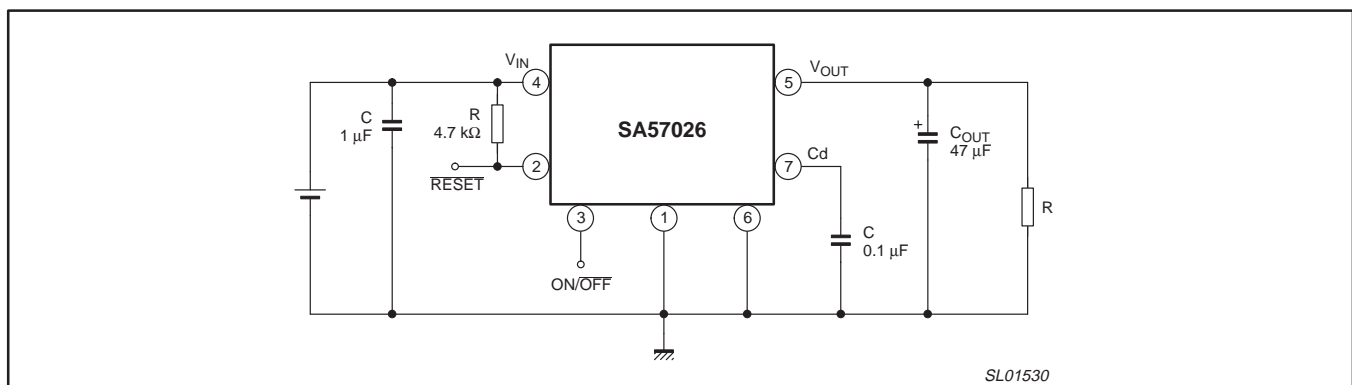


Figure 3. Typical application circuit.

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PACKING METHOD

The SA57026 is packed in reels, as shown in Figure 4.

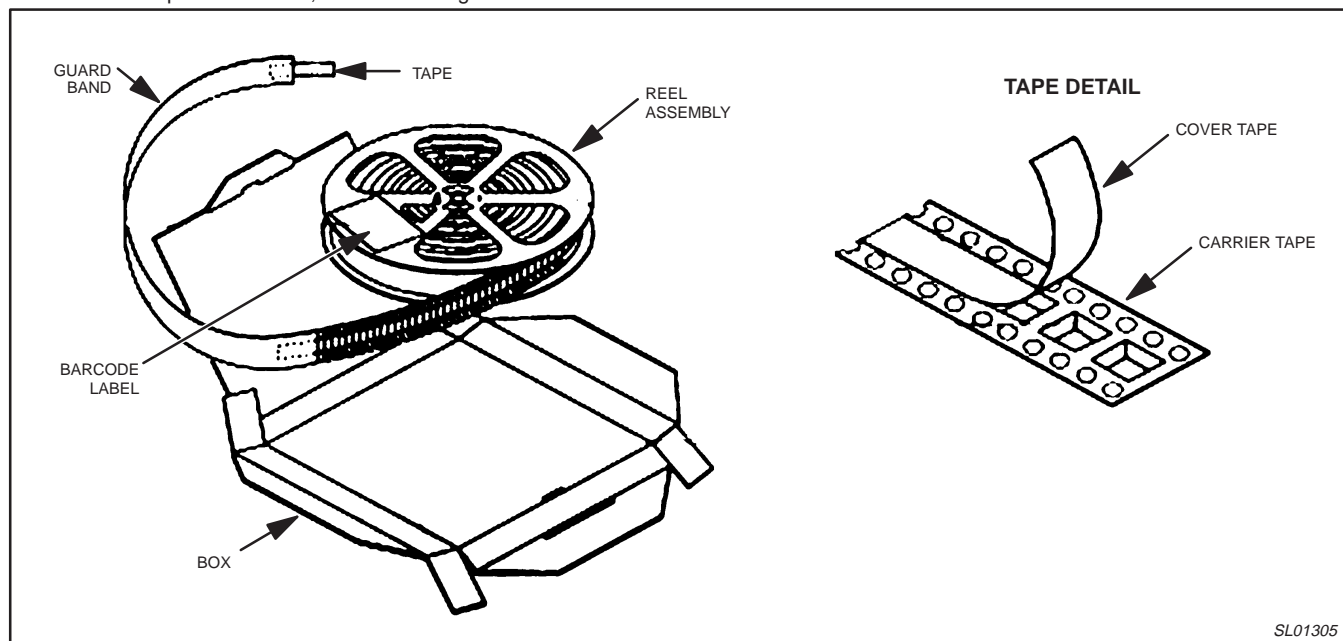


Figure 4. Tape and reel packing method

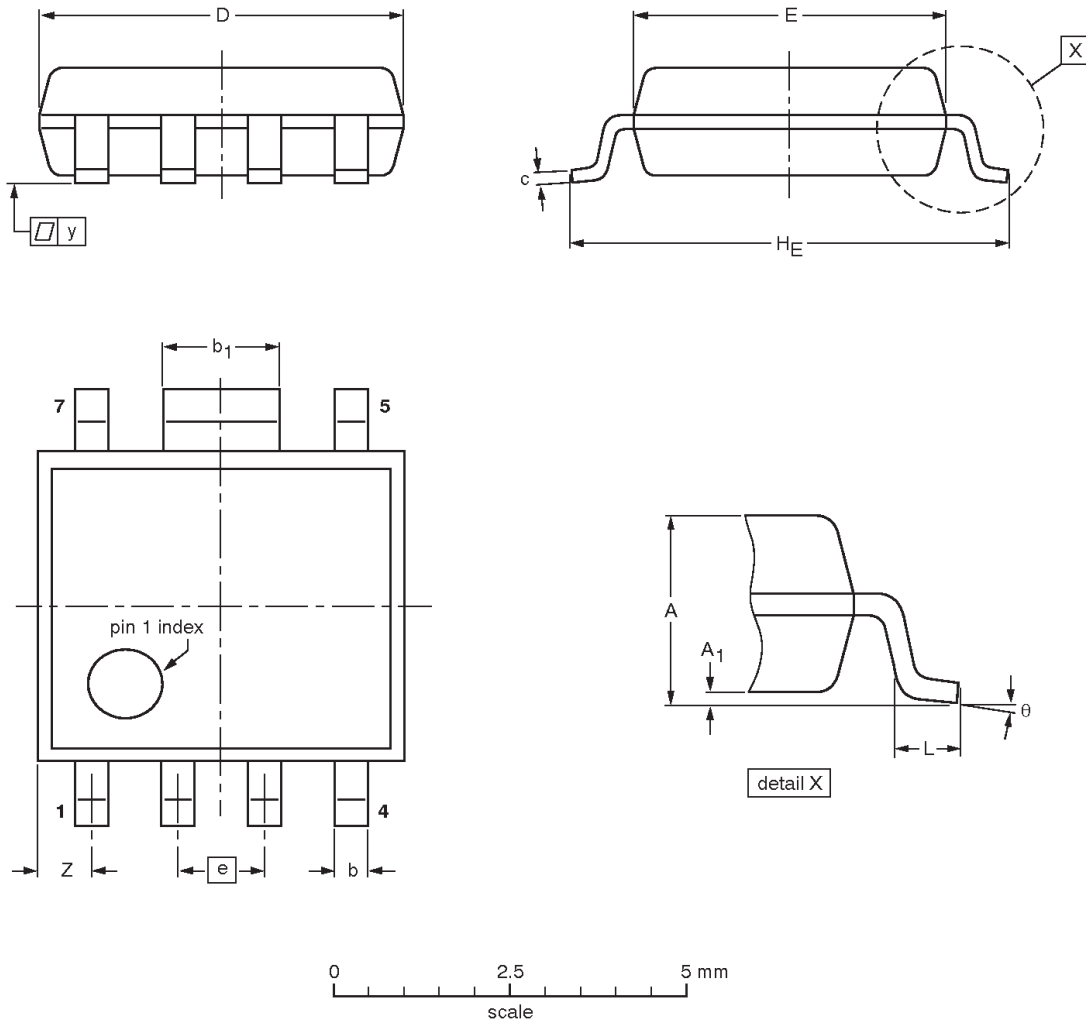
SL01305

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Plastic small outline package; 7 leads; body width 4.4 mm

SOP002



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	b	b ₁	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	y	Z max.	θ
mm	1.7	0.1 0.0	0.5 0.3	1.87 1.47	0.25 0.10	5.3 4.7	4.6 4.2	1.27	6.5 5.9	0.6 0.2	0.1	0.895	10° 0°
inches	0.067	0.004 0.0	0.02 0.012	0.074 0.058	0.010 0.006	0.208 0.185	0.181 0.173	0.05	0.256 0.232	0.024 0.008	0.004	0.035	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOP002						03-06-23 03-10-07

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REVISION HISTORY

Rev	Date	Description
_2	20031013	Product data (9397 750 12113). ECN 853-2292 30327 of 09 September 2003. Modifications: <ul style="list-style-type: none"> Change package name from SOP-7B to SOP002 in Ordering information and Package outline sections.
_1	20011003	Product data (9397 750 08968). ECN 853-2292 27197 of 03 October 2001.

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Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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