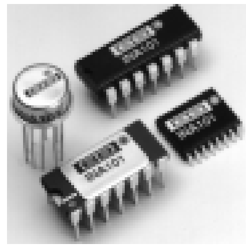
BURR - BROWN ®



INA101

High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW DRIFT: 0.25μV/°C max
- LOW OFFSET VOLTAGE: 25μV max
- LOW NONLINEARITY: 0.002%
- LOW NOISE: 13nV/√Hz
- HIGH CMR: 106dB AT 60Hz
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- 14-PIN PLASTIC, CERAMIC DIP, SOL-16, AND TO-100 PACKAGES

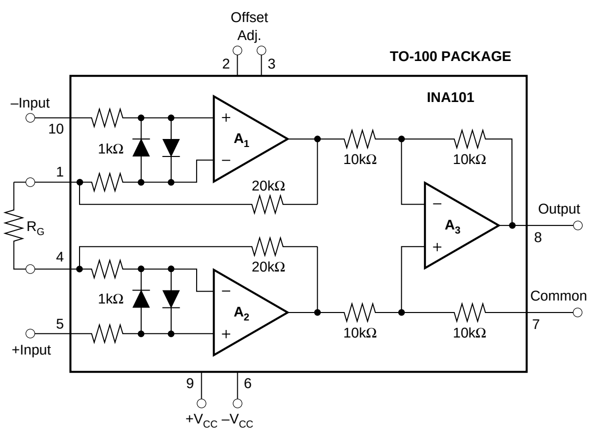
APPLICATIONS

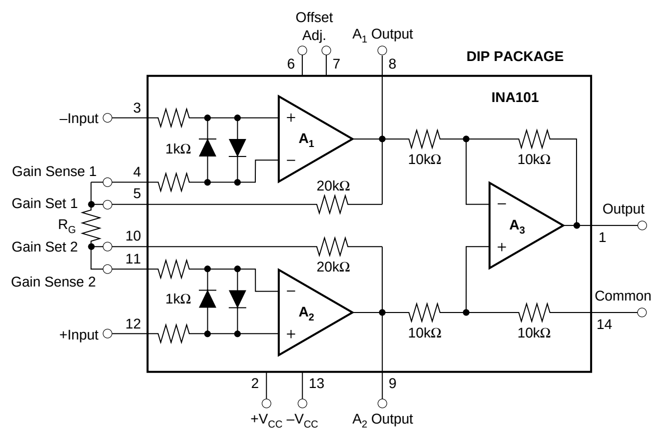
- STRAIN GAGES
- THERMOCOUPLES
- RTDs
- REMOTE TRANSDUCERS
- LOW-LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The INA101 is a high accuracy instrumentation amplifier designed for low-level signal amplification and general purpose data acquisition. Three precision op amps and laser-trimmed metal film resistors are integrated on a single monolithic integrated circuit.

The INA101 is packaged in TO-100 metal, 14-pin plastic and ceramic DIP, and SOL-16 surface-mount packages. Commercial, industrial and military temperature range models are available.





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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

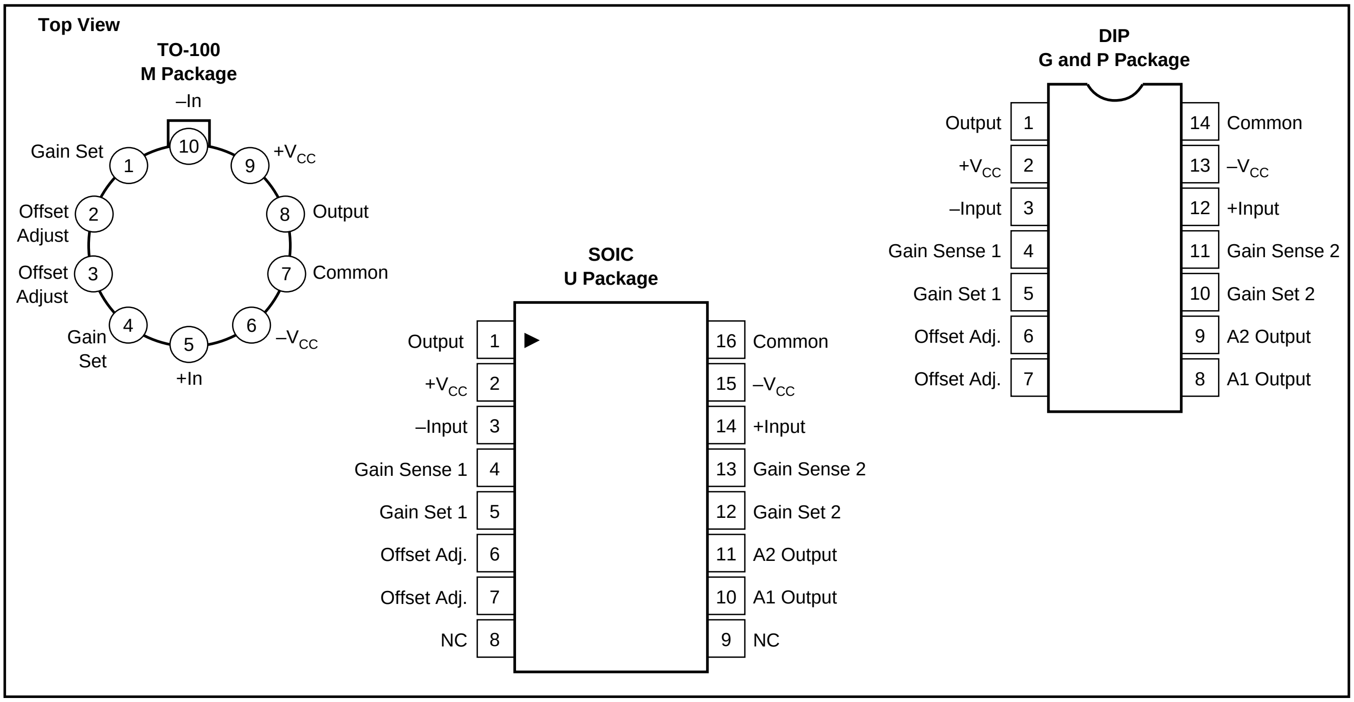
At +25°C with ±15VDC power supply and in circuit of Figure 1, unless otherwise noted.

	INA101AM, AG			INA101SM, SG			INA101CM, CG			INA101HP, KU			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN													
Range of Gain	1		1000	*		*	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*			*		V/V
Error from Equation, DC(1)		±(0.04 + 0.00016G –0.02/G)	±(0.1 + 0.0003G –0.05/G)		*	*		*	*		±(0.1 + 0.00015G) –0.05/G	±(0.3 + 0.0002G) –0.10/G	%
Gain Temp. Coefficient(3)													
G = 1		2	5		*	*		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	*		*	*	ppm/°C
G = 100		22	110		*	*		11	*		*	*	ppm/°C
G = 1000		22	110		*	*		11	*		*	*	ppm/°C
Nonlinearity, DC(2)		±(0.002 + 10^{-5} G)	±(0.005 + 2 x 10^{-5} G)		±(0.001 +10^{-5} G)	±(0.002 +10^{-5} G)		±(0.001 +10^{-5} G)	±(0.002 +10^{-5} G)		*	*	% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		*	*		*	*		*	*		V
Current	±5	±10		*	*		*	*		*	*		mA
Output Impedance		0.2			*			*			*		Ω
Capacitive Load		1000			*			*			*		pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		±(25 + 200/G)	±(50 + 400/G)		±10+ 100/G)	±(25 +200/G)		±(10+ 100/G)	±(25 + 200/G)		±(125 + 450/G)	±(250 + 900/G)	μV
vs Temperature			±(2 + 20/G)			±(0.75 + 10/G)			±(0.25 + 10/G)		±(2 + 20/G)		μV/°C
vs Supply		±(1 + 20/G)			*			*			*		μV/V
vs Time		±(1 + 20/G)			*			*			*		μV/mo
INPUT BIAS CURRENT													
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.2			*			*			*		nA/°C
vs Supply		±0.1			*			*			*		nA/V
Initial Offset Current		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.5			*			*			*		nA/°C
INPUT IMPEDANCE													
Differential		10^{10} || 3			*			*			*		Ω || pF
Common-mode		10^{10} || 3			*			*			*		Ω || pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		*	*		*	*		*	*		V
CMR with 1kΩ Source Imbalance													
DC to 60Hz, G = 1	80	90		*	*		*	*		65	85		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		90	95		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		100	105		dB
INPUT NOISE													
Input Voltage Noise													
f_B = 0.01Hz to 10Hz		0.8			*			*			*		μV, p-p
Density, G = 1000													
f_O = 10Hz		18			*			*			*		nV/√Hz
f_O = 100Hz		15			*			*			*		nV/√Hz
f_O = 1kHz		13			*			*			*		nV/√Hz
Input Current Noise													
f_B = 0.01Hz to 10Hz		50			*			*			*		pA, p-p
Density													
f_O = 10Hz		0.8			*			*			*		pA/√Hz
f_O = 100Hz		0.46			*			*			*		pA/√Hz
f_O = 1kHz		0.35			*			*			*		pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness													
G = 1		300			*			*			*		kHz
G = 10		140			*			*			*		kHz
G = 100		25			*			*			*		kHz
G = 1000		2.5			*			*			*		kHz
Small Signal, ±1% Flatness													
G = 1		20			*			*			*		kHz
G = 10		10			*			*			*		kHz
G = 100		1			*			*			*		kHz
G = 1000		200			*			*			*		Hz
Full Power, G = 1 to 100		6.4			*			*			*		kHz
Slew Rate, G = 1 to 100	0.2	0.4		*	*		*	*		*	*		V/μs
Settling Time (0.1%)													
G = 1		30	40		*	*		*	*		*	*	μs
G = 100		40	55		*	*		*	*		*	*	μs
G = 1000		350	470		*	*		*	*		*	*	μs
Settling Time (0.01%)													
G = 1		30	45		*	*		*	*		*	*	μs
G = 100		50	70		*	*		*	*		*	*	μs
G = 1000		500	650		*	*		*	*		*	*	μs
POWER SUPPLY													
Rated Voltage		±15			*			*			*		V
Voltage Range	±5		±20	*		*	*		*	*		*	V
Current, Quiescent(2)		±6.7	±8.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE(5)													
Specification	–25		+85	–55		+125	*		*	0		+70	°C
Operation	–55		+125	*		*	*		*	–25		+85	°C
Storage	–65		+150	*		*	*		*	–40		+85	°C

* Specifications same as for INA101AM, AG.

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G. (4) Adjustable to zero at any one gain. (5) θ_{JC} output stage = 113°C/W, θ_{JC} quiescent circuitry = 19°C/W, θ_{CA} = 83°C/W.

PIN CONFIGURATIONS



ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
INA101AM	10-Pin Metal TO-100	–25°C to +85°C
INA101CM	10-Pin Metal TO-100	–25°C to +85°C
INA101AG	14-Pin Ceramic DIP	–25°C to +85°C
INA101CG	14-Pin Ceramic DIP	–25°C to +85°C
INA101HP	14-Pin Plastic DIP	0°C to +70°C
INA101KU	SOL-16 Surface-Mount	0°C to +70°C
INA101SG	14-Pin Ceramic DIP	–55°C to +125°C
INA101SM	10-Pin Metal TO-100	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Power Dissipation	600mW
Input Voltage Range	±V_{CC}
Output Short Circuit (to ground)	Continuous
Operating Temperature M, G Package	–55°C to +125°C
P, U Package	–25°C to +85°C
Storage Temperature M, G Package	–65°C to +150°C
P, U Package	–40°C to +85°C
Lead Temperature (soldering, 10s) M, G, P Package	+300°C
Lead Temperature (wave soldering, 3s) U Package	+260°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA101AM	10-Pin Metal TO-100	007
INA101CM	10-Pin Metal TO-100	007
INA101AG	14-Pin Ceramic DIP	169
INA101CG	14-Pin Ceramic DIP	169
INA101HP	14-Pin Plastic DIP	010
INA101KU	SOL-16 Surface-Mount	211
INA101SG	14-Pin Ceramic DIP	169
INA101SM	10-Pin Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

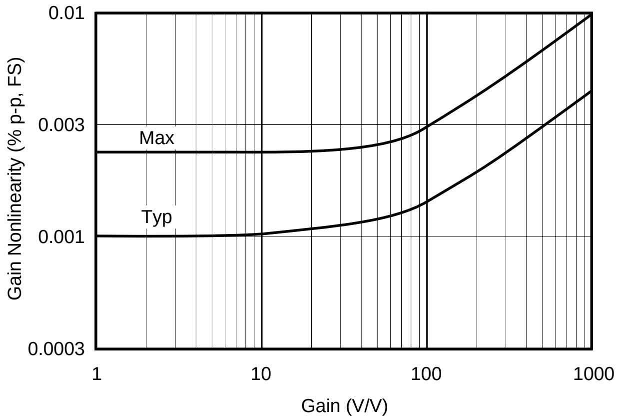
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

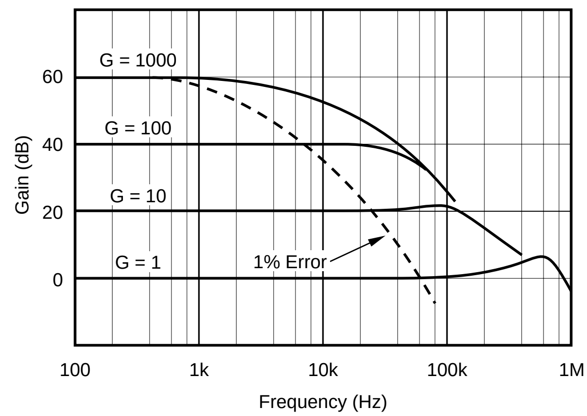
TYPICAL PERFORMANCE CURVES

At +25°C, V_{CC} = ±15V unless otherwise noted.

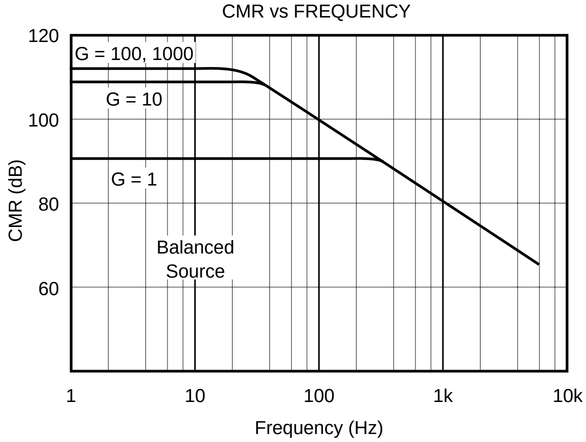
GAIN NONLINEARITY vs GAIN



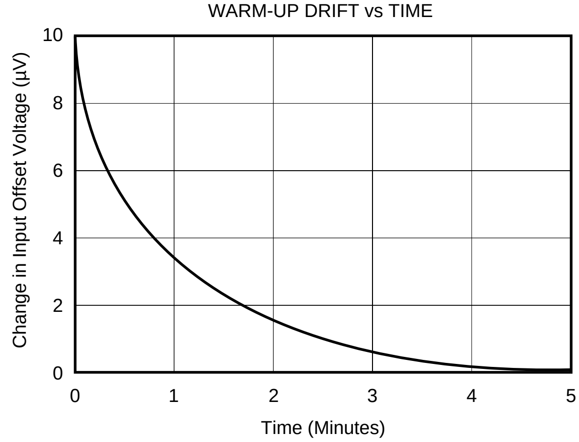
GAIN vs FREQUENCY



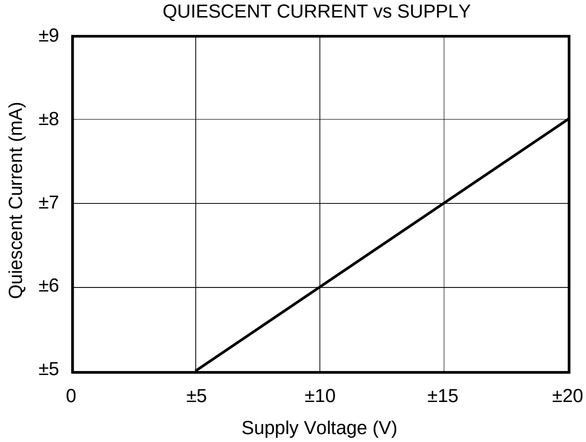
CMR vs FREQUENCY



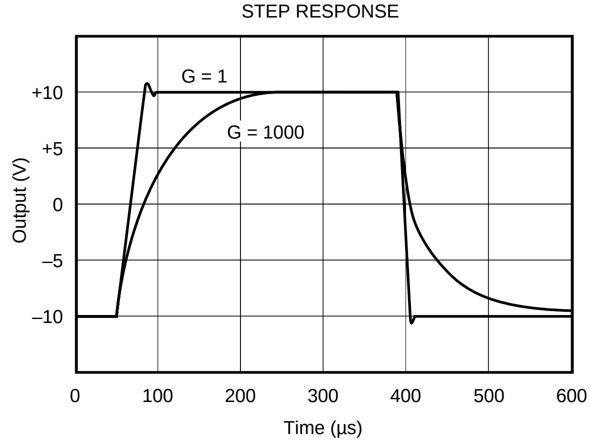
WARM-UP DRIFT vs TIME



QUIESCENT CURRENT vs SUPPLY



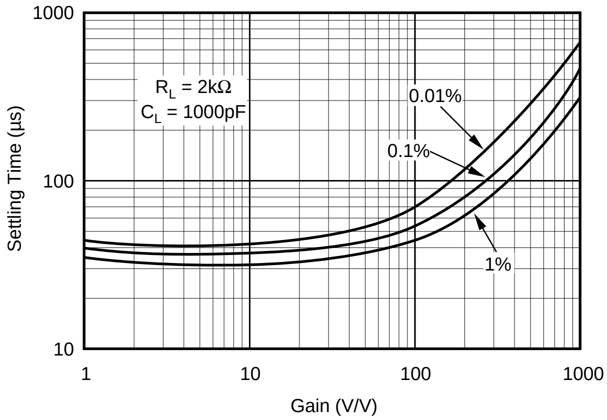
STEP RESPONSE



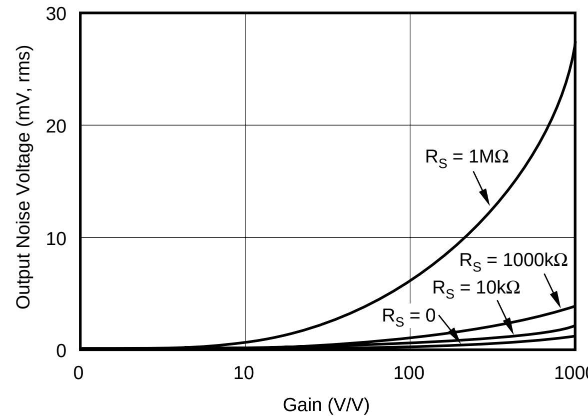
TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, V_{CC} = ±15V unless otherwise noted.

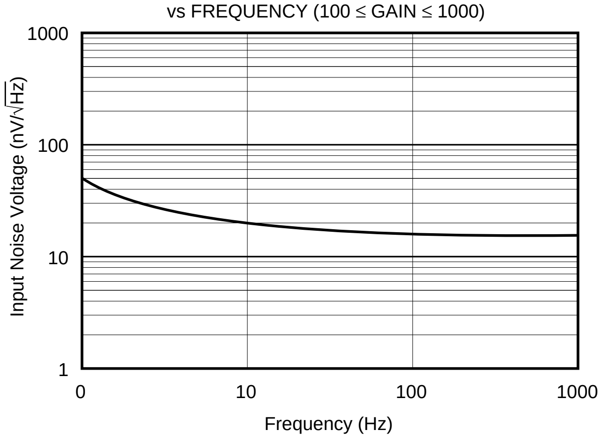
SETTLING TIME vs GAIN



OUTPUT NOISE vs GAIN



INPUT NOISE VOLTAGE
vs FREQUENCY (100 ≤ GAIN ≤ 1000)



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA101. (Pin numbers shown are for the TO-100 metal package.) Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output Common terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance greater than 0.1Ω in series with the Common pin will cause common-mode rejection to fall below 106dB.

SETTING THE GAIN

Gain of the INA101 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{40k\Omega}{R_G} \quad (1)$$

The 40kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA101.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. The gain sense connections on the DIP and SOL-16 packages (see Figure 2) reduce the gain error produced by wiring or socket resistance.

OFFSET TRIMMING

The INA101 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows connection of an optional potentiometer connected to the Offset Adjust pins for trimming the input offset voltage. (Pin numbers shown are for the DIP package.) Use this adjustment to null the offset voltage in high gain (G ≥ 100) with both inputs connected to ground. Do not use this adjustment to null offset produced by the source or other system offset since this will increase the offset voltage drift by 0.3µV/°C per 100µV of adjusted offset.

Offset of the output amplifier usually dominates when the INA101 is used in unity gain (G = 1). The output offset voltage can be adjusted with the optional trim circuit connected to the Common pin as shown in Figure 2. The voltage applied to Common terminal is summed with the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp connected as a buffer provides low impedance.

THERMAL EFFECTS ON OFFSET VOLTAGE

To achieve lowest offset voltage and drift, prevent air currents from circulating near the INA101. Rapid changes in temperature will produce a thermocouple effect on the package leads that will degrade offset voltage and drift. A shield or cover that prevents air currents from flowing near the INA101 will assure best performance.

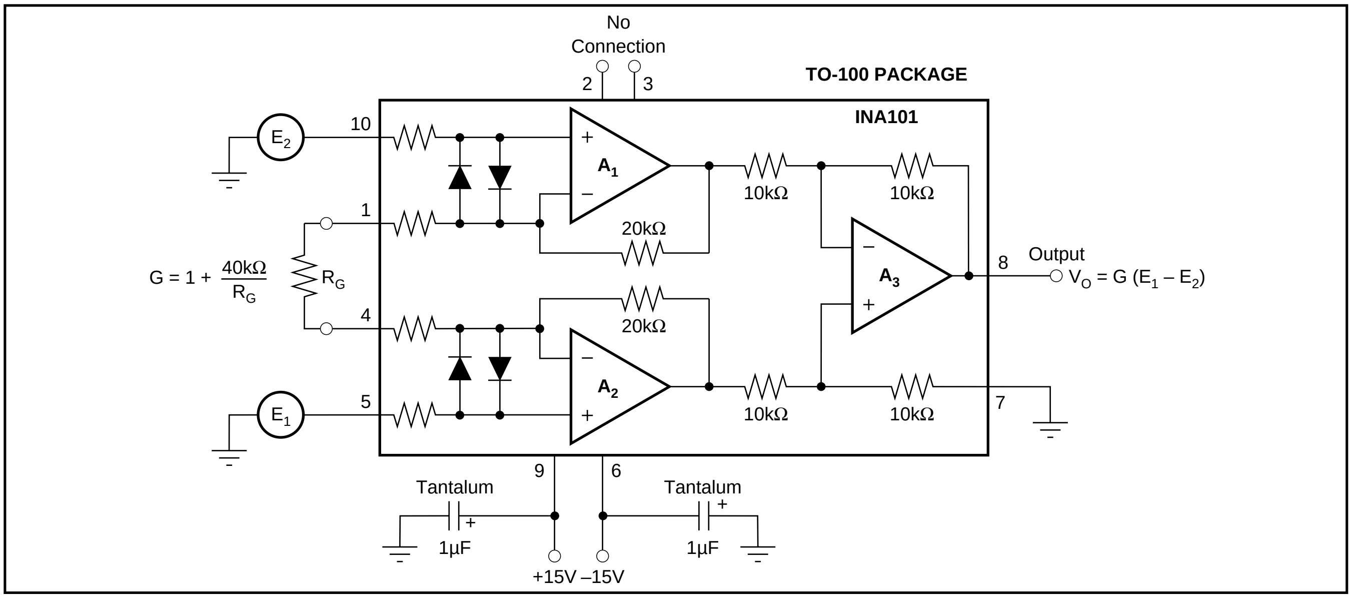


FIGURE 1. Basic Connections.

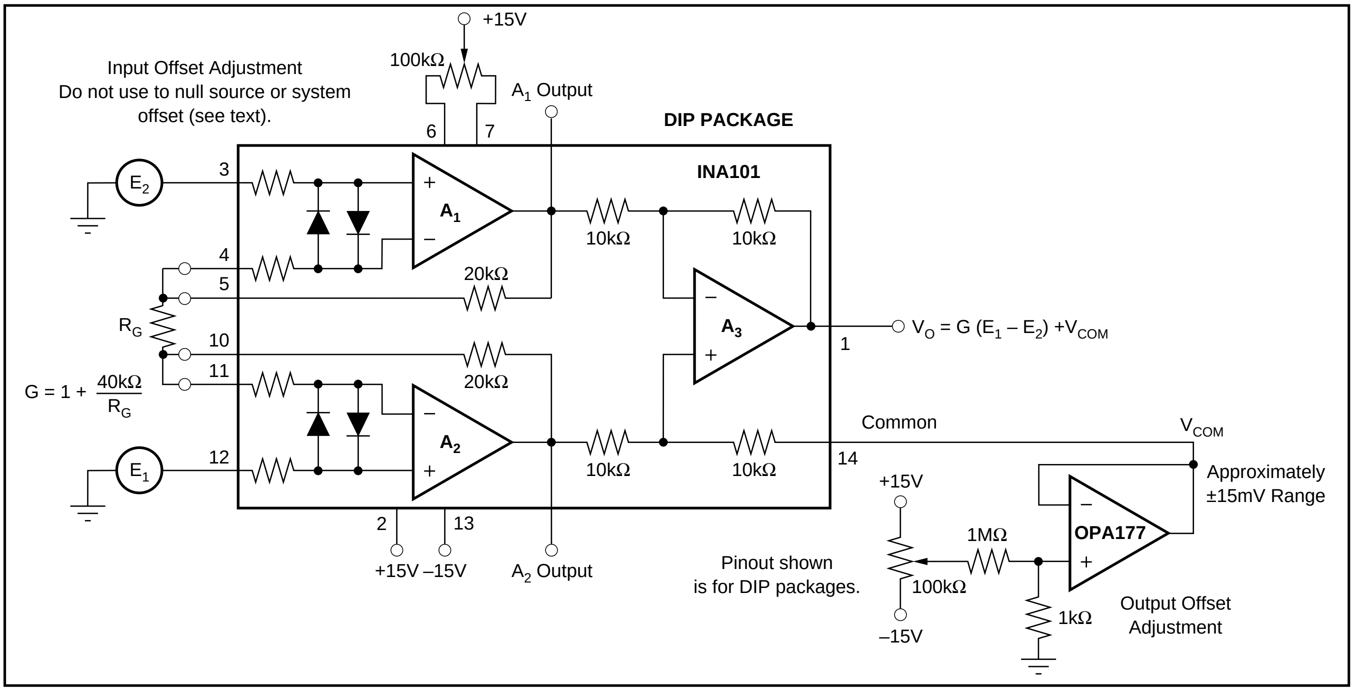


FIGURE 2. Optional Trimming of Input and Output Offset Voltage.