HA5340/883

High Speed, Low Distortion, Precision Monolithic Sample and Hold Amplifier

June 1994

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Acquisition Time (0.01%) 900ns**
- **Fast Hold Mode Settling Time (0.01%) 300ns**
- **Low Distortion (Hold Mode) . . . . . -72dBc (Typ) (V_{IN} = 200kHz, Fs = 450kHz, $5V_{P-P}$)**
- **Bandwidth Minimally Affected By External C_H**
- **Fully Differential Analog Inputs**
- **Built-in 135pF Hold Capacitor**
- **Pin Compatible with HA-5320**

Applications

- **High Bandwidth Precision Data Acquisition Systems**
- **Inertial Navigation and Guidance Systems**
- **Ultrasonics**
- **SONAR**
- **RADAR**

Description

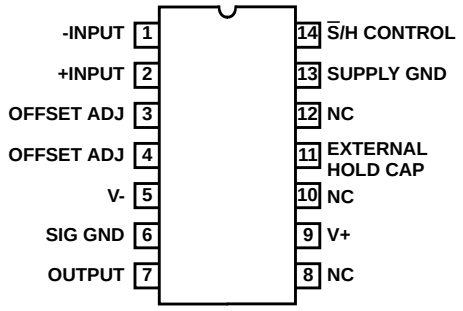
The HA-5340/883 combines the advantages of two sample/hold architectures to create a new generation of monolithic sample/hold. High amplitude, high frequency signals can be sampled with very low distortion being introduced. The combination of exceptionally fast acquisition time and specified/characterized hold mode distortion is an industry first. Additionally, the AC performance is only minimally affected by additional hold capacitance.

To achieve this level of performance, the benefits of an integrating output stage have been combined with the advantages of a buffered hold capacitor. To the user this translates to a front-end stage that has high bandwidth due to charging only a small capacitive load and an output stage with constant pedestal error which can be nulled out using the offset adjust pins. Since the performance penalty for additional hold capacitance is low, the designer can further minimize pedestal error and droop rate without sacrificing speed.

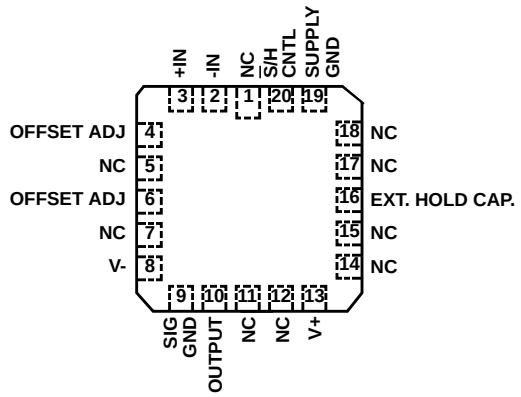
Low distortion, fast acquisition, and low droop rate are the result, making the HA-5340/883 the obvious choice for high speed, high accuracy sampling systems.

Pinouts

HA-5340/883 (CERDIP)
TOP VIEW



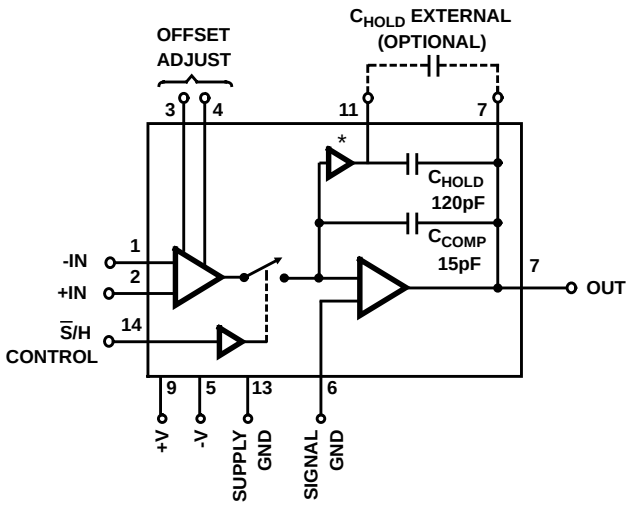
HA-5340/883 (CLCC)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5340/883	-55°C to +125°C	14 Lead CerDIP
HA4-5340/883	-55°C to +125°C	20 Lead Ceramic LCC

Functional Diagram



NOTE: Buffer acts as a buffer in sample mode, acts as a closed switch in hold mode.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage 24V
Digital Input Voltage (S/H Pin) . . . . . +8V, -6V
Output Current, Continuous . . . . . ±20mA
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$
ESD Classification . . . . . <2000V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	$68^oC/W$	$17^oC/W$
Ceramic LCC Package	$68^oC/W$	$18^oC/W$

Package Power Dissipation at $+75^oC$
CerDip Package 1.5W
Ceramic LCC Package 1.5W
Package Power Dissipation Derating Factor Above $+75^oC$
CerDip Package . . . . . $15mW/^oC$
Ceramic LCC Package . . . . . $15mW/^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . $-55^oC \le T_A \le +125^oC$
Operating Supply Voltage ($\pm V_S$) . . . . . ±15V
Analog Input Voltage . . . . . ±10V
Logic Level Low (V_{IL}) . . . . . 0V to 0.8V
Logic Level High (V_{IH}) . . . . . 2.0V to 5.0V

TABLE 1. DC ELECTICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = Internal = 135pF; Signal GND = Supply GND, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}		1	$+25^oC$	-1.5	1.5	mV
			2, 3	$+125^oC$, -55^oC	-3	3	mV
Input Bias Current	$+I_B$		1	$+25^oC$	-350	350	nA
			2, 3	$+125^oC$, -55^oC	-350	350	nA
	$-I_B$		1	$+25^oC$	-350	350	nA
			2, 3	$+125^oC$, -55^oC	-350	350	nA
Input Offset Current	I_{IO}		1	$+25^oC$	-350	350	nA
			2, 3	$+125^oC$, -55^oC	-350	350	nA
Open Loop Voltage Gain	$+A_{VS}$	R_L = 2kΩ, C_L = 60pF, V_{OUT} = +10V	1	$+25^oC$	110	-	dB
			2, 3	$+125^oC$, -55^oC	100	-	dB
	$-A_{VS}$	R_L = 2kΩ, C_L = 60pF, V_{OUT} = -10V	1	$+25^oC$	110	-	dB
			2, 3	$+125^oC$, -55^oC	100	-	dB
Common Mode Rejection Ratio	+CMRR	V+ = 5V, V- = -25V, V_{OUT} = -10V, $V_{\overline{S}/H}$ = -9.2V	1	$+25^oC$	72	-	dB
			2, 3	$+125^oC$, -55^oC	72	-	dB
	-CMRR	V+ = 25V, V- = -5V, V_{OUT} = +10V, $V_{\overline{S}/H}$ = 10.8V	1	$+25^oC$	72	-	dB
			2, 3	$+125^oC$, -55^oC	72	-	dB
Output Current	$+I_O$	V_{OUT} = +10V	1	$+25^oC$	10	-	mA
			2, 3	$+125^oC$, -55^oC	10	-	mA
	$-I_O$	V_{OUT} = -10V	1	$+25^oC$	-10	-	mA
			2, 3	$+125^oC$, -55^oC	-10	-	mA
Output Voltage Swing	$+V_{OP}$	R_L = 2kΩ, C_L = 60pF	1	$+25^oC$	10	-	V
			2, 3	$+125^oC$, -55^oC	10	-	V
	$-V_{OP}$	R_L = 2kΩ, C_L = 60pF	1	$+25^oC$	-	-10	V
			2, 3	$+125^oC$, -55^oC	-	-10	V

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Spec Number **511117-883**

TABLE 1. DC ELECTICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = Internal = 135pF; Signal GND = Supply GND, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Power Supply Current	$+I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-	25	mA
			2, 3	+125°C, -55°C	-	25	mA
	$-I_{CC}$	V_{OUT} = 0V, I_{OUT} = 0mA	1	+25°C	-25	-	mA
			2, 3	+125°C, -55°C	-25	-	mA
Power Supply Rejection Ratio	+PSRR	V+ = 13.5V, 16.5V V- = -15V, -15V	1	+25°C	75	-	dB
			2, 3	+125°C, -55°C	75	-	dB
	-PSRR	V+ = +15V, +15V, V- = -13.5V, -16.5V	1	+25°C	75	-	dB
			2, 3	+125°C, -55°C	75	-	dB
Digital Input Current	I_{INL}	V_{IN} = 0V	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	40	µA
	I_{INH}	V_{IN} = 5V	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	40	µA
Digital Input Voltage	V_{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
	V_{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Output Voltage Droop Rate	V_D	V_{OUT} = 0V	2	+125°C	-	95	µV/µs

TABLE 2. AC ELECTICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = Internal = 135pF; - Input Tied to Output, Signal GND = Supply GND, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Hold Step Error	V_{ERROR}	V_{IL} = 0V, V_{IH} = 4.0V, $t_{RISE}(V_{S/H})$ = 15ns	4	+25°C	-50	50	mV
Rise Time & Fall Time	T_R	C_L=60pF, R_L=2kΩ, A_V = +1, V_{OUT} = 0V to +200mV Step 10%, 90%pts	4	+25°C	-	50	ns
			5, 6	+125°C, -55°C	-	50	ns
	T_F	C_L = 60pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 0V to -200mV Step 10%, 90%pts	4	+25°C	-	50	ns
Overshoot	+OS	C_L = 60pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 0V to +200mV Step	4	+25°C	-	60	%
			5, 6	+125°C, -55°C	-	60	%
	-OS	C_L = 60pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 0V to -200mV Step	4	+25°C	-	60	%
			5, 6	+125°C, -55°C	-	60	%
Slew Rate	+SR	C_L = 60pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 0V to +10V Step, 25%, 75% pts	4	+25°C	40	-	V/µs
			5, 6	+125°C, -55°C	40	-	V/µs
	-SR	C_L = 60pF, R_L = 2kΩ, A_V = +1, V_{OUT} = 0V to -10V Step, 25%, 75% pts	4	+25°C	40	-	V/µs
			5, 6	+125°C, -55°C	40	-	V/µs

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Hold Mode Feedthrough	V_{HMF}	V_{IN} = 20V_{P-P}, 200kHz	1	+25°C	-	-70	dB
Sample Mode Noise Voltage	$E_{n(SAMPLE)}$	DC to 10MHz, $V_{S/H}$ = 0V, R_{LOAD} = 2K	1	+25°C	-	335	μV_{RMS}
Hold Mode Noise Voltage	$E_{n(HOLD)}$	DC to 10MHz, $V_{S/H}$ = 5V, R_{LOAD} = 2K	1	+25°C	-	100	μV_{RMS}
Input Capacitance	C_{IN}	$V_{S/H}$ = 0V	1	+25°C	-	5	pF
Input Resistance	R_{IN}	$V_{S/H}$ = 0V, Delta V_{IN} = 20V	1	+25°C	1	-	MΩ
0.1% Acquisition Time	T_{ACQ} 0.1%	C_L = 60pF, R_L = 2K, V_{OUT} = 0V to 10V Step	1	+25°C	-	600	ns
Total Harmonic Distortion Hold Mode	$THD_{200K(HOLD)}$	F_S = 450kHz, V_{IN} = 20V_{P-P}, 200kHz	1	+25°C	-	-50	dBc
	$THD_{500K(HOLD)}$	F_S = 450kHz, V_{IN} = 5V_{P-P}, 500kHz	1	+25°C	-	-47	dBc
Total Harmonic Distortion Sample Mode	$THD_{200K(SAMPLE)}$	V_{IN} = 20V_{P-P}, 200kHz	1	+25°C	-	-60	dBc
	$THD_{500K(SAMPLE)}$	V_{IN} = 5V_{P-P}, 500kHz	1	+25°C	-	-49	dBc

NOTE:

1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	-
Final Electrical Test Parameters	1(Note 1), 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Die Characteristics

DIE DIMENSIONS:
84 x 139 x 19mils

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

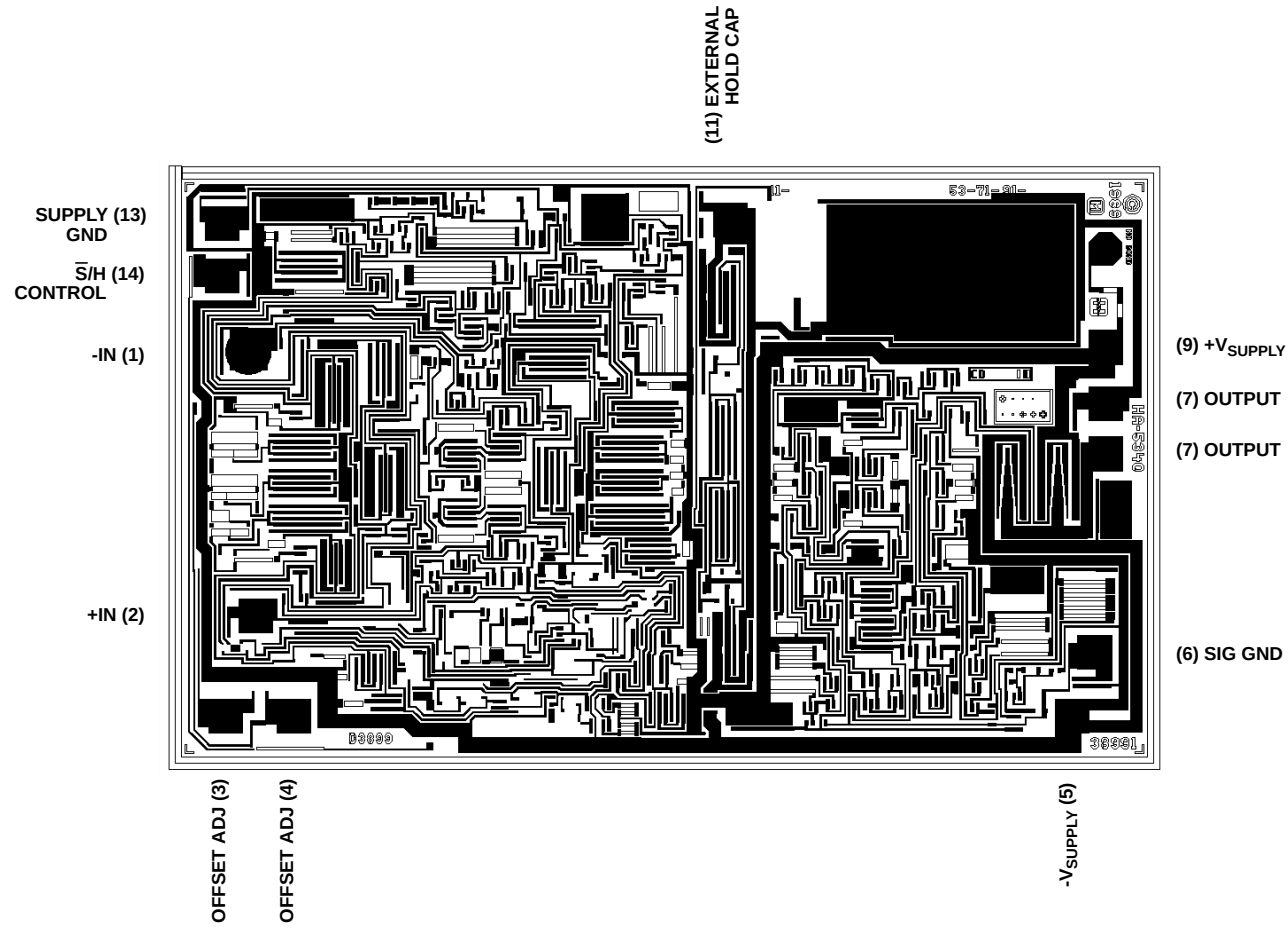
GLASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 2.0kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature:Ceramic DIP - 460°C (Max)
Ceramic LCC - 420°C (Max)

WORST CASE CURRENT DENSITY:
5.33 x 10^4 A/cm^2

Metallization Mask Layout

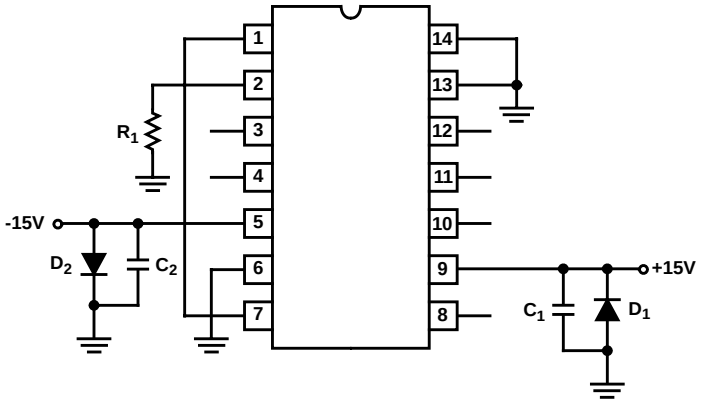
HA-5340/883



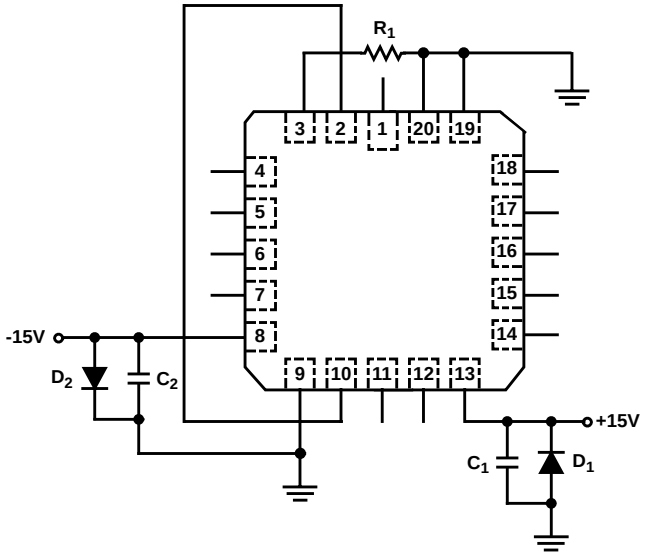
Spec Number **511117-883**

Burn-In Circuits

HA-5340/883 DIP BURN-IN/LIFE TEST CIRCUIT



HA-5340/883 LCC BURN-IN/LIFE TEST CIRCUIT

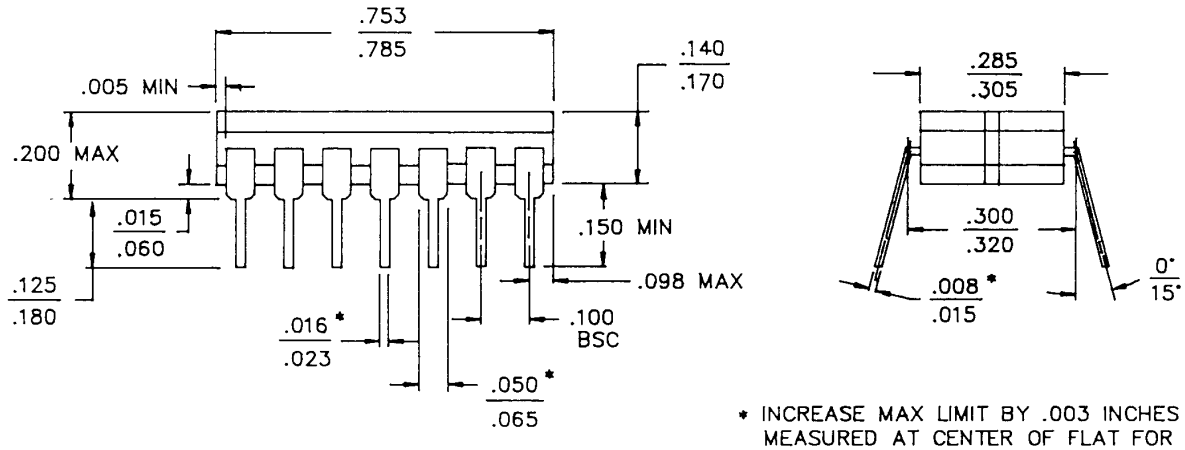


NOTES:

1. R_1 = 100kΩ, 5%, $^1/_4$W or $^1/_2$W (per socket).
2. C_1, C_2 = 0.01µF minimum per socket or 0.1µF minimum per row.
3. D_1, D_2 = 1N4002 or equivalent (per board).

Packaging†

14 PIN CERAMIC DIP

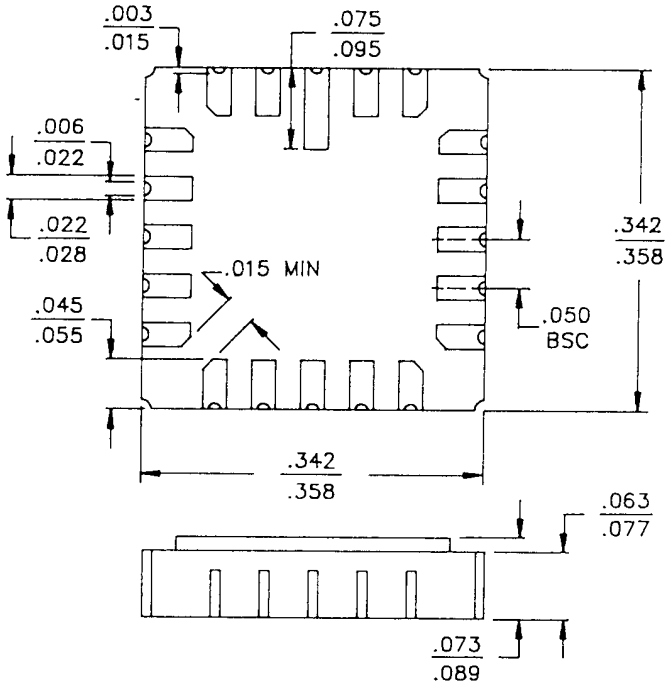


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: $450^{o}C \pm 10^{o}C$
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510-D-1

20 PIN CERAMIC LCC



LEAD MATERIAL: Type C
LEAD FINISH: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: $320^{o}C \pm 10^{o}C$
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510-C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$; Dimensions are in inches.

Spec Number **511117-883**

HARRIS Semiconductor

HA5340

DESIGN INFORMATION

August 1999

High Speed, Low Distortion, Precision Monolithic Sample and Hold Amplifier

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Applying the HA-5340

The HA-5340 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Intersil Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1µF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5340 includes a 135pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

The hold capacitor CH should have high insulation resistance and low dielectric absorption, to minimize droop errors. Teflon®, polystyrene and polypropylene dielectric capacitor types offer good performance over the specified operating temperature range.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and ‘‘guarded’’ by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Applications

Figure 1 shows the HA-5340 connected as a unity gain noninverting amplifier – its most widely used configuration. As an input device for a fast successive – approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5340’s hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The HA-5340 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

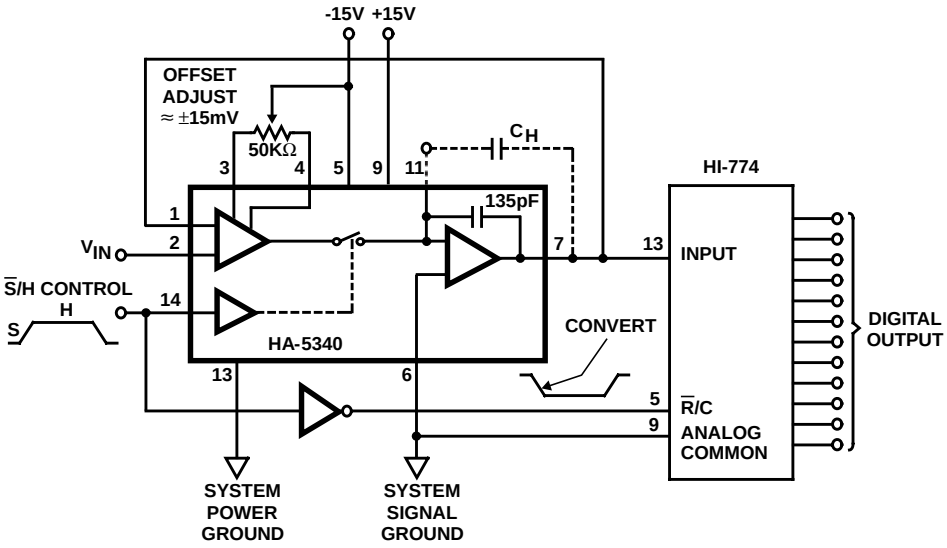

FIGURE 1. TYPICAL HA-5340 CONNECTIONS; NONINVERTING UNITY GAIN MODE

NOTE: Pin Numbers Refer to DIP Package Only.

Spec Number **511117-883**

DESIGN INFORMATION (Continued)

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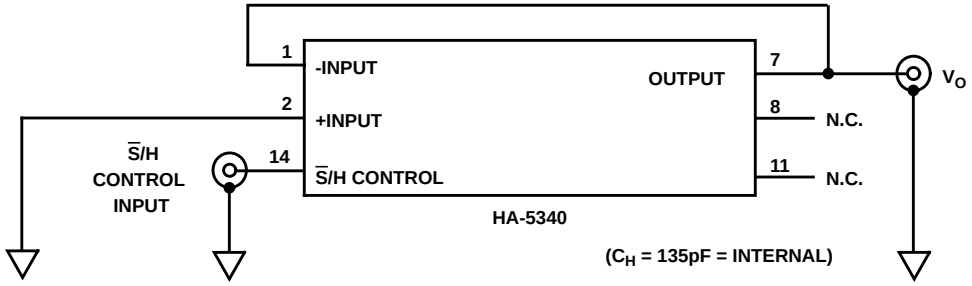
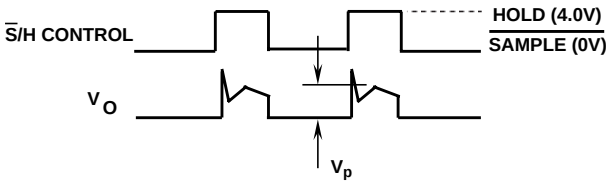
Test Circuits

HOLD STEP ERROR AND DROOP RATE



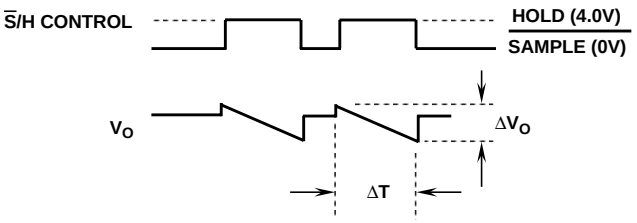
HOLD STEP ERROR

1. Observe the "hold step" voltage V_p:



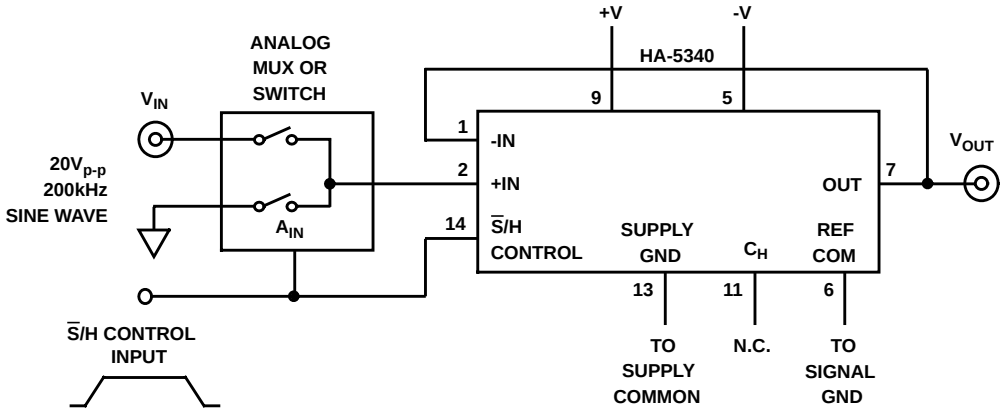
DROOP RATE TEST

1. Observe the voltage "droop", $\Delta V_O/\Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$.
3. Droop can be positive or negative - usually to one rail or the other not to GND.

HOLD MODE FEED THROUGH ATTENUATION



Feedthrough in dB = 20 Log $\frac{V_{OUT}}{V_{IN}}$ where:

V_{OUT} = Voltsp-p, Hold Mode,
V_{IN} = Voltsp-p.

DESIGN INFORMATION (Continued)

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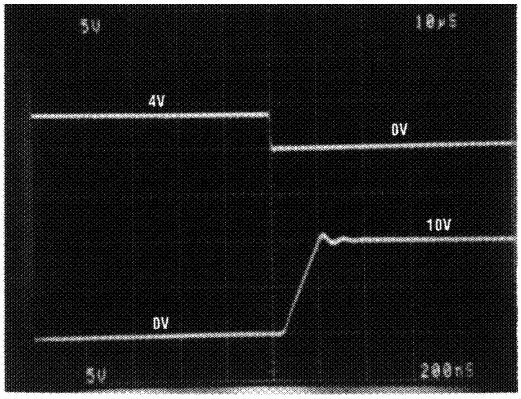
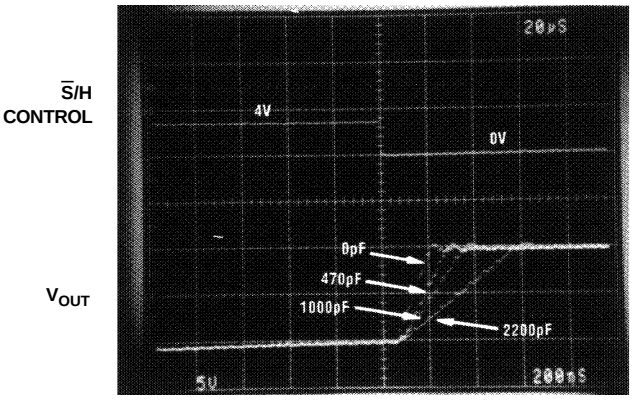
Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, Unless Otherwise Specified.

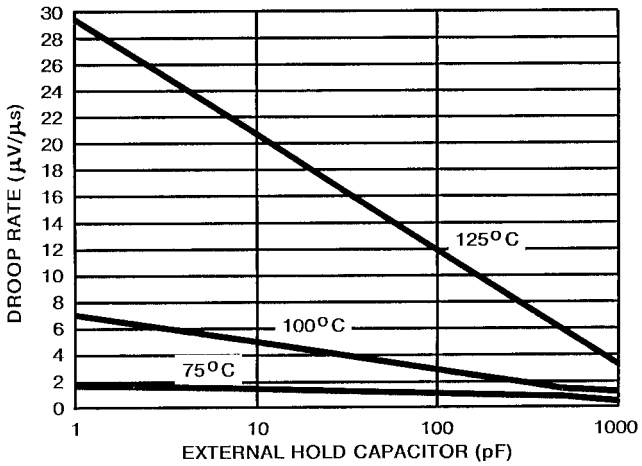
T_{ACQ} POS 0 TO +10 STEP



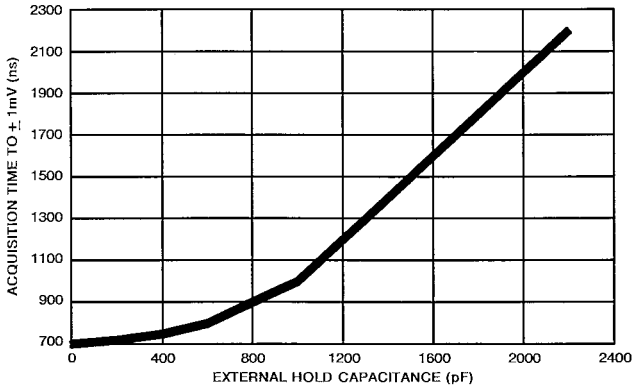
T_{ACQ} vs. ADDITIONAL C_H



DROOP RATE vs. HOLD CAPACITOR SIZE

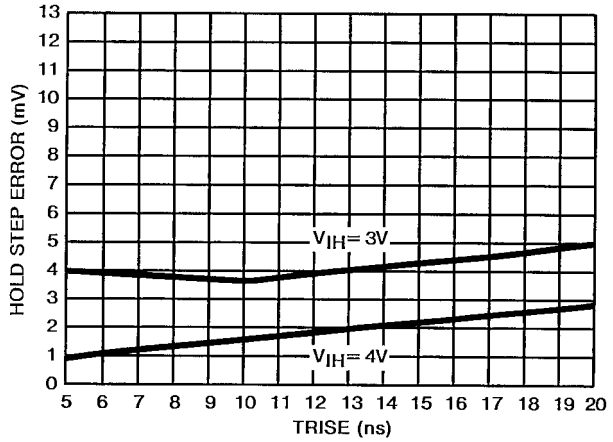


ACQUISITION TIME (0.01%) vs. HOLD CAPACITANCE



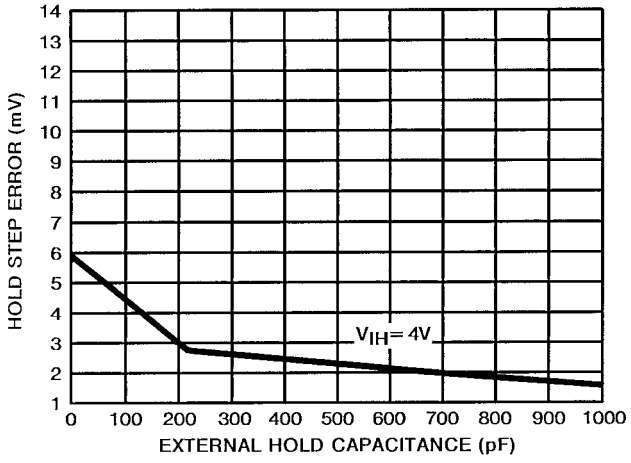
HOLD STEP ERROR vs. T_{RISE}

C_H = Internal; Temperature +25°C



HOLD STEP ERROR vs. HOLD CAPACITANCE

T_{RISE} = 5ns; Temperature = +25°C



DESIGN INFORMATION (Continued)

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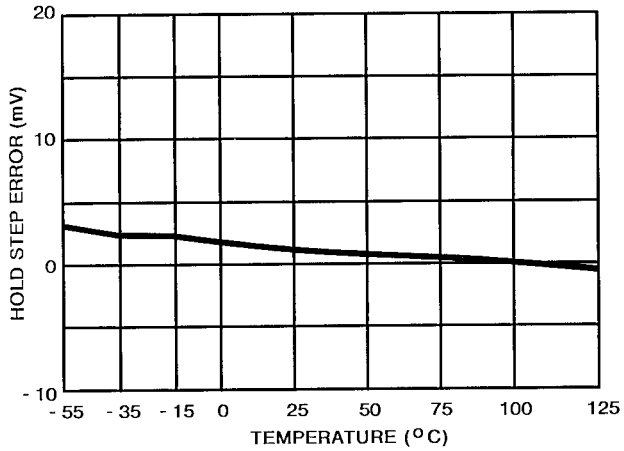
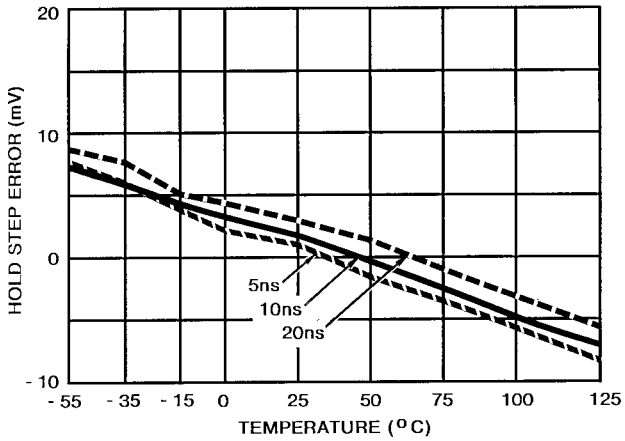
Performance Curves (Continued) $V_S = \pm15V$, $T_A = +25^oC$, Unless Otherwise Specified.

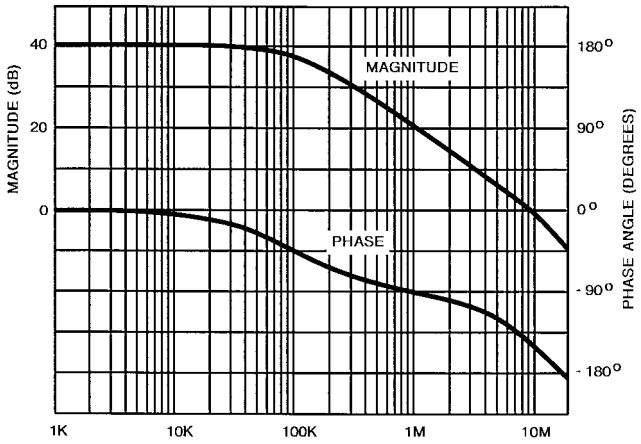
HOLD STEP ERROR vs. TEMPERATURE
$V_{IH} = 4V$, $C_H = 470pF$



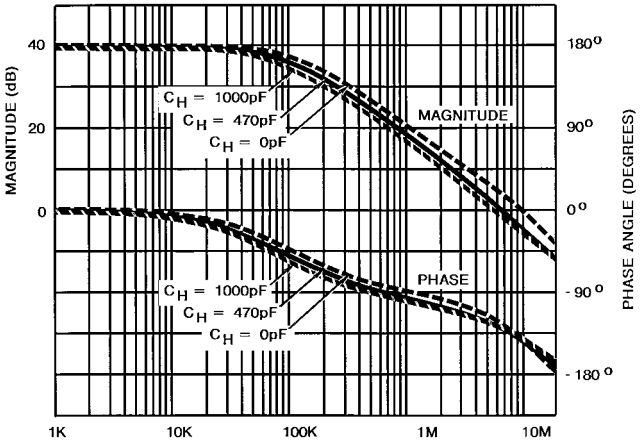
HOLD STEP ERROR vs. TEMPERATURE
$V_{IH} = 4V$, C_H = Internal
t_r = 5ns, 10ns, 20ns



CLOSED LOOP PHASE/GAIN
$A_V = +100$, ±15V and ±12V Supplies*



CLOSED LOOP PHASE/GAIN
$A_V = +100$



* ±15V and ±12V supplies trace the same line within the width of the line, therefore only one line is shown.

DESIGN INFORMATION (Continued)

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Typical Performance Characteristics

PARAMETER	CONDITIONS	TEMPERATURE	TYP	UNITS
Input Voltage Range		Full	±10	V
Offset Voltage Drift		Full	30	µV/C
Gain Bandwidth Product (ChExt = 0pF)	Av = +1, V_O = 200mVpp, R_L = 2K, C_L = 60pF	+25°C	10	MHz
Gain Bandwidth Product (ChExt = 100pF)	Av = +1, V_O = 200mVpp, R_L = 2K, C_L = 60pF	+25°C	9.6	MHz
Gain Bandwidth Product (ChExt = 1000pF)	Av = +1, V_O = 200mVpp, R_L = 2K, C_L = 60pF	+25°C	6.7	MHz
Full Power Bandwidth	V_O = 20Vpp, R_L = 2K, C_L = 60pF, Slew Rate Limited	+25°C	900	KHz
Output Resistance (Hold Mode)		+25°C	0.05	Ω
0.1% Acquisition Time	V_O = 10V Step, R_L = 2K, C_L = 60pF	+25°C	430	ns
0.01% Acquisition Time	V_O = 10V Step, R_L = 2K, C_L = 60pF	+25°C	700	ns
Effective Aperture Delay Time		+25°C	-15	ns
Aperture Uncertainty		+25°C	0.2	ns
1mV Hold Mode Settling Time		+25°C	200	ns