A Cirrus Logic Company

CS8403A CS8404A

96 kHz Digital Audio Transmitter

Features

- Sample rates up to 108 kHz
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 professional and consumer formats
- Generates CRC codes and parity bits
- On-Chip RS422 line driver
- Configurable buffer memory (CS8403A)
- Transparent mode allows direct connection of CS8404A and CS8414 or CS8403A and CS8413
- Pin compatible with CS8401A and CS8402A

Description

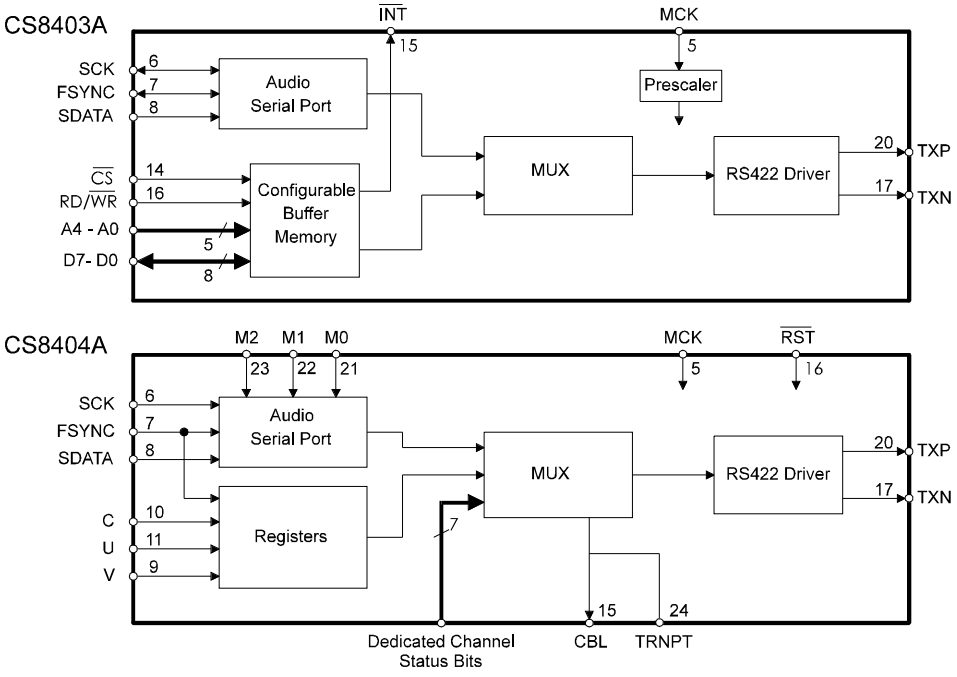
The CS8403A and CS8404A are digital audio transmitters which support 96 kHz sample rate operation. The devices encode and transmit audio data according to the AES/EBU, IEC958, S/PDIF, & EIAJ CP-340 interface standards. The CS8403A and CS8404A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8403A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8404A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

ORDERING INFO

CS8403A-CS, 0 to 70 °C, 24-pin Plastic SOIC
CS8404A-CS, 0 to 70 °C, 24-pin Plastic SOIC



Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS (GND = 0V, all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply		VD+	-	6.0	V
Input Current, Any Pin Except Supply	Note 1	I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VD+	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0V, all voltages with respect to ground)

Parameters		Symbol	Min	Typ	Max	Units
DC Voltage		VD+	4.75	5.0	5.25	V
Supply Current	Note 2	I_{DD}	-	3	10	mA
Ambient Operating Temperature	Note 3	T_A	0	25	70	°C
Power Consumption	Note 2	P_D	-	15	53	mW

Notes: 2. Drivers open (unloaded). The majority of power is used in the load connected to the drivers.

3. Specified to operate over 0 to 70 °C but tested at 25 °C only.

DIGITAL CHARACTERISTICS (T_A = 25 °C; VD+ = 5V ±5%)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	(VD+) + 0.3	V
Low-Level Input Voltage		V_{IL}	-0.3	-	+0.8	V
High-Level Output Voltage	I_O = 200 µA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_O = 3.2 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	1.0	10	µA
Master Clock Frequency	Note 4	MCK	-	-	27.6	MHz
Master Clock Duty Cycle			40	-	60	%

Notes: 4. MCK for the CS8403A must be 128, 192, 256, or 384x the input word rate based on M0 and M1 in control register 2. MCK for the CS8404A must be 128x the input word rate, except in Transparent Mode where MCK is 256x the input word rate.

Specifications are subject to change without notice

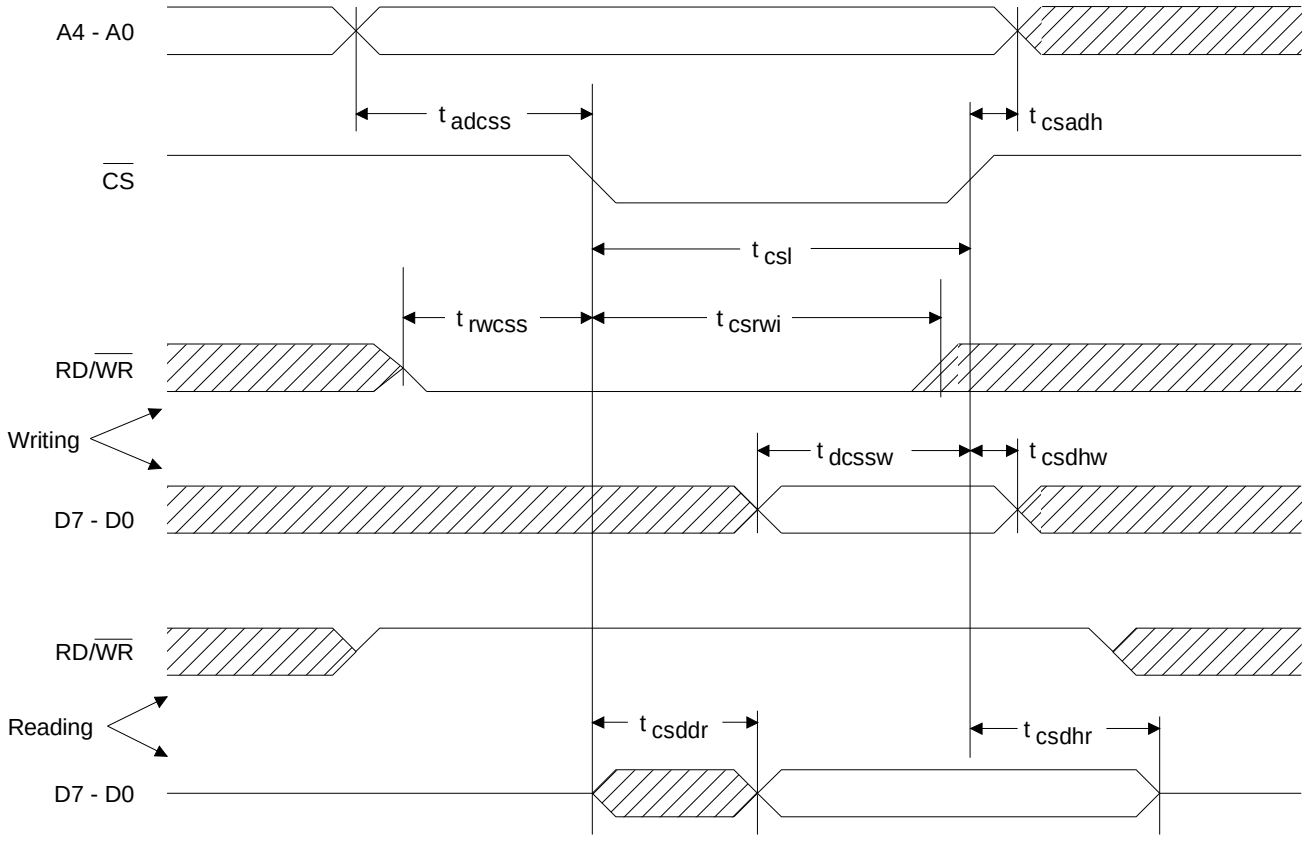
DIGITAL CHARACTERISTICS - RS422 DRIVERS (TXP, TXN pins only; VD+ = 5.0V ±5%)

Parameters		Symbol	Min	Typ	Max	Units
Output High Voltage	I_{OH} = -30 mA	V_{OH}	(VD+) - 0.7	(VD+) - 0.4	-	V
Output Low Voltage	I_{OL} = 30 mA	V_{OL}	-	0.4	0.7	V

SWITCHING CHARACTTERISTICS - CS8403A PARALLEL PORT (T_A = 25 °C;

VD+ = 5V, Inputs: Logic0 = GND, Logic1 = VD+, C_L = 20 pF)

Parameters		Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{CS}$ low		t_{adcss}	13.5	-	-	ns
$\overline{CS}$ high to ADDRESS invalid		t_{csadh}	0	-	-	ns
RD/$\overline{WR}$ valid to $\overline{CS}$ low		t_{rwcss}	10	-	-	ns
$\overline{CS}$ low to RD/$\overline{WR}$ invalid		t_{csrwi}	35	-	-	ns
$\overline{CS}$ low		t_{csl}	35	-	-	ns
DATA valid to $\overline{CS}$ rising	RD/$\overline{WR}$ low (writing)	t_{dcssw}	32	-	-	ns
$\overline{CS}$ high to DATA invalid	RD/$\overline{WR}$ low (writing)	t_{csdhw}	0	-	-	ns
$\overline{CS}$ falling to DATA valid	RD/$\overline{WR}$ high (reading)	t_{csddr}	-	-	35	ns
$\overline{CS}$ rising to DATA Hi-Z	RD/$\overline{WR}$ high (reading)	t_{csdhr}	5	-	-	ns



CS8403A Parallel Port Timing

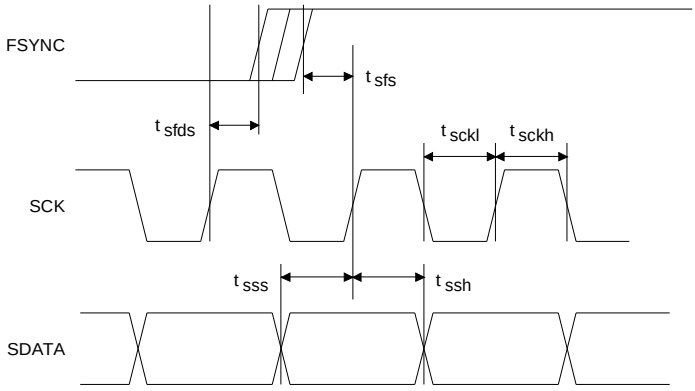
SWITCHING CHARACTERISTICS - SERIAL PORTS

(T_A = 25 °C; VD+ = 5V; Inputs: Logic0 = GND, Logic1 = VD+; C_L = 20 pF)

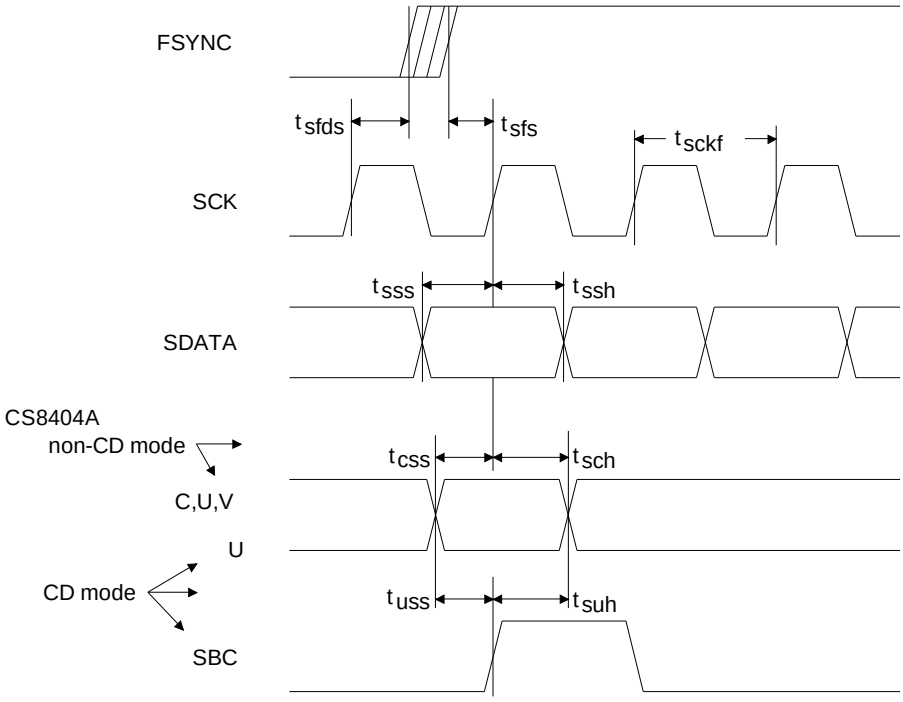
Parameters			Symbol	Min	Typ	Max	Units
Input Word Rate		Note 5	IWR	-	-	108	kHz
SCK Frequency	Master Mode Slave Mode	Note 6 Note 6	t_{sckf}	- -	IWR x 64	- 12.5	Hz MHz
SCK Pulse Width Low	Slave Mode	Note 6	t_{sckl}	25	-	-	ns
SCK Pulse Width High	Slave Mode	Note 6	t_{sckh}	25	-	-	ns
SCK rising to FSYNC edge delay		Notes 6, 7	t_{sfds}	20	-	-	ns
SCK rising to FSYNC edge setup		Notes 6, 7	t_{sfs}	20	-	-	ns
SDATA valid to SCK rising setup		Note 7	t_{sss}	20	-	-	ns
SCK rising to SDATA hold time		Note 7	t_{ssh}	20	-	-	ns
C, U, V valid to SCK rising setup	CS8404A non-CD Mode	Notes 7, 8	t_{css}	0	-	-	ns
SCK rising to C, U, V hold time	CS8404A non-CD Mode	Notes 7, 8	t_{scs}	50	-	-	ns
U valid to SBC rising setup	CS8404A, CD mode	Note 8	t_{uss}	0	-	-	ns
SBC rising to U hold time	CS8404A, CD mode	Note 8	t_{suh}	80	-	-	ns
$\overline{RST}$ Pulse Width	CS8404A			150	-	-	ns

Notes:

5. The input word rate (IWR) refers to the frequency at which stereo audio input sample pairs are input to the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample.
6. Master mode is defined as SCK and FSYNC being outputs. In Slave mode they are inputs. In the CS8403A, control register 3 bit 1, MSTR, selects master. In the CS8404A, only format 0 is master.
7. The table above assumes data is output on the falling edge and latched on the rising edge. In both parts the edge is selectable. The table is defined for the CS8403A with control register 3 bit 0, SCED, set to one, and for the CS8404A in formats 4 through 7. For the other formats, the table and figure edges must be reversed (i.e. “rising” to “falling” and vice versa).
8. The diagrams show SBC rising coincident with the first rising edge of SCK after FSYNC transitions. This is true for all modes except FSF0 & 1 both equal 1 in the CS8403A, and format 4 in the CS8404A. In these modes SBC is delayed one full SCK period.



Serial Input Timing - Slave Mode



Serial Input Timing - Master Mode & C, U, V Port

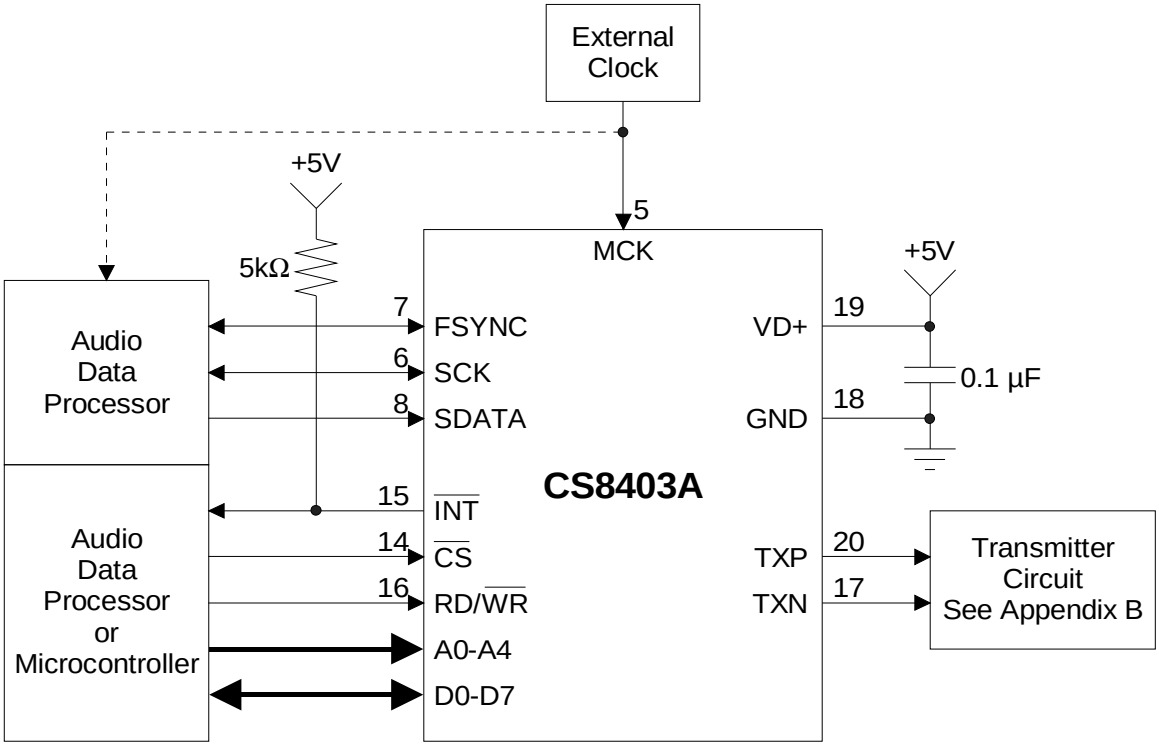


Figure 1. CS8403A Typical Connection Diagram

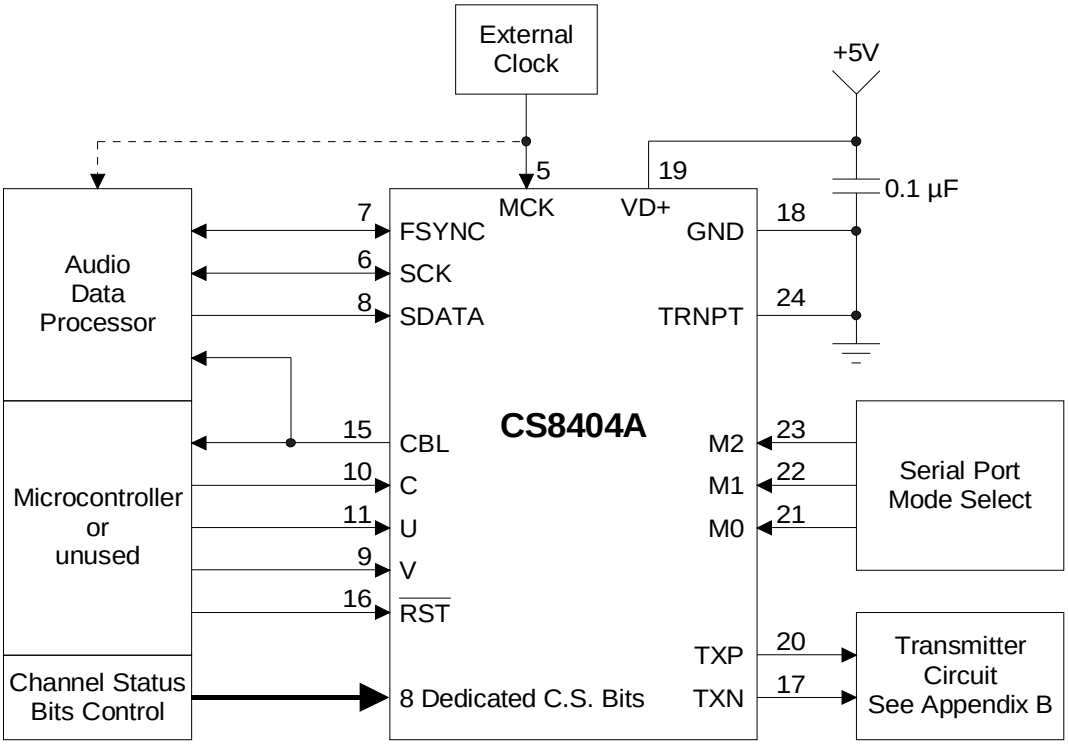


Figure 2. CS8404A Professional & Consumer Modes Typical Connection Diagram

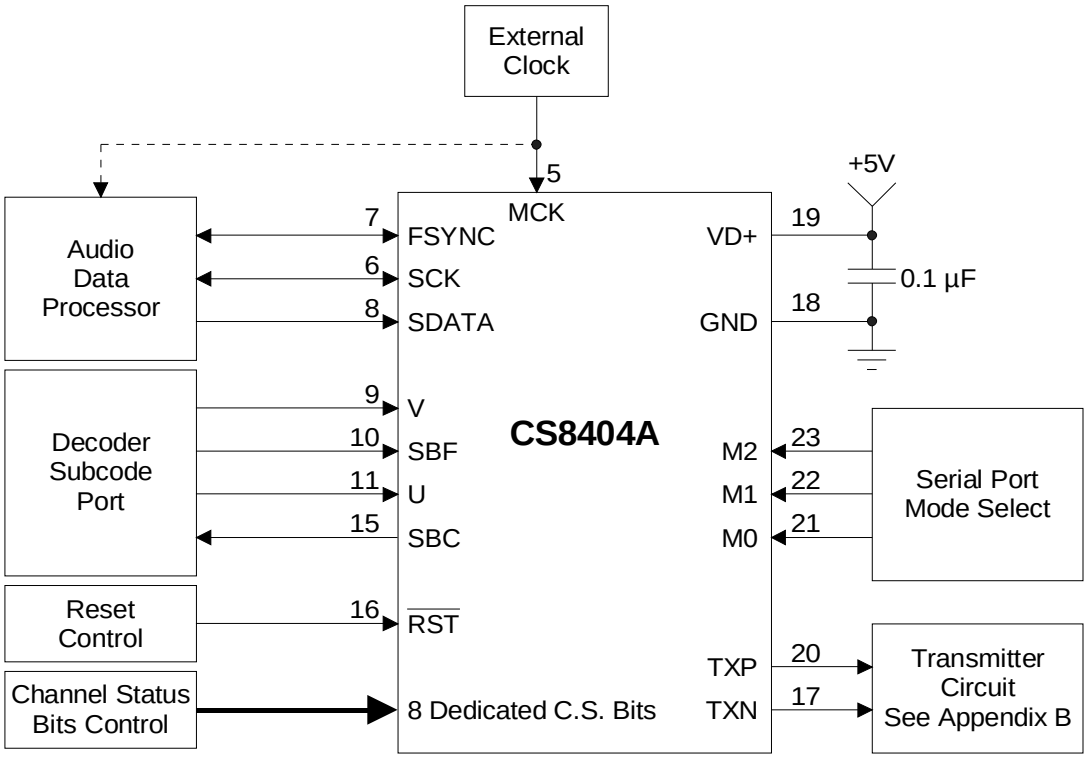


Figure 3. Consumer CD Submode Typical Connection Diagram

GENERAL DESCRIPTION

The CS8403A/4A are monolithic CMOS circuits that encode and transmit audio and digital data according to the AES/EBU, IEC958 (S/PDIF), and EIAJ CP-340 interface standards. Both chips accept audio and control data separately, multiplex and biphase-mark encode the data internally, and drive it, directly or through a transformer, to a transmission line. The CS8403A is fully software programmable through a parallel port and contains buffer memory for control data, while the CS8404A has dedicated pins for the most important control bits and a serial input port for the C, U, and V bits.

Familiarity with the AES/EBU and IEC958 specifications are assumed throughout this data sheet. Many terms such as channel status, user data, auxiliary data, professional mode, etc. are not defined. The Application Note, Overview of AES/EBU Digital Audio Interface Data Structures, provides an overview of the AES/EBU and IEC958 specifications and is included for clarity; however, it is not meant to be a complete reference, and the complete standards should be obtained from the Audio Engineering Society or ANSI for the AES/EBU document, and the International Electrotechnical Commission for the IEC document.

Line Drivers

The RS422 line drivers for both the CS8403A and CS8404A are low skew, low impedance, differential outputs capable of driving 110 Ω transmission lines with a 4 Vpp signal when configured as shown in Appendix A. To prevent possible short circuits, both drivers are set to ground when no master clock (MCK) is provided. They can also be disabled by resetting the device ($\overline{RST}$ = low). Appendix A contains more information on the line drivers. A 0.1 µF capacitor, with short leads, should be placed as close as possible to the VD+ and GND pins.

CS8403A DESCRIPTION

The CS8403A accepts 16- to 24-bit audio samples through a configurable serial port, and channel status, user, and auxiliary data through an 8-bit parallel port. The parallel port allows access to 32 bytes of internal memory which is used to store control information and buffer channel status, user, and auxiliary data. This data is multiplexed with the audio data from the serial port, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver. A block diagram of the CS8403A is shown in Figure 4. In accordance with the professional definition of channel status, the CRCC code (C.S. byte 23) can be internally generated.

Parallel Port

The parallel port accesses one status register, three control registers, and 28 bytes of dual port buffer memory. The address bus and RD/$\overline{WR}$ line must be valid when $\overline{CS}$ goes low. If RD/$\overline{WR}$ is low, the value on the data bus will be written into the buffer memory at the specified address. If RD/$\overline{WR}$ is high, the value in the buffer memory, at the specified address, is placed on the data bus. The detailed timing for reading and writing the CS8403A can be found in the Digital Switching Characteristics table. The memory space is allocated as shown in Figure 5. There are three defined buffer memory modes selectable by two bits in control register 2.

Status and Control Registers

Upon power up the CS8403A control registers contain all zeros. Therefore, the part is initially in reset and is muted. One's must be written to control register 2, bits $\overline{RST}$ and $\overline{MUTE}$, before the part will transmit data. *The remaining registers are not initialized on power-up and may contain random data.*

The first register, shown in Figure 6, is the status register in which only three bits are valid. The lower three bits contain flags indicating the position of

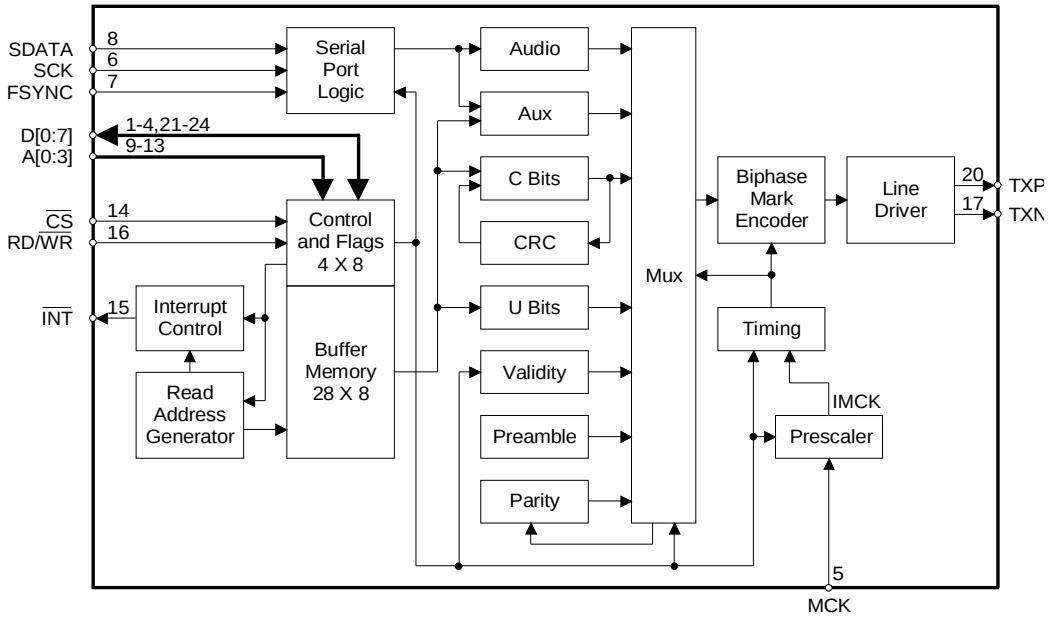


Figure 4. CS8403A Block Diagram

the transmit pointer in the buffer memory. These flags may be used to avoid contention between the transmit pointer reading the data and the user updating the buffer memory. Besides indicating the byte location being transmitted, the flags indicate the block of memory the part is currently addressing, thereby telling the user which block is free to be written. Each flag has a corresponding mask bit (control register1) which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. Flag 0 and flag 1 cause interrupts on both edges whereas flag 2 causes an interrupt only on the rising edge. Timing and further explanation of the flags can be found in the buffer memory section.

The two most significant bits of control register 1, BKST and TRNPT, are used for Transparent Mode operation of the CS8403A. Transparent Mode is used for those applications where it is useful to maintain frame alignment between the received and transmitted audio data signals. In Transparent Mode (TRNPT="1") the MCK, FSYNC, SCK and SDATA inputs of the CS8403A can be connected to their corresponding outputs of the CS8413. In Transparent Mode, FSYNC synchronizes the transmitter and the receiver. The data delay through the CS8403A is set so that three frame delays occur from the input of the CS8413 to the output of the CS8403A. In Transparent Mode, 32 SCKs are required per subframe.

Channel status block alignment between the CS8413 and the CS8403A is accomplished by setting BKST high at the occurrence of the Flag 2 rising edge of the CS8413. If FSYNC is a left/right signal, BKST is sampled once per frame; if FSYNC is a word clock, BKST is sampled once per subframe. A low to high transition of BKST (based on two successive internal samples) resets the channel status block boundary to the beginning.

Control register 2, shown in Figure 8, contains various system level functions. The two most significant bits, M1 and M0, select the frequency at the MCK pin as shown in Table 1. As an example, if the audio sample frequency is 44.1 kHz and M0 and M1 are both zero, MCK would then be 128x the audio sample rate or 5.6448 MHz. The next bit (5) in control register 2, V, indicates the validity of the current audio sample. According to the digital audio specifications, V=0 signifies that the audio signal is suitable for conversion to analog. B1 and

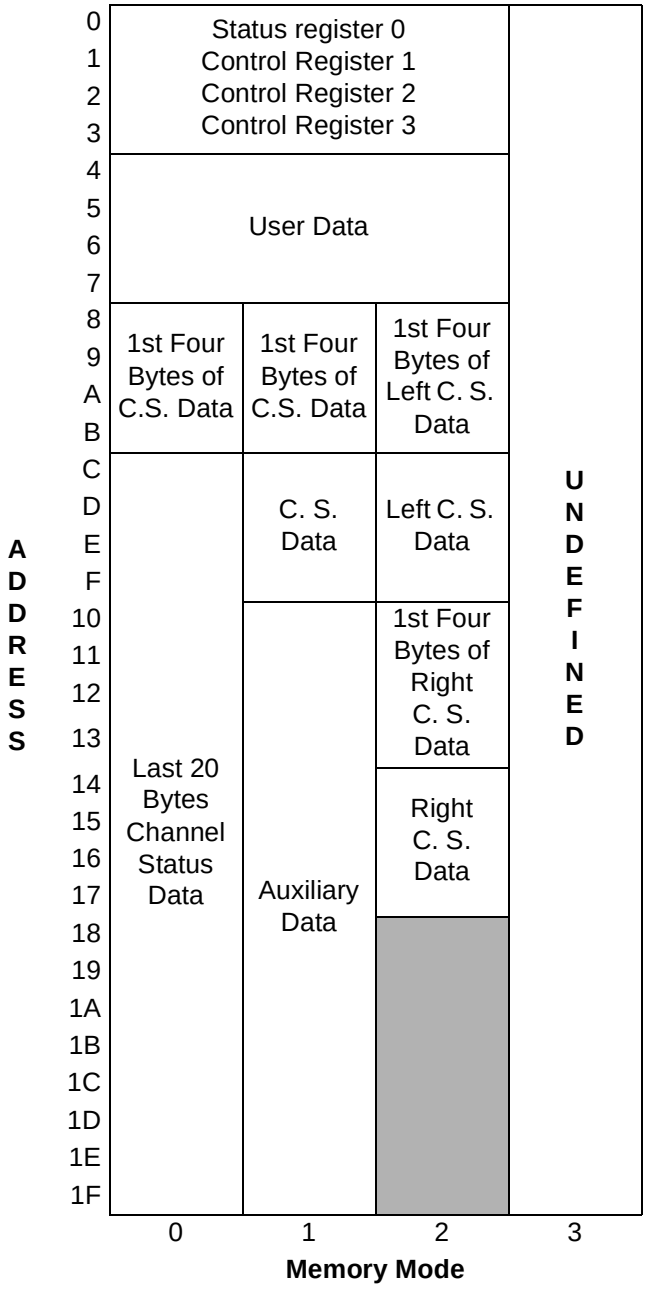
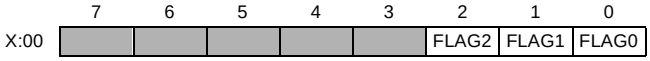


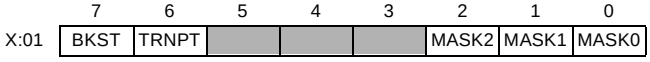
Figure 5. CS8403A Buffer Memory Modes

B0 select one of three modes for the buffer memory. The different modes are shown in Figure 5 and the bit combinations in Table 2. More information on the different modes can be found in the **Buffer Memory** section. Bit 2, CRCE, is the channel status CRCC enable and should only be used in professional mode. When CRCE is high, the channel status data cyclic redundancy check characters are



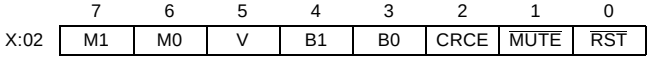
FLAG2: High for first four bytes of channel status
FLAG1: Memory mode dependent - See Figure 11
FLAG0: High for last two bytes of user data

Figure 6. Status Register



BKST: Causes realignment of data block when set to "1"
TRNPT: Selects Transparent Mode appropriatley setting data delay through device
MASK2: Interrupt mask for FLAG2. A "1" enables the interrupt.
MASK1: Interrupt mask for FLAG1.
MASK0: Interrupt mask for FLAG0.

Figure 7. Control Register 1



M1: with M0, selects MCK frequency.
M0: with M1, selects MCK frequency.
V: Validity bit of current sample.
B1: with B0, selects the buffer memory mode
B0: with B1, selects the buffer memory mode
CRCE: Channel status CRC Enable. Professional mode only.
$\overline{\text{MUTE}}$: When clear, transmitted audio data is set to zero.
$\overline{\text{RST}}$: When clear, drivers are disabled, frame counters cleared.

Figure 8. Control Register 2

M1	M0	MCLK
0	0	128x Input Word Rate
0	1	192x Input Word Rate
1	0	256x Input Word Rate
1	1	384x Input Word Rate

Table 1. MCLK Frequencies

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 2. Buffer Memory Modes

generated independently for channels A and B and are transmitted at the end of the channel status block. When $\overline{\text{MUTE}}$ (bit 1) is low, the transmitted audio data is forced to zero. Both $\overline{\text{RST}}$ and $\overline{\text{MUTE}}$ are set to zero upon power up.

When $\overline{\text{RST}}$ is low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the rest of the CS8403A to the audio serial port, the transmit timing counters, which include the flags in the status register, are not enabled after $\overline{\text{RST}}$ is set high until eight and one half SCK periods after the active edge (first edge after reset is exited) of FSYNC.

When FSYNC is configured as a left/right signal (FSF1=1), the counters and flags are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and channel B is right as per the digital audio interface specs.

Control register 3 contains format information for the serial audio input channel. The MSB is unused and the next three bits, SDF2-SDF0, select the format for the serial input data with respect to FSYNC. There are five valid combinations of these bits as shown in Figure 10. The next two bits, FSF1 and FSF0, select the format of FSYNC. Two of the formats delineate each channel's data and do not indicate the particular channel. The other two formats also indicate the specific channel. The formats are shown in Figure 10. Bit1, MSTR, determines whether FSYNC and SCK are inputs, MSTR low, or outputs, MSTR high. Bit0, serial clock edge select, SCED, selects the edge that audio data gets latched on. When SCED is low, the falling edge of SCK latches data in the chip and when SCED is high, the rising edge is used.

	7	6	5	4	3	2	1	0
X:03		SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

SDF2: with SDF0 & SDF1, select serial data format.
SDF1: with SDF0 & SDF2, select serial data format.
SDF0: with SDF1 & SDF2, select serial data format.
FSF1: with FSF0, select FSYNC format.
FSF0: with FSF1, select FSYNC format.
MSTR: When set, SCK and FSYNC are outputs.
SCED: When set, rising edge of SCK latches data.
When clear, falling edge of SCK latches data.

Figure 9. Control Register 3

The multitude of combinations allow for a zero glue logic interface to almost all DSPs, encoder chips, and standard serial data formats.

Serial Port

The serial port is used to enter audio data and consists of three pins: SCK, SDATA, and FSYNC. The serial port is double buffered with SCK clocking in the data from SDATA, and FSYNC delineating audio samples and may define the particular channel, left or right.

Control register 3, shown in Figure 9, configures the serial port. All the various formats are illustrated in Figure 10. When FSF1 is low, FSYNC only delineates audio samples. When FSF1 is high, it delineates audio samples and specifies the channel. When FSF1 is low and the port is a master (MSTR = 1), FSYNC is a square wave output. When FSF1 is low and the port is a slave (input), FSYNC can be a square wave or a pulse provided the active edge, as defined in Figure 10, is properly positioned with respect to SDATA.

Bits 4, 5, and 6, SDF0-SDF2, define the format of SDATA and is also described in Figure 10. The five allowable formats are MSB first, MSB last, 16-bit LSB last, 18-bit LSB last, and 20-bit LSB last. The MSB first and MSB last formats accept any word length from 16 to 24 bits. The word length is controlled by providing trailing zeros in MSB first mode and leading zeros in MSB last mode, or by restricting the number of SCK periods between samples to the sample word length. The 16-, 18-, and 20-bit LSB-last modes require at least 16, 18, or 20

SCK periods per sample respectively. As a master, 32 SCK periods are output per sample.

FSYNC must be derived from MCK via a DSP using the same clock or by external counters. If FSYNC moves (jitters) with respect to MCK by more than 4 MCK periods, the CS8403A may reset the channel status block and flags. Appendix C contains more information on the relationship of FSYNC and MCK.

Buffer Memory

In all buffer modes, the status register and control registers are located at addresses 0-3 respectively, and the user data is buffered in locations 4-7. The parallel port can access any location in the user data buffer at any time; however, care must be taken not to modify a location when that location is being read internally. This internal reading is done through the second port of the buffer in a cyclic manner.

Reset initializes the internal pointer to 04H(Hex). Data is read from this location and stored in an 8-bit shift register which is shifted once per audio sample. (An audio sample is defined as a single channel, not a stereo pair.) The byte is transmitted LSB first, D0 being the first bit. After transmitting 8 samples, i.e. 8 user bits, the address pointer is incremented and the next byte of user data is loaded into the shift register. After transmitting all four bytes, 32 audio samples, the user read pointer is reset to 04H (Hex) and the cycle repeats.

Flag 0 in the status register monitors the position of the internal user data read pointer. When the first byte, location 04H, is read, flag 0 is set low and when the third byte, location 06H, is read, flag 0 is set high. If mask 0 in control register1 is set, a transition of flag 0 will generate a low pulse on the interrupt pin. The value of flag 0 indicates which two bytes the part will read next, thereby indicating which two bytes are free to be updated.

Flag 1 is mode dependent, changing with buffer memory configuration, and is discussed in the individual buffer mode sections.

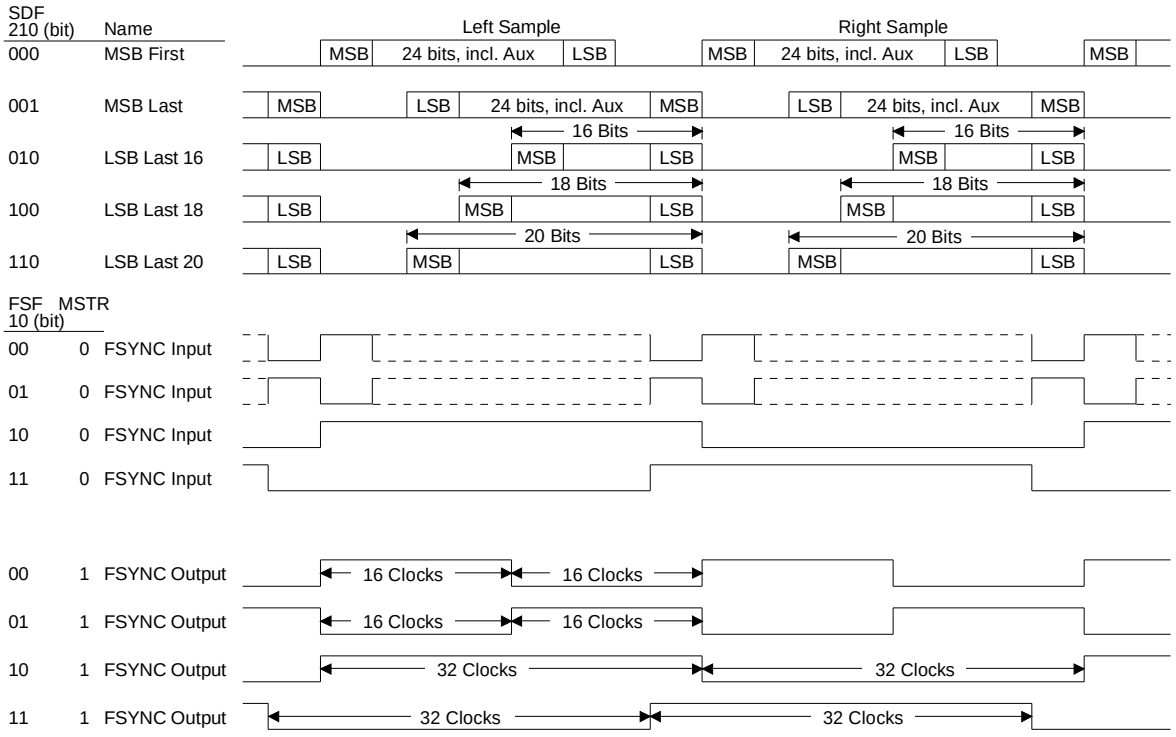


Figure 10. CS8403A Serial Port SDATA and FSYNC Timing

Flag 2 is set high when byte 0 of the channel status, address 08H, is read, and set low when byte 4, address 0BH, is read. Therefore, flag 2 high indicates the part is reading the first four bytes of channel status and the last 20 bytes are free to update. If the interrupt mask bit for flag 2 is set, the rising edge will cause an interrupt indicating the beginning of a channel status block as shown in Figure 11. Although a falling edge on flag 0 and flag 1 may cause an interrupt, the falling edge of flag 2 will not.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of channel status data and 384 audio samples. (This figure assumes the channel status bit is the same for the audio pair.) The lower portion of Figure 11 expands the first byte of channel status showing eight pairs of data with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits as per the AES/EBU specifications (see Appendix A). When transmitting stereo, channel A is left and channel B is right. The preamble at the bottom of Figure 11 is expanded in Figure 15 to show the exact timing between flags, the interrupt pin, and internal buffer-read timing.

Buffer Mode 0

In buffer mode 0, in addition to the user-data buffer previously discussed, one entire block of channel status data is buffered in 24 memory locations from address 08H to 1FH. This block will be transmitted

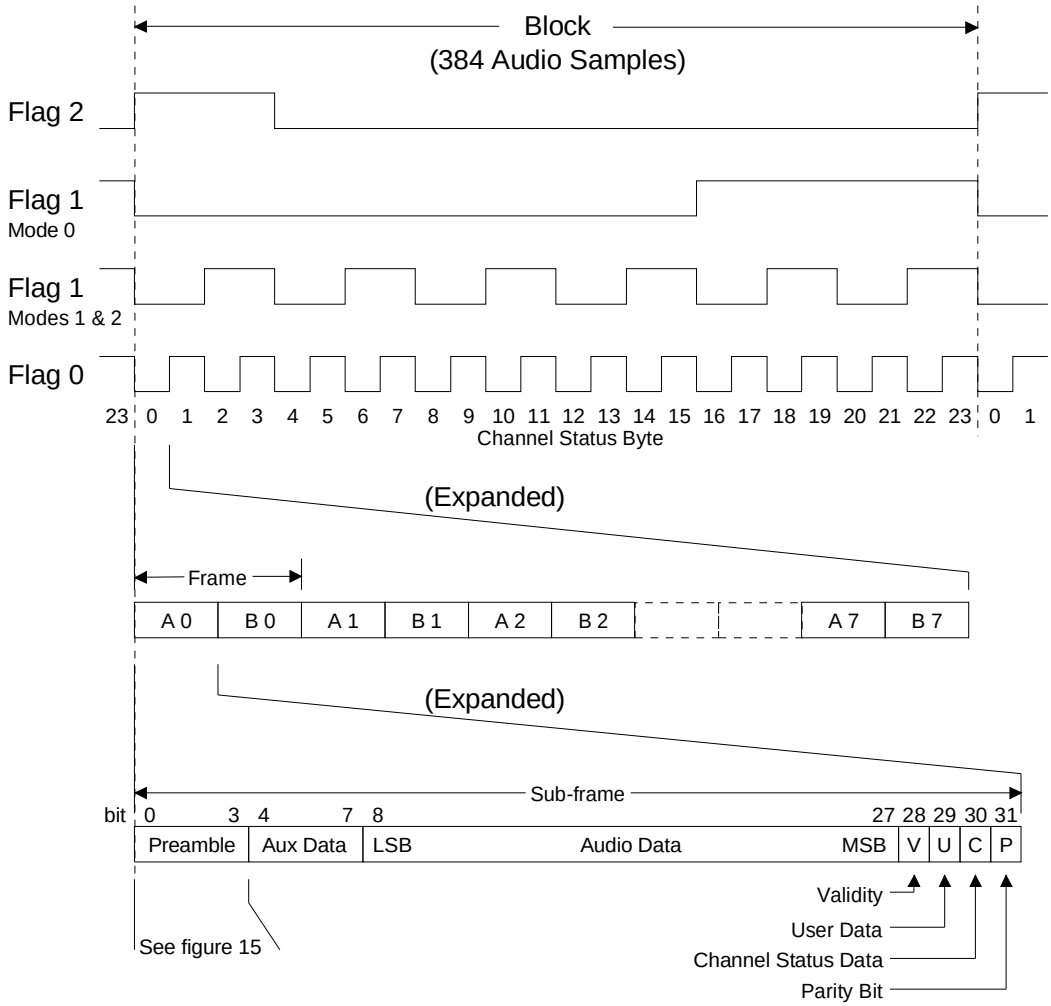


Figure 11. CS8403A Status Register Flag Timing

in both channel A and channel B, one bit per frame. Like the user-data buffer, the parallel port can access any location in this buffer at any time. The transmitter section reads this buffer in a cyclic non-destructive manner and stores the byte in an 8-bit shift register that is shifted once per two transmitted audio samples (once per frame).

Flag1 in the status register can be used to monitor the channel status buffer. In mode 0, flag 1 is set low when byte 0, location 08H, is read and set high when byte 16, location 18H, is read. If mask 1 in control register 1 is set, a transition on flag 1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory read sequence for buffer mode 0 along with the flag timing. The arrows on the flags indicate an interrupt if the appropriate mask bit is set. Flag 0 can cause an interrupt on either edge, which is shown only in the expanded portion of the Figure for clarity. The expanded section also shows that the user buffer is reread when location 0AH of the channel status is read.

Buffer Mode 1

In buffer mode 1, eight bytes are allocated for channel status data and 16 bytes for auxiliary data as shown in Figure 5. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are read once per channel status block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data.

Similar to mode 0, transmitted channel status data will be the same for channel A and channel B (one channel status bit per frame). Flag 1 and flag 2 can be used to monitor this buffer. Flag 1 is set low when byte 0 of channel status data, location 08H, is read and is toggled when every other byte is read. As shown in Figure 13, flag 2 is set high when byte 0, location 08H, is read and set low when byte 4, location 0CH, is read. Flag 2 determines whether the channel status pointer is reading the first four-byte section or the second four-byte section, while flag 1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is read in a cyclic manner similar to the data buffer; however, four auxiliary data bits are transmitted per audio sample (sub-frame). Since the auxiliary buffer must be read four times as often as the user data buffer and is four times as large, flag 0 can be used to monitor both.

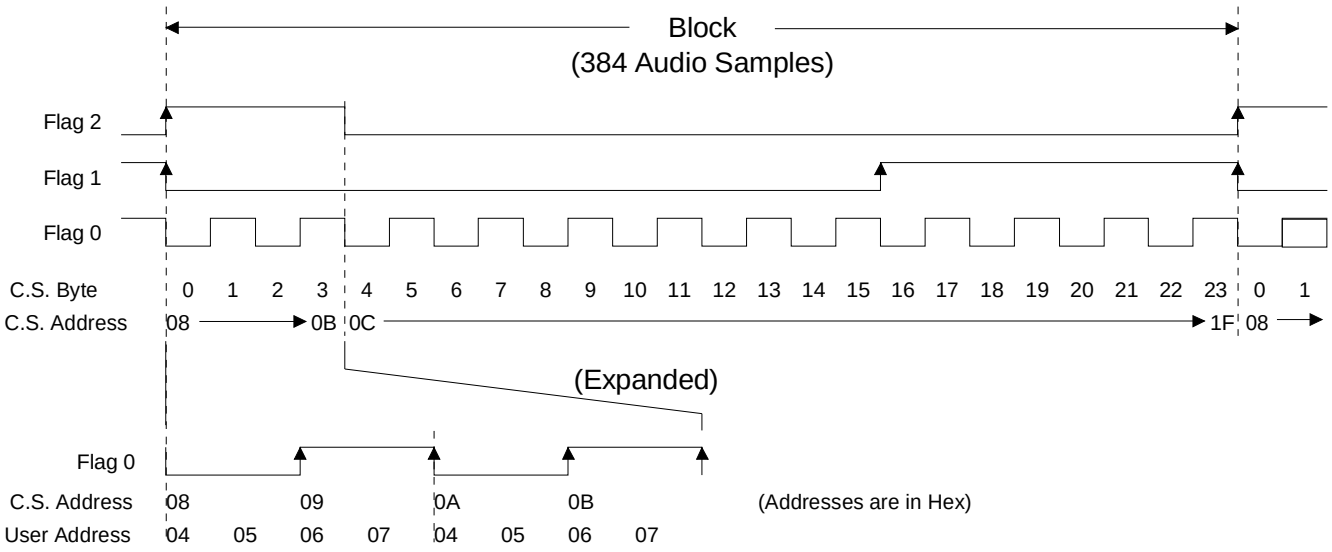


Figure 12. CS8403A Buffer Momory Read Sequence - MODE 0

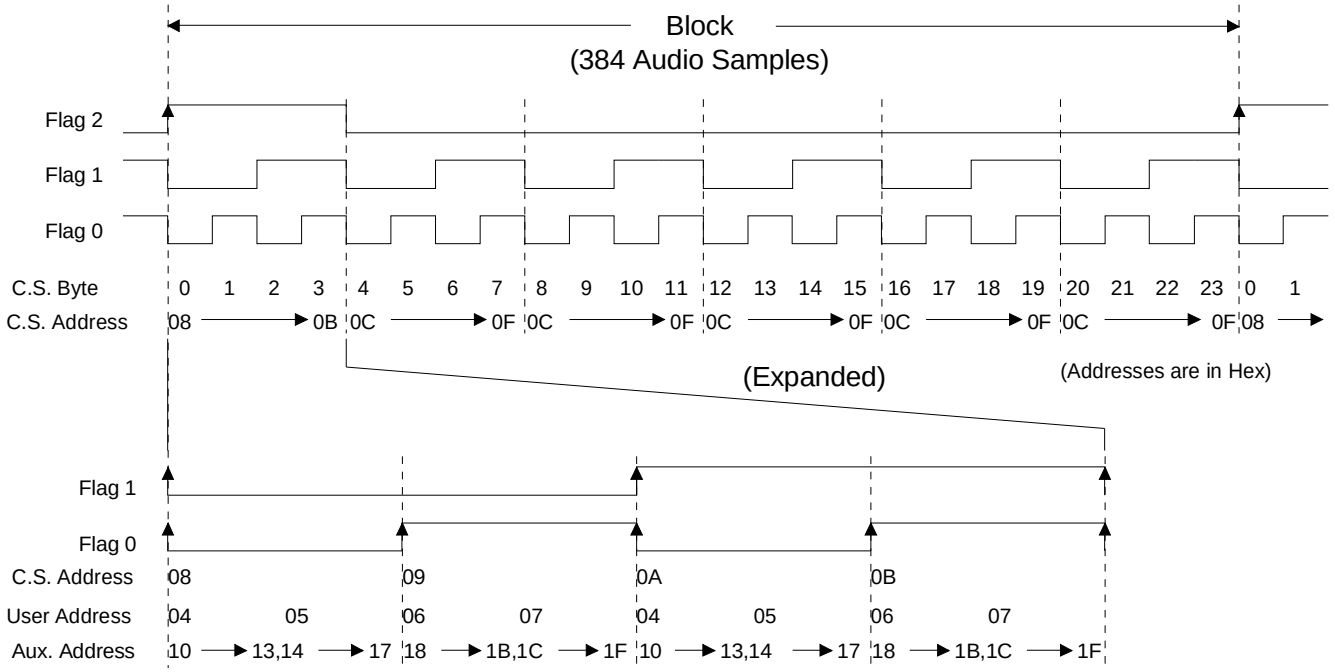


Figure 13. CS8403A Buffer Memory Read Sequence - MODE 1

Buffer Mode 2

In buffer mode 2, two 8-byte buffers are available for buffering both channel A and channel B channel status data independently. Both buffers are identical to the channel status buffer in mode 1 except that each channel can have unique channel status data. The two buffers are read simultaneously with locations 08H to 0FH transmitted in channel A and locations 10H to 17H transmitted in channel B. Figure 5 contains the buffer memory modes and Figure 14 illustrates the buffer read sequence for mode 2.

Buffer-Read and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally writing to the buffer ram and the CS8403A internally reading bytes of ram for transmission may be averted by using the flag levels to avoid the section currently being addressed by the part. Interrupts occur at flag edges indicating the exact byte that the part is currently reading. Utilizing $\overline{INT}$ along with the flags, the byte currently being read by the part can be avoided allowing access to all other bytes instead of just a section. Figure 15 illustrates the timing between flags, $\overline{INT}$, and the internal reading of the buffer for transmission. The master clock IMCK is shown as 128x Fs. Other MCK frequencies are initially divided to obtain 128x Fs, defined as IMCK (internal MCK), which is then used for all internal timing, so the timing in Figure 15 is valid for all MCK frequencies. When the parity bit (P) is transmitted, a transition on a flag causes $\overline{INT}$ to go low if the appropriate mask bit is set. Concurrently, the part starts reading from the internal buffer. Writing to the buffer ram location being read by the part should be avoided while the internal "ram read" signal is high.

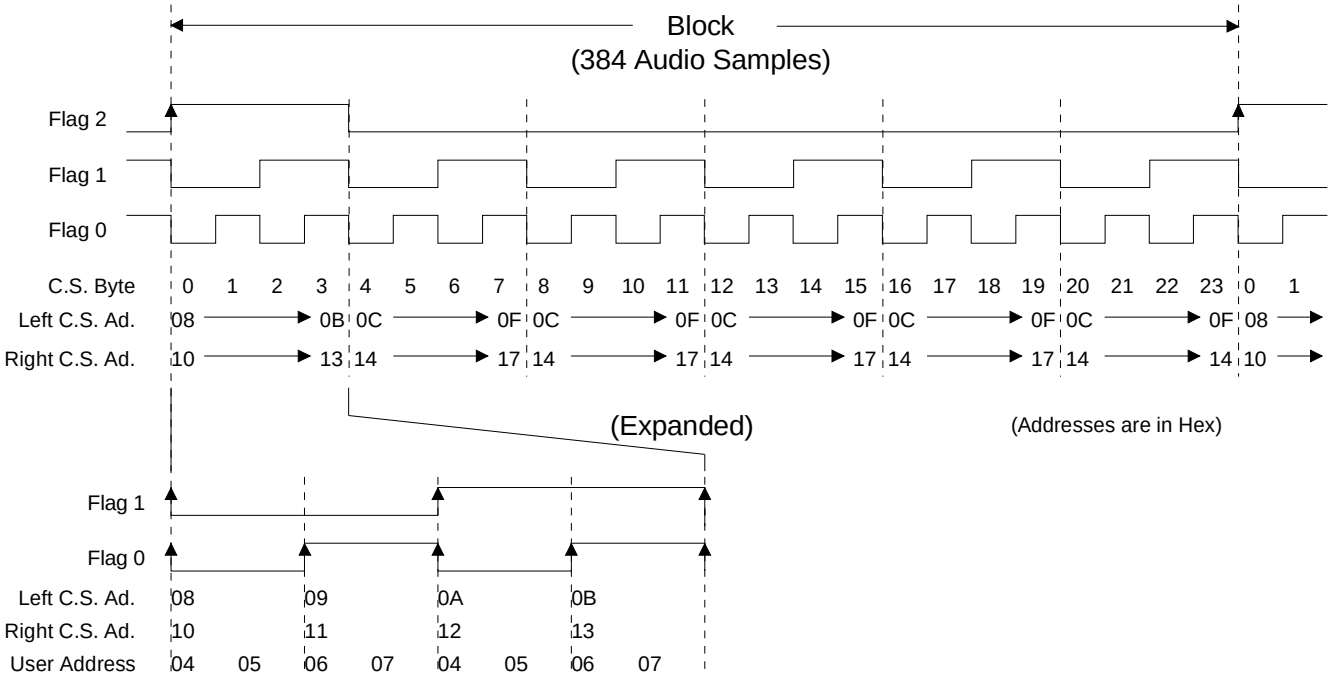


Figure 14. CS8403A Buffer Memory Read Sequence - MODE 2

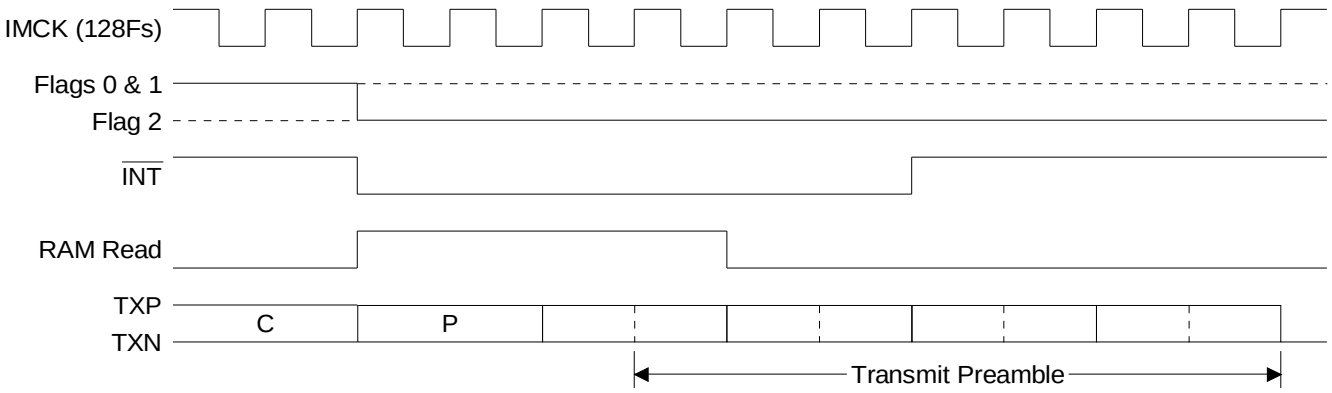
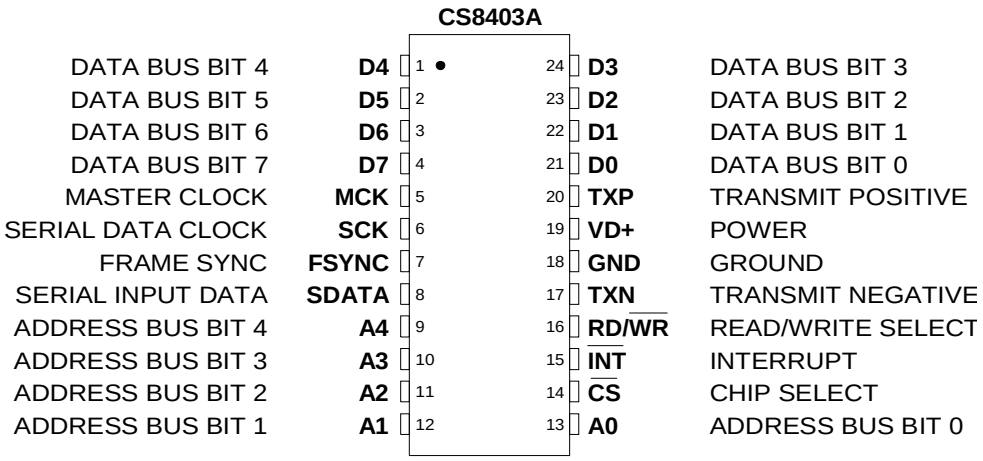


Figure 15. RAM/Buffer-Read and Interrupt Timing

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

GND - Ground, PIN 18.

Ground for the digital section.

Audio Input Interface

SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via control register 3) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 3.

SDATA - Serial Data, PIN 8.

Audio data serial input pin.

Parallel Interface

$\overline{CS}$ - Chip Select, PIN 14.

This input is active low and allows access to the 32 bytes of internal memory. The address bus and RD/$\overline{WR}$ must be valid while $\overline{CS}$ is low.

RD/$\overline{WR}$ - Read/Write, PIN 16.

If RD/$\overline{WR}$ is low when $\overline{CS}$ goes active (low), the data on the data bus is written to internal memory. If RD/$\overline{WR}$ is high when $\overline{CS}$ goes active, the data in the internal memory is placed on the data bus.

A4-A0 - Address Bus, PINS 9-13.

Parallel port address bus that selects the internal memory location to be read from or written to.

D0-D7 - Data Bus, PINS 21-24, 1-4.

Parallel port data bus used to check status, write control words, or write internal buffer memory.

$\overline{INT}$ - Interrupt, PIN 15.

Open drain output that can signal the state of the internal buffer memory. A 5 kΩ resistor to VD+ is typically used to support logic gates. All bits affecting $\overline{INT}$ are maskable allowing total control over the interrupt mechanism.

Transmitter Interface

MCK - Master Clock, PIN 5.

Clock input which defines the transmit timing. It can be configured, via control register 2, for 128, 192, 256, or 384 times the sample rate.

TXP, TXN - Differential Line Drivers, PINS 20, 17.

RS422 compatible line drivers. Drivers are pulled low when part is in reset state.

CS8404A DESCRIPTION

The CS8404A accepts 16- to 24-bit audio samples through a serial port configured in one of seven formats, provides several pins dedicated to particular channel status bits, and allows all channel status, user, and validity bits to be serially input through port pins. This data is multiplexed, the parity bit is generated, and the bit stream is biphase-mark encoded and driven through an RS422 line driver.

The CS8404A operates as a professional or consumer interface transmitter selectable by pin 2, $\overline{\text{PRO}}$. As a professional interface device, the dedicated channel status input pins are defined according to the professional standard, and the CRC code (C.S. byte 23) can be internally generated.

As a consumer device, the dedicated channel status input pins are defined according to the consumer standard. A submode provided under the consumer mode is compact disk, CD, mode. When transmitting data from a compact disk, the CD subcode port can accept CD subcode data, extract channel status information from it, and transmit it as user data.

The master clock, MCK, controls timing for the entire chip and must be 128x Fs. As an example, if stereo data is input to the CS8404A at 44.1 kHz, MCK input must be 128 times that or 5.6448 MHz.

Audio Serial Port

The audio serial port is used to enter audio data and consist of three pins: SCK, SDATA, and FSYNC. SCK clocks in SDATA, which is double buffered, while FSYNC delineates the audio samples and may indicate the particular channel, left or right. To support many different interfaces, M2, M1, and M0 select one of seven different formats for the serial port. The coding is shown in Table 3 while the formats are shown in Figure 16. Format 0 and 1 are designed to interface with Crystal ADCs. Format 2 communicates with Motorola and TI DSPs. Format 3 is reserved. Format 4 is compatible with the I^2S standard. Formats 5 and 6 make the CS8404A look similar to existing 16- and 18-bit DACs, and interpolation filters. Format 7 is an MSB-last format and is conducive to serial arithmetic. SCK and FSYNC are outputs in Format 0 and inputs in all other formats. In Format 2, the rising edge of FSYNC delineates samples and the falling edge must occur a minimum of one bit period before or after the rising edge. In all formats except 2, FSYNC contains left/right information requiring both edges of FSYNC to delineate samples. Formats 5 and 6 require a minimum of 16- or 18-bit audio words respectively. In all formats other than 5 and 6, the CS8404A can accept any word length from 16 to 24 bits by adding leading zeros in format 7 and trailing zeros in the other formats, or by restricting the number of SCK periods between active edges of FSYNC to the sample word length.

M2	M1	M0	Format
0	0	0	0 - FSYNC & SCK Output
0	0	1	1 - Left/Right, 16-24 Bits
0	1	0	2 - Word Sync, 16-24 Bits
0	1	1	3 - Reserved
1	0	0	4 - Left/Right, I^2S Compatible
1	0	1	5 - LSB Justified, 16 Bits
1	1	0	6 - LSB Justified, 18 Bits
1	1	1	7 - MSB Last, 16-24 Bits

Table 3. CS8404A Audio Port Modes

FSYNC must be derived from MCK, either through a DSP using the same clock, or using counters. If FSYNC moves (jitters) with respect to MCK by four MCK periods, the internal counters and CBL may be reset. Appendix B contains more information on the relationship between FSYNC and MCK.

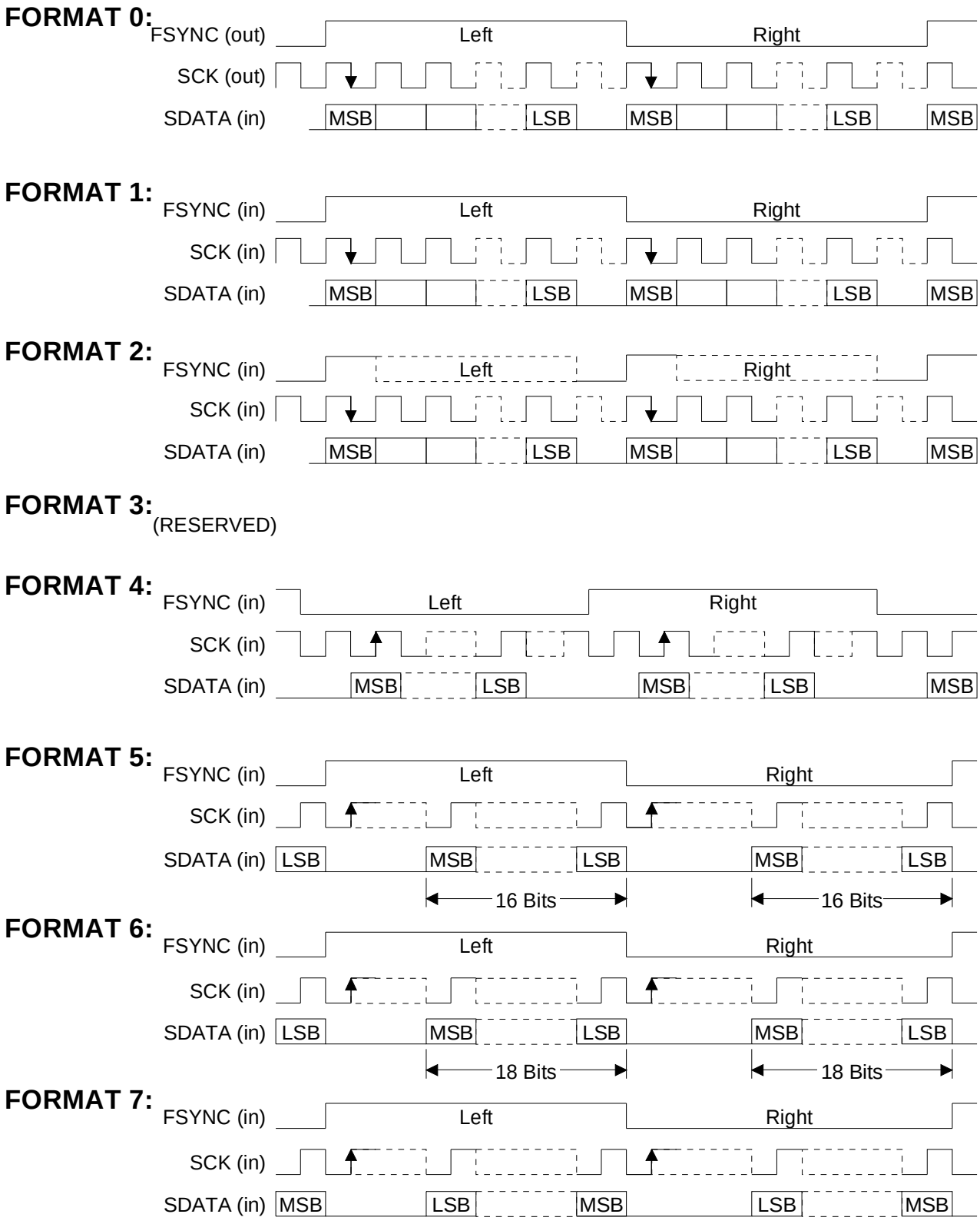


Figure 16. CS8404A Audio Serial Port Formats

C, U, V Serial Port

The serial input pins for channel status (C), user (U), and validity (V) are sampled during the first bit period after the active edge of FSYNC for all formats except Format 4. Format 4 is sampled during the second bit period (coincident with the MSB). In Figure 16, the arrows on SCK indicate when the C, U, and V bits are sampled. The C, U, and V bits are transmitted with the audio sample entered before the FSYNC edge that sampled it. The V bit, as defined in the audio standards, is set to zero to indicate the audio data is suitable for conversion to analog. Therefore, when the audio data is errorred, or the data is not audio, the V bit should be set high. The channel status serial input pin (C) is not available in consumer mode when the CD subcode port is enabled (FC1 = FC0 = high). Any channel status data entered through the channel status serial input (C) is logically OR'ed with the data entered through the dedicated pins or internally generated.

$\overline{\text{RST}}$ and CBL (TRNPT is low)

When $\overline{\text{RST}}$ goes low, the differential line drivers are set to ground and the block counters are reset to the beginning of the first block. In order to properly synchronize the CS8404A to the audio serial port, the transmit timing counters, which include CBL, are not enabled after $\overline{\text{RST}}$ goes high until eight and one half SCK periods after the active edge (first edge after reset is exited) of FSYNC. When FSYNC is configured as a left/right signal (all defined formats except 2), the counters and CBL are not enabled until the right sample is being entered (during which the previous left sample is being transmitted). This guarantees that channel A is left and channel B is right as per the digital audio interface specs.

As shown in Figure 17, channel block start output (CBL), can assist in serially inputting the C, U and V bits as CBL goes high one bit period before the first bit of the preamble of the first sub-frame of the

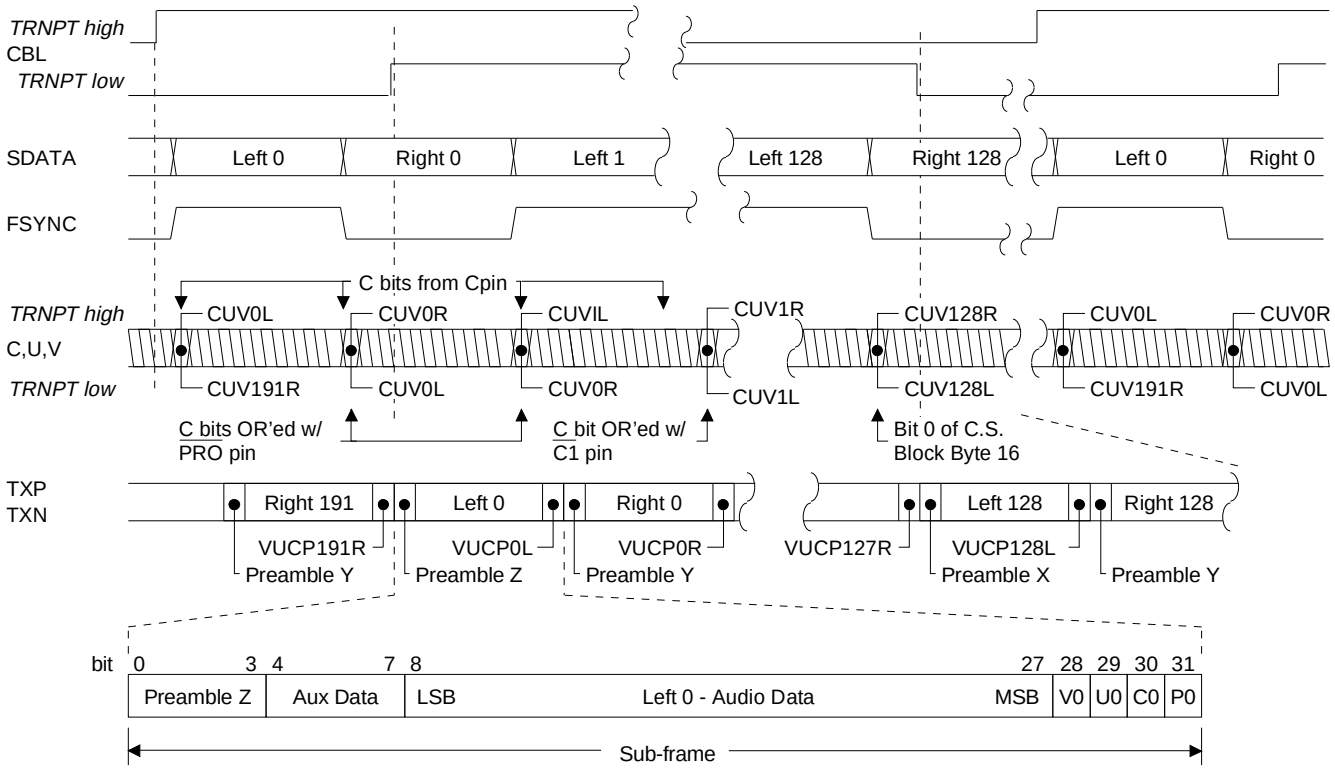


Figure 17. CBL and Tranmitter Timing

channel status block is transmitted. This sub-frame contains channel status byte 0, bit 0. CBL returns low one bit period before the start of the frame that contains bit 0 of channel status byte 16. CBL is the exact inverse of flag 1 in mode 0 on the CS8403A (see Figure 11). CBL is not available when the CD subcode port is enabled.

Figure 17 illustrates timing for stereo data input on the audio port. Notice how CBL rises while the right channel data (Right 0) is input, but the previous left channel data (Left 0) is being transmitted as the first sub-frame of the channel status block (starting with preamble Z). The C, U, and V input ports only need to be valid for a short period after FSYNC changes. A sub-frame includes one audio sample while a frame includes a stereo pair. A channel status (C.S.) block contains 24 bytes of channel status and 384 audio samples (or 192 stereo pairs, or frames, of samples).

Figure 17 shows the CUV ports as having left and right bits (e.g. CUV0L, CUV0R). Since the C.S. block is defined as 192 bits, or one bit per frame, there are actually 2 C.S. blocks, one for channel A (left) and one for channel B (right). When inputting stereo audio data, both blocks normally contain the same information, so C0L and C0R from the input port pin are both channel status bit 0 of byte 0, which is defined as professional/consumer. These first two bits from the port, C0L and C0R, are logically OR'ed with the inverse of $\overline{PRO}$, since $\overline{PRO}$ is a dedicated channel status pin defined as C.S. bit 0. Also, if in professional mode, $\overline{C1}$, $\overline{C6}$, $\overline{C7}$ and $\overline{C9}$ are dedicated C.S. pins. The inverse of $\overline{C1}$ is logically OR'ed with channel status input port bits C1L and C1R. In similar fashion, $\overline{C6}$, $\overline{C7}$ and $\overline{C9}$ are OR'ed with their respective input bits. Also, the C bits in CUV128L and CUV128R are both channel status block bit 128, which is bit 0 of channel status byte 16.

Transparent Mode

In certain applications it is desirable to receive digital audio data with the CS8414 and retransmit with the CS8404A. In this case, channel status, user and validity information must pass through unaltered. For studio environments, AES recommends that signal timing synchronization be maintained throughout the studio. Frame synchronization of digital audio signals input to and output from a piece of equipment must be within ±5%.

The transparent mode of the CS8404A is selected by setting TRNPT (pin 24) high. In this mode, the CBL pin becomes an input, allowing direct connection of the outputs of the CS8414 to the inputs of the CS8404A as shown in Figure 18. The transmitter and receiver are synchronized by the FSYNC signal. CBL specifies the start of a new channel status block boundary, allowing the transmit block structure to be slaved to the block structure of the receiver. In the transparent mode, C, U, and V are now transmitted with the current audio sample as shown in Figure 17 (TRNPT high) and the dedicated channel status pins are ignored. When in the transparent mode, the propagation delay of data through the CS8404A is set so that the total propagation delay from the receive inputs of the CS8414 to the transmit outputs of the CS8404A is three frames.

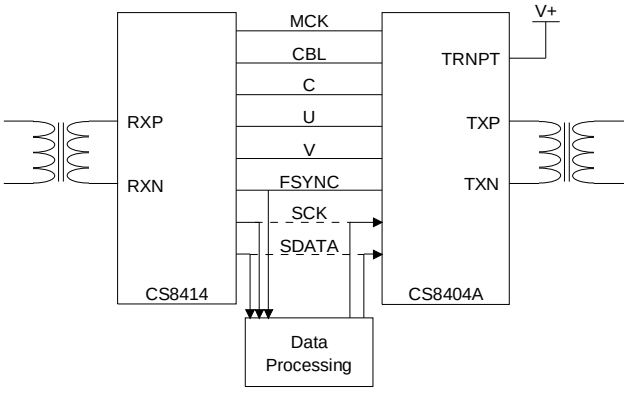


Figure 18. Transparent Mode Interface

When FSYNC is a word clock (Format 2), CBL is sampled when left C, U, V are sampled. When FSYNC is Left/Right, CBL is sampled when left C, U, V are sampled. The channel status block boundary is reset when CBL transitions from low to high (based on two successive samples of CBL). MCK for the CS8404A is normally expected to be 128 times the sample frequency, in the transparent mode MCK must be 256 Fs.

Professional Mode

Setting $\overline{PRO}$ low places the CS8404A in professional mode as shown in Figure 19. In professional mode, channel status bit 0 is transmitted as a one and bits 1, 2, 3, 4, 6, 7, and 9 can be controlled via dedicated pins. The pins are actually the inverse of the identified bit. For example, tying the $\overline{C1}$ pin low places a one in channel status bit 1. As shown in the Application Note (AN22), Overview of AES/EBU Digital Audio Interface Data Structures, $\overline{C1}$ indicates audio/non-audio; $\overline{C6}$ and $\overline{C7}$ determine the sample frequency; and $\overline{C9}$ allows the encoded channel mode to be stereophonic. EM1 and EM0 determine emphasis and encode $\overline{C2}$, $\overline{C3}$, $\overline{C4}$ as shown in Table 4. The dedicated channel status pins are read at the appropriate time and are logically OR'ed with data input on the channel status port, C. In Transparent Mode, these dedicated channel status pins are ignored and channel status bits are input at the C pin.

EM1	EM0	$\overline{C2}$	$\overline{C3}$	$\overline{C4}$
0	0	1	1	1
0	1	1	1	0
1	0	1	0	0
1	1	0	0	0

Table 4. Emphasis Encoding

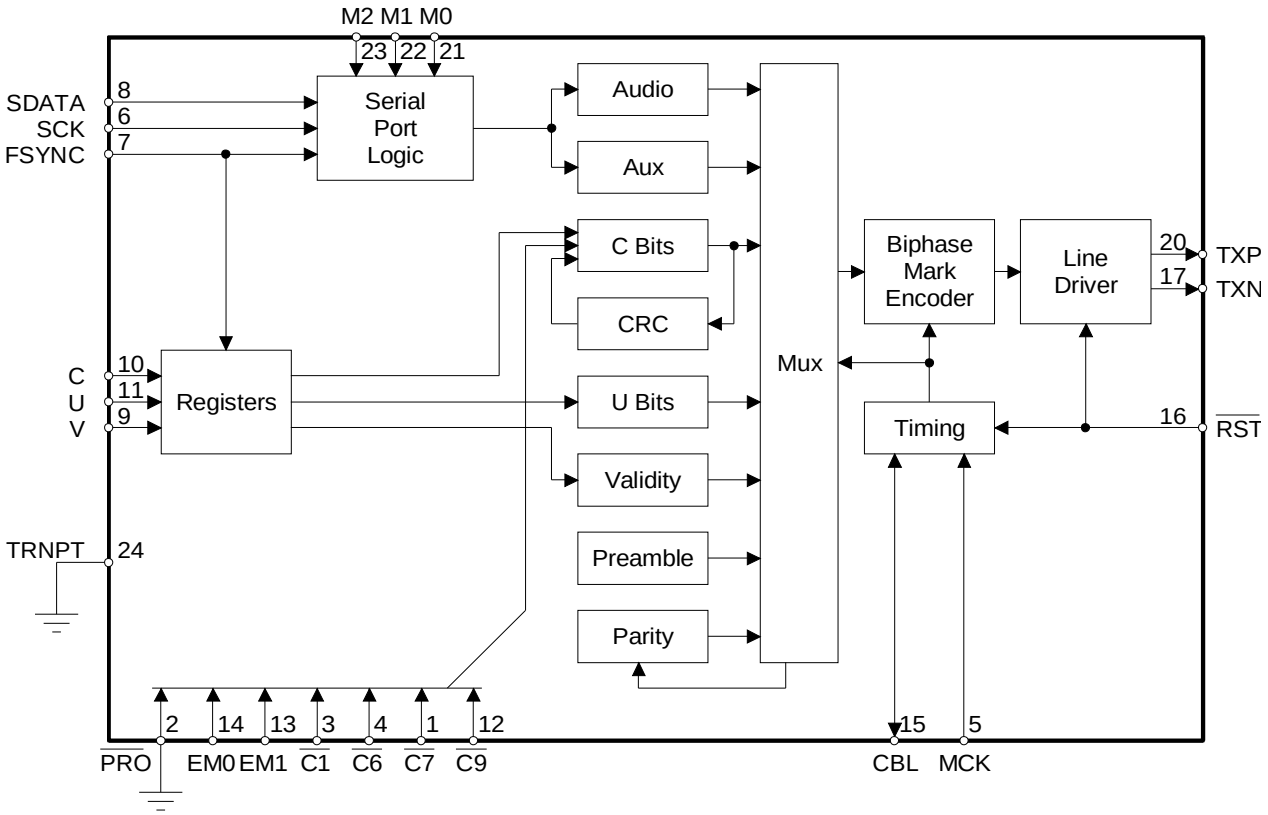


Figure 19. CS8404A Block Diagram - Professional Mode

The channel status data cyclic redundancy check character (C.S. byte 23) is always generated independently for channels A and B and is transmitted at the end of the channel status block.

Data should not be input through the channel status port, C, during the CRCC byte time frame, since inputs on C are logically OR'ed with internally generated data.

Consumer Mode

Setting $\overline{PRO}$ high places the CS8404A in consumer mode which redefines the pins as shown in Figure 20. In consumer mode, channel status bit 0 is transmitted as a zero and channel status bits 2, 3, 8, 9, 15, 24, and 25 are controlled via dedicated pins. The pins are actually the inverse of the bit so if pin $\overline{C2}$ is tied high, channel status bit 2 will be transmitted as a zero. Also, FC0 and FC1 are encoded versions of channel status bits 24 and 25, which define the sample frequency. When FC0 and FC1 are both high, the part is placed in a CD submode which activates the CD subcode port. This submode is described in detail in the next section. Table 5 describes the encoding of $\overline{C24}$ and $\overline{C25}$ through the FC1 and FC0 pins. According to AES/EBU standards, $\overline{C2}$ is copy prohibit/permit, $\overline{C3}$ specifies pre-emphasis, $\overline{C8}$ and $\overline{C9}$ define the category code, and $\overline{C15}$ identifies the generation status of the transmitted material (i.e. first generation, second generation).

FC1	FC0	$\overline{C24}$	$\overline{C25}$	Comments
0	0	0	0	44.1 kHz
0	1	0	1	48.0 kHz
1	0	1	1	32.0 kHz
1	1	0	0	44.1 kHz, CD Mode

Table 5. Sample Frequency Encoding

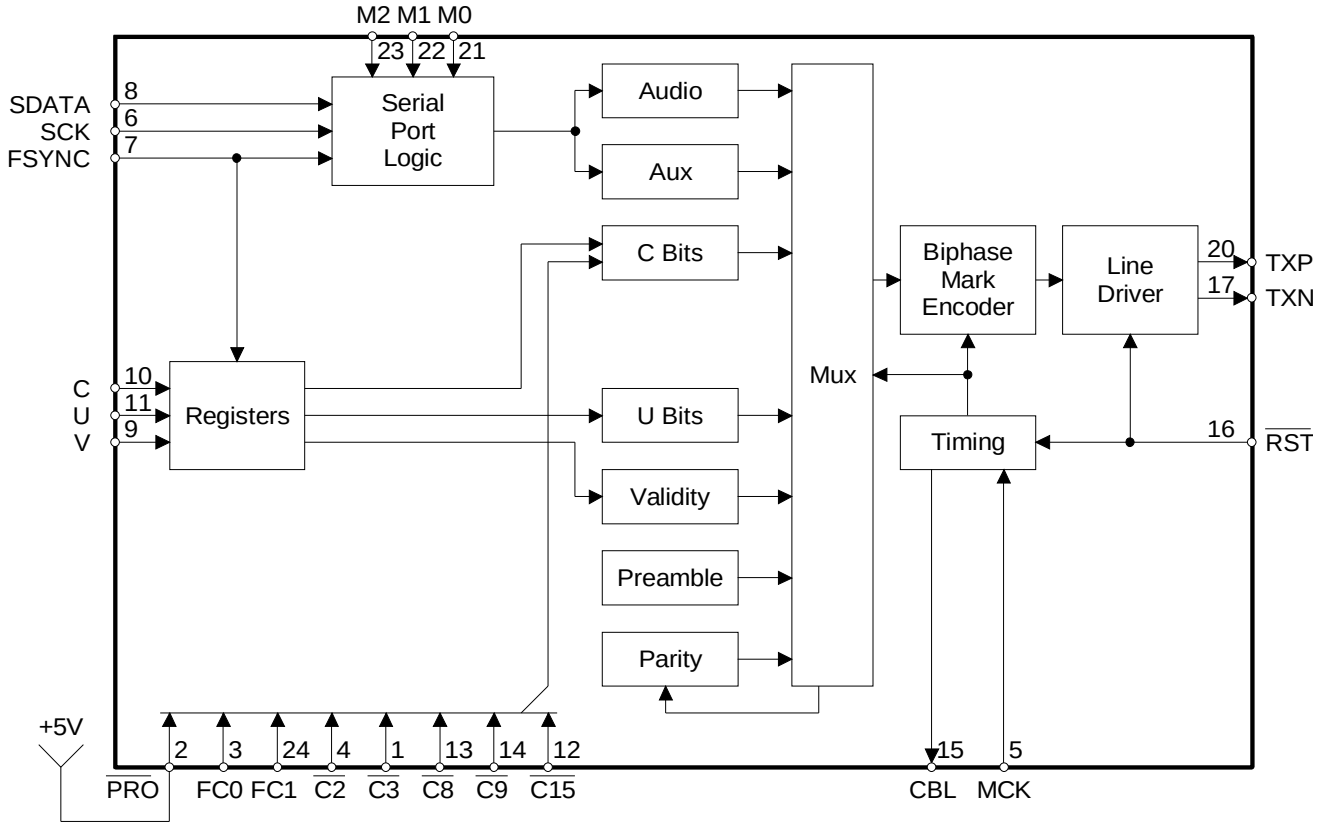


Figure 20. CS8404A Block Diagram - Consumer Mode

Consumer - CD Submode

The consumer CD submode is invoked by placing the part in consumer mode ($\overline{PRO}$ = high) and setting both FC1 and FC0 high. This mode redefines some of the pins for a CD subcode port as shown in Figure 21. The CD subcode port pins, SBF and SBC, replace the C and CBL pins respectively. The user data input, U, becomes the CD subcode input. Figure 22 describes the timing for the CD subcode port. When SBF is low, SBC becomes active, clocking in the subcode bits. SBF goes high for one SCK period, one half SCK period after the active edge of FSYNC for all formats (except format 4, which will be one and a half SCK periods after the active edge of FSYNC). SBF high for more than 16 SBC periods indicates the start of a subcode block. The first, third, and fourth Q bits after the start of a subcode block become channel status bits 5, 2, and 3 respectively. Channel status bits are set by the dedicated pins; the category code is forced to CD.

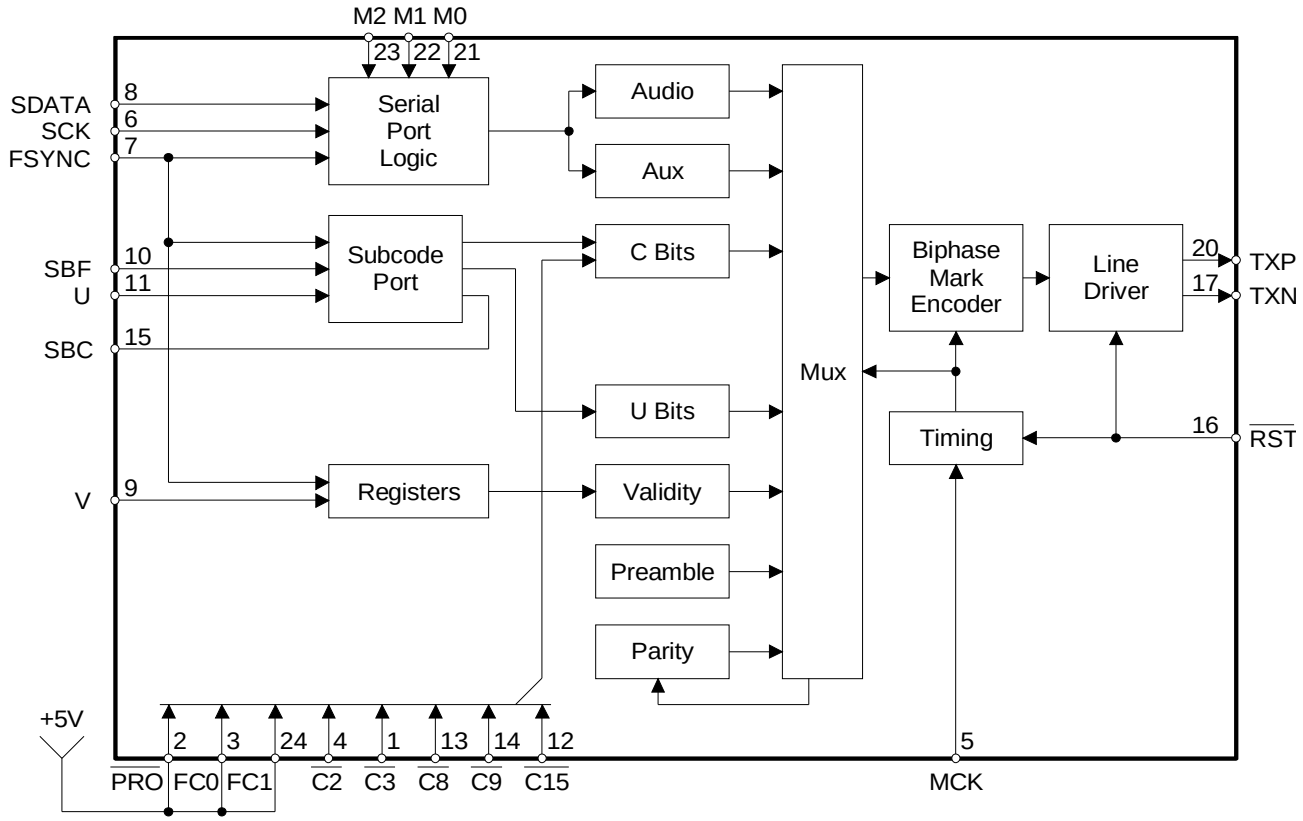


Figure 21. CS8404A Block Diagram - Consumer Mode, CD Submode

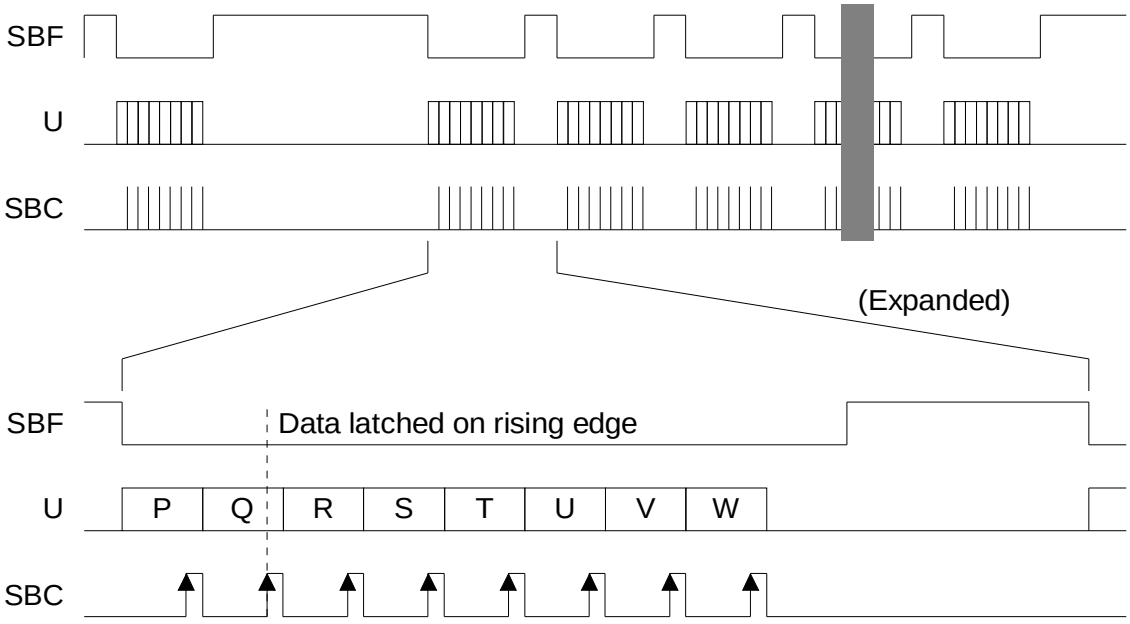
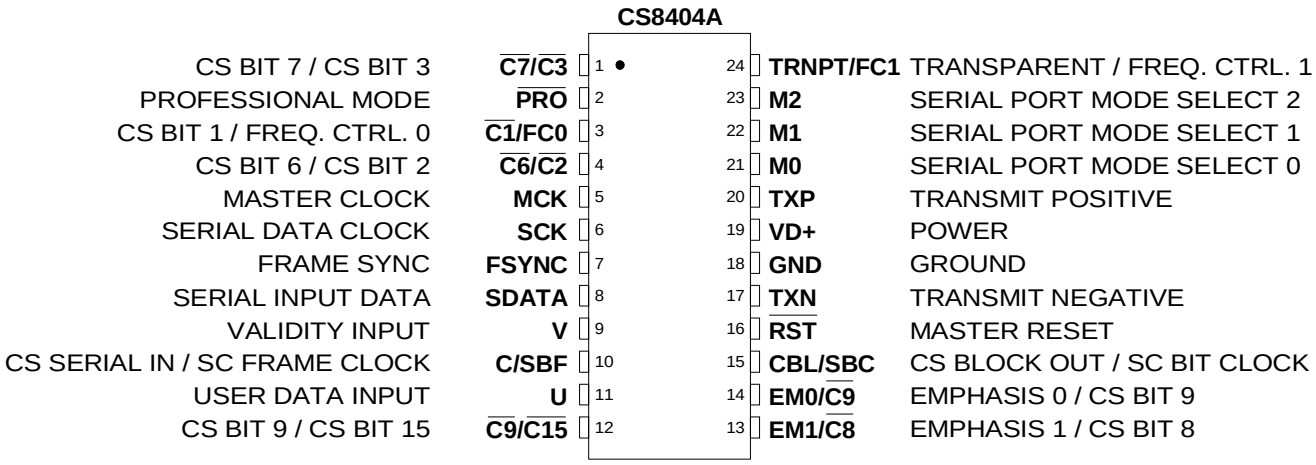


Figure 22. CD Subcode Port Timing

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 19.

Positive supply for the digital section. Nominally +5 volts.

GND - Ground, PIN 18.

Ground for the digital section.

Audio Input Interface

SCK - Serial Clock, PIN 6.

Serial clock for SDATA pin which can be configured (via the M0, M1, and M2 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will contain 32 clocks for every audio sample. As an input, it does not need to be continuous and can be up to 15 MHz.

FSYNC - Frame Sync, PIN 7.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, and M2 pins.

SDATA - Serial Data, PIN 8.

Audio data serial input pin.

M0, M1, M2 - Serial Port Mode Select, PINS 21, 22, 23.

Selects the format of FSYNC and the sample edge of SCK with respect to SDATA.

Control Pins

$\overline{\text{RST}}$ - Master Reset, PIN 16.

When low, all internal counters are reset and the line drivers are disabled, pulling low.

V - Validity, PIN 9.

Validity bit serial input port. This bit is defined according to the digital audio standards wherein V=0 signifies the audio signal is suitable for conversion to analog. V=1 signifies the audio signal is not suitable for conversion to analog, i.e. invalid. V is sampled once per subframe

U - User Bit, PIN 11.

User bit serial input port is sampled once per subframe.

$\overline{\text{PRO}}$ - Professional/Consumer Select, PIN 2.

Selects between professional mode ($\overline{\text{PRO}}$ low) and consumer mode ($\overline{\text{PRO}}$ high). This pin defines the functionality of the next seven pins. $\overline{\text{PRO}}$ must be low for Transparent Mode, but will have no effect on the channel status bits.

$\overline{\text{C9}}$/$\overline{\text{C15}}$ - Channel Status Bit 9 / Channel Status Bit 15, PIN 12.

In professional mode, $\overline{\text{C9}}$ is the inverse of channel status bit 9 (bit 1 of byte 1). In consumer mode, $\overline{\text{C15}}$ is the inverse of channel status bit 15 (bit 7 of byte 1). $\overline{\text{C9}}$/$\overline{\text{C15}}$ are ignored in Transparent Mode.

EM0/$\overline{\text{C9}}$ - Emphasis 0 / Channel Status Bit 9, PIN 14.

In professional mode, EM0 and EM1 encode channel status bits 2, 3, and 4. In consumer mode, $\overline{\text{C9}}$ is the inverse of channel status bit 9 (bit 1 or byte 1). EMO/$\overline{\text{C9}}$ are ignored in Transparent Mode.

EM1/$\overline{\text{C8}}$ - Emphasis 1 / Channel Status Bit 8, PIN 13.

In professional mode, EM0 and EM1 encode channel status bits 2, 3, and 4. In consumer mode, $\overline{\text{C8}}$ is the inverse of channel status bit 8 (bit 0 of byte 1). EM1/$\overline{\text{C8}}$ are ignored in Transparent Mode.

$\overline{\text{C7}}$/$\overline{\text{C3}}$ - Channel Status Bit 7 / Channel Status Bit 3, PIN 1.

In professional mode, $\overline{\text{C7}}$ is the inverse of channel status bit 7. In consumer mode, $\overline{\text{C3}}$ is the inverse of channel status bit 3. $\overline{\text{C7}}$/$\overline{\text{C3}}$ are ignored in Transparent Mode.

$\overline{\text{C6}}$/$\overline{\text{C2}}$ - Channel Status Bit 6 / Channel Status Bit 2, PIN 4.

In professional mode, $\overline{\text{C6}}$ is the inverse of channel status bit 6. In consumer mode, $\overline{\text{C2}}$ is the inverse of channel status bit 2. $\overline{\text{C6}}$/$\overline{\text{C2}}$ are ignored in Transparent Mode.

$\overline{\text{C1}}$/FC0 - Channel Status Bit 1 / Frequency Control 0, PIN 3.

In professional mode, $\overline{\text{C1}}$ is the inverse of channel status bit 1. In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25 (bits 0 and 1 of byte 3). When FC0 and FC1 are both high, CD mode is selected. $\overline{\text{C1}}$/FC0 are ignored in Transparent Mode.

TRNPT/FC1 - Transparent Mode / Frequency Control 1, PIN 24.

In professional mode, setting TRNPT low selects normal operation & CBL is an output. Setting TRNPT high, allows the CS8404A to be connected directly to a CS8414. In transparent mode, CBL is an input & MCK must be at 256 Fs. In consumer mode, FC0 and FC1 are encoded versions of channel status bits 24 and 25. When FC0 and FC1 are both high, CD mode is selected.

C/SBF - Channel Status Serial Input / Subcode Frame Clock, PIN 10.

In professional and consumer modes this pin is the channel status serial input port. In CD mode this pin inputs the CD subcode frame clock.

CBL/SBC - Channel Status Block Output / Subcode Bit Clock, PIN 15.

In professional and consumer modes, the channel status block output is high for the first 16 bytes of channel status. In CD mode, this pin outputs the subcode bit clock.

Transmitter Interface

MCK - Master Clock, PIN 5.

Clock input at 128x Fs the sample frequency which defines the transmit timing. In transparent mode, MCK must be 256x Fs.

TXP, TXN - Differential Line Drivers, PINS 20, 17.

RS422 compatible line drivers. Drivers are pulled to low when part is in reset state.

APPENDIX A: RS422 DRIVER INFORMATION

The RS422 drivers on the CS8403A and CS8404A are designed to drive both the professional and consumer interfaces. The AES/EBU specification for professional/broadcast use calls for a 110 Ω source impedance and a balanced drive capability. Since the transmitter impedance is very low, a 110 Ω resistor should be placed in series with one of the transmit pins. (A 110 Ω resistor in parallel with the transformer would, with the receiver impedance of 110 Ω, provide a 55 Ω load to the part which is too low.) The specifications call for a balanced output drive of 2-7 volts peak-to-peak into a 110 Ω load with no cable attached. Using the circuit in Figure A1, the output of the transformer is short-circuit protected, has the proper source impedance, and provides a 5 volt peak-to-peak signal into a 110 Ω load. Lastly, the two output pins should be attached to an XLR connector with male pins and a female shell, and with pin 1 of the connector grounded.

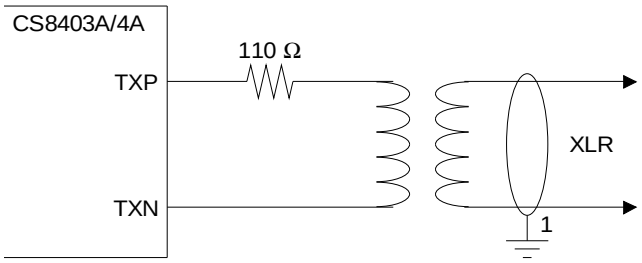


Figure A1. Professional Output Circuit

In the case of consumer use, the specifications call for an unbalanced drive circuit with an output impedance of 75 Ω and a output drive level of 0.5 volts peak-to-peak ±20% when measured across a 75 Ω load using no cable. The circuit shown in Figure A2 only uses the TXP pin and provides the proper output impedance and drive level using standard 1% resistors. The connector for consumer would be an RCA phono socket. This circuit is also short circuit protected.

The TXP pin may be used to drive TTL or CMOS gates as shown in Figure A3. This circuit may be used for optical connectors for digital audio since they are usually TTL compatible. This circuit is also useful when driving multiple digital audio outputs since RS422 line drivers have TTL interfaces.

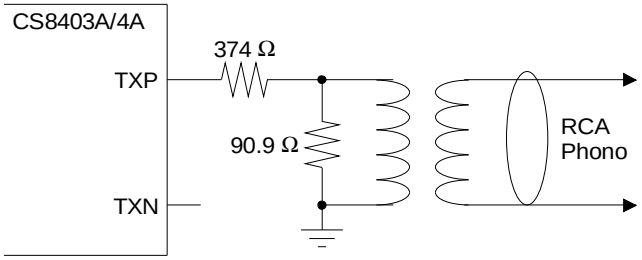


Figure A2. Consumer Output Circuit

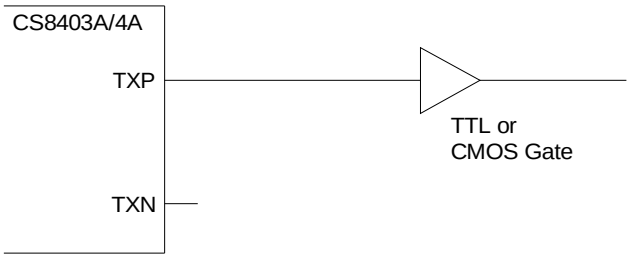


Figure A3. TTL/CMOS Output Circuit

The transformer should be capable of operating from 1.5 to 14 MHz, which is the audio data rate of 25 kHz to 108 kHz after biphase-mark encoding. Transformers provide isolation from ground loops, 60Hz noise, and common mode noise and interference. One of the important considerations when choosing transformers is minimizing shunt capacitance between primary and secondary windings. The higher the shunt capacitance, the lower the isolation between primary and secondary, and the more coupling of high frequency energy. This energy appears in the form of common mode noise on the receive side ground and has the potential to degrade analog performance. Therefore, for best performance, shielded transformers optimized for minimum shunt capacitance should be used. The following are a few typical transformers:

Pulse Engineering
Telecom Products Group
7250 Convoy Ct.
San Diego, CA 92111

(619) 268-2400
Part Number: PE65612

Schott Corporation
1000 Parkers Lane Rd.
Wayzata, MN 55391
(612) 475-1173
FAX (612) 475-1786
Part Number:
67125450 - compatible with Pulse
67128990 - lower cost
67129000 - surface mount
67129600 - single shield

Scientific Conversions Inc.
42 Truman Drive
Novato, CA. 94947
(415) 892-2323
Part Number:
SC916-01 - single shield
SC916-02 - surface mount

APPENDIX B: MCK AND FSYNC RELATIONSHIP

FSYNC should be derived either directly or indirectly from MCK. The indirect case could be a DSP, providing FSYNC through its serial port, using the same master oscillator that generates MCK. In either case, FSYNC's relationship to MCK is fixed and does not move. Since this appendix provides information on what would happen if FSYNC did move with respect to MCK, it does not apply to the majority of users.

All internal timing is derived from MCK. On the CS8404A, MCK is always 128xFs. On the CS8403A, the external MCK is programmable and is initially divided to 128xFs before being used by the part. The internal clock IMCK used in the following discussion is always 128xFs regardless of the external MCK pin.

After $\overline{\text{RST}}$, the CS8403A and CS8404A synchronize the internal timing to the audio data port, more specifically FSYNC, to guarantee that channel A is left channel data and channel B is right channel data as per the AES/EBU specification. If FSYNC moves with respect to IMCK, the transmitter could lose synchronization, which causes an internal reset.

Figure B1 shows the structure of the serial port input, to the transmitter output. The audio data is serially shifted into R1. PLD is an internal signal that parallel loads R1 into the R2 buffer, and, at the same time, the C, U, and V bits are latched. On the CS8403A, the C, U, and V bits are held in RAM, whereas on the CS8404A, they are latched from external pins. The PLD signal rises on the first SCK edge that can latch data. This is coincident with the latching of the MSB of audio data in MSB-first, left-justified modes. PLD stays high for one SCK period. In the CS8404A section, the arrows on SCK in Figure 16 indicate when PLD goes high. Also, SBC in the CS8404A CD submode is an external version of PLD gated by the SBF input.

When the part is finished transmitting the preamble of a sub-frame, the internal signal LDS rises to parallel-load R2 into R3 for transmission. After $\overline{\text{RST}}$, the part synchronizes the audio port to IMCK as shown in Figure B2. Since PLD is based on FSYNC and LDS is based on IMCK, if FSYNC moves with respect to IMCK until PLD and LDS occur at the same time, the data would not be properly loaded into R3. If LDS and PLD overlap, an internal reset is initiated causing the timing to return to the initial state shown in Figure B2.

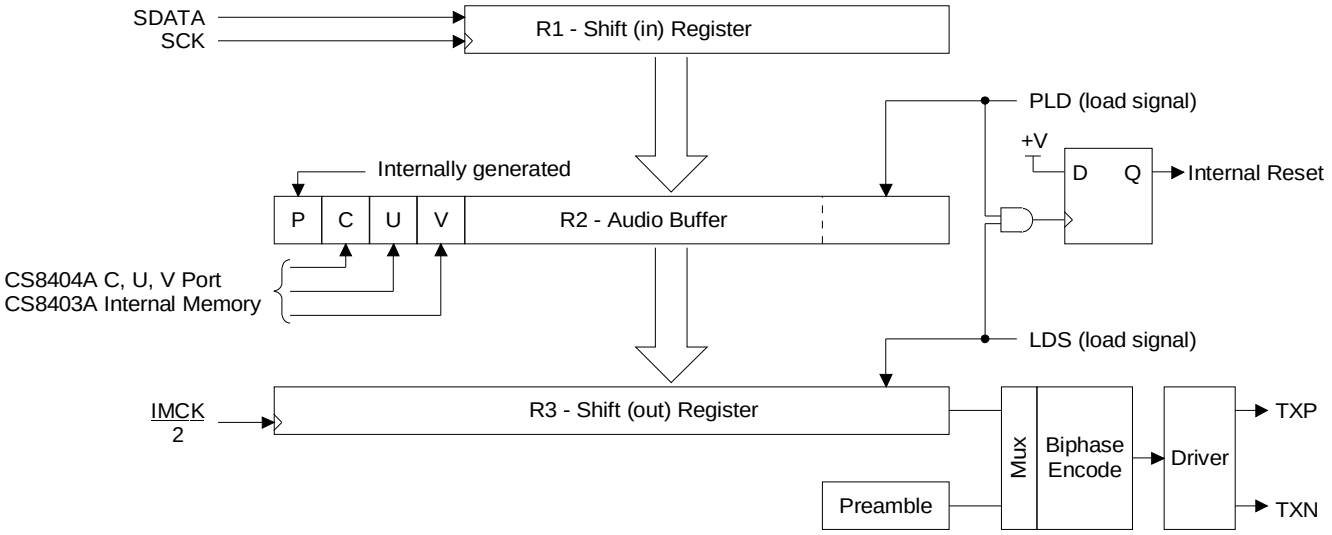


Figure B1. Serial Port-to-Transmitter Block Diagram

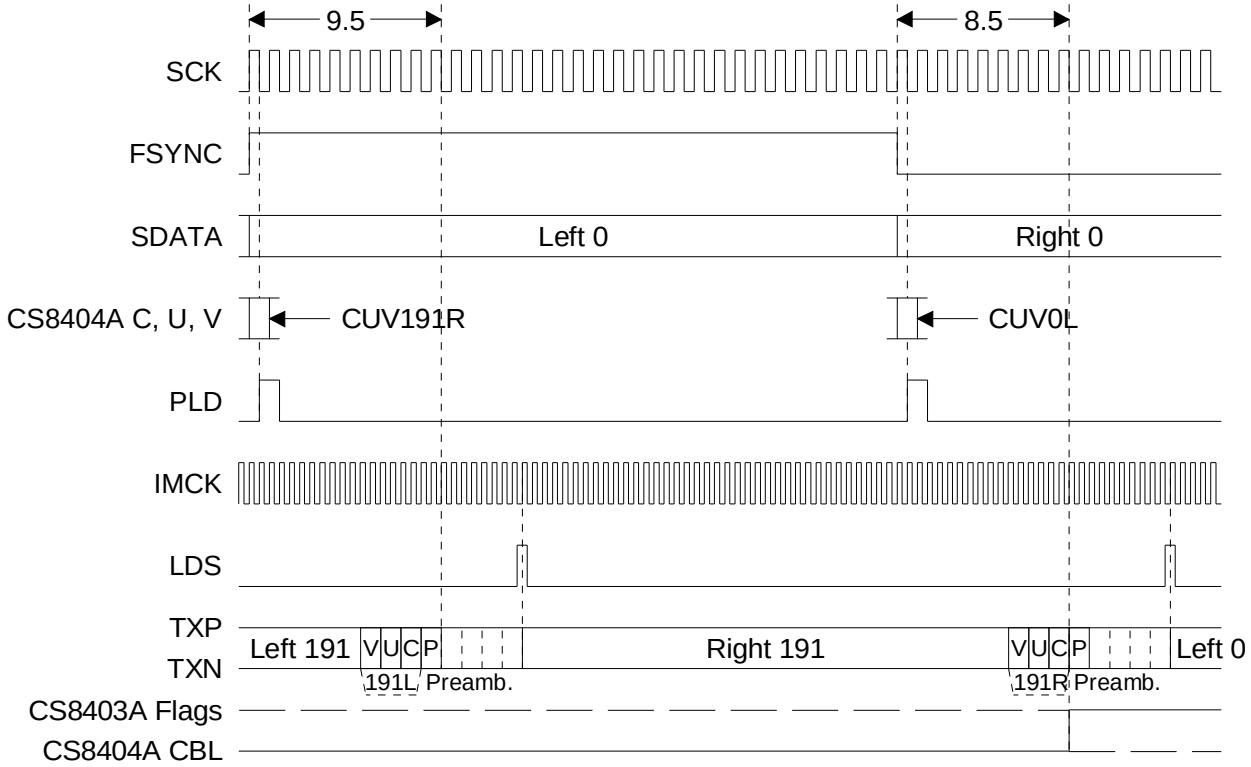
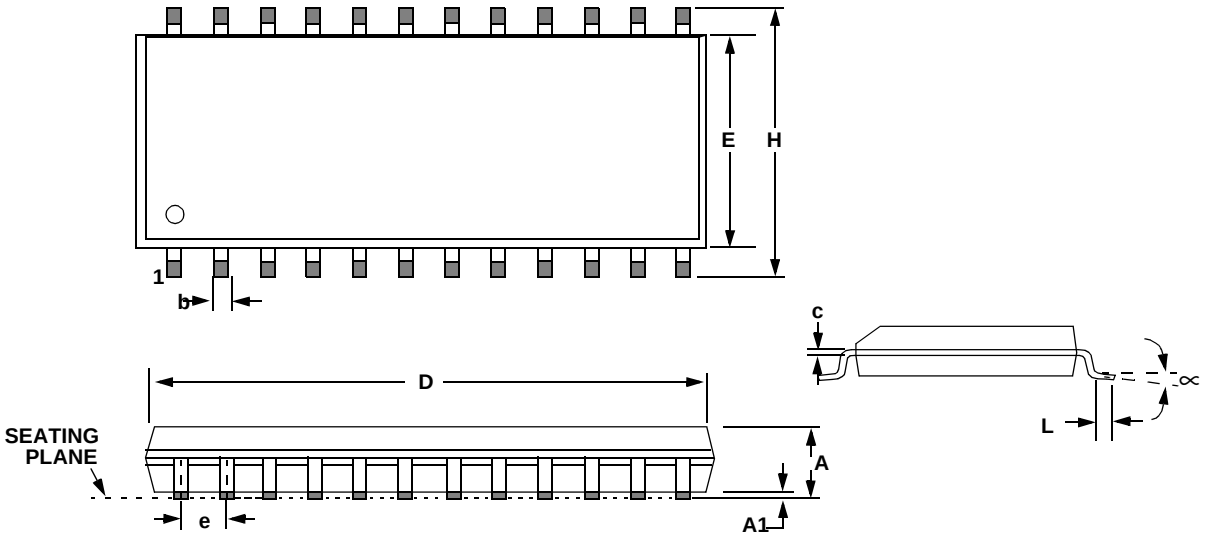


Figure B2. Serial Port-to-Transmitter Timing (slave mode)

24L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°