HA-5004/883

July 1998

100MHz Current Feedback Amplifier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Slew Rate . . . . . 1000V/μs (Min) 1200V/μs (Typ)**
- **Output Current . . . . . ±80mA (Min) ±100mA (Typ)**
- **Drives . . . . . ±8.0V into 100Ω (Min) ±9.5V into 100Ω (Typ)**
- **V_{SUPPLY} . . . . . ±5V to ±18V**
- **Thermal Overload Protection and Output Flag**
- **Bandwidth Nearly Independent of Gain**
- **Output Enable/Disable**

Applications

- **Unity Gain Video/Wideband Buffer**
- **Video Gain Block**
- **High Speed Peak Detector**
- **Fiber Optic Transmitters**
- **Zero Insertion Loss Transmission Line Drivers**
- **Current to Voltage Converter**
- **Radar Systems**

Description

The HA-5004/883 current feedback amplifier is a video/wideband amplifier optimized for low gain applications. The design is based on current-mode feedback which allows the amplifier to achieve higher closed loop bandwidth than voltage-mode feedback operational amplifiers. Since feedback is employed, the HA-5004/883 can offer better gain accuracy and lower distortion than open loop buffers. Unlike conventional op amps, the bandwidth and rise time of the HA-5004/883 are nearly independent of closed loop gain. The 100MHz bandwidth at unity gain reduces to only 65MHz at a gain of 10. The HA-5004/883 may be used in place of a conventional op amp with a significant improvement in speed power product.

Several features have been designed in for added value. A thermal overload feature protects the part against excessive junction temperature by shutting down the output. If this feature is not needed, it can be inhibited via a TTL input (TOI). A TTL chip enable/disable ($\overline{OE}$) input is also provided; when the chip is disabled its output is high impedance. Finally, an open collector output flag ($\overline{TOL}$) is provided to indicate the status of the chip. The status flag goes low to indicate when the chip is disabled due to either the internal Thermal Overload shutdown or the external disable.

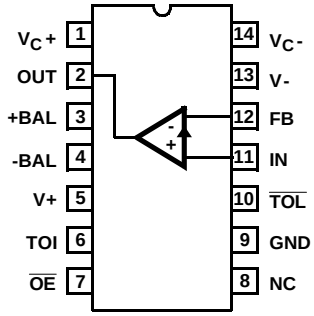
In order to maximize bandwidth and output drive capacity, internal current limiting is not provided. However, current limiting may be applied via the V_C+ and V_C- pins which provide power separately to the output stage.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
HA1-5004/883	-55 to +125	14 Lead CerDIP

Pinout

HA-5004/883
(CERDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Spec Number **511053-883**
File Number **3706.1**

Absolute Maximum Ratings

Voltage between V+ and V- Terminals 40V
Differential Input Voltage 5V
Voltage at Either Input Terminal . . . . . V+ to V-
Peak Output Current Pulsed at 1ms ≤ 10% Duty Cycle . . . . ±300mA
Continuous Output Current . . . . . ±120mA rms
Junction Temperature (T_J) . . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating . . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	73°C/W	18°C/W

Package Power Dissipation Limit at +75°C
CerDIP Package 1.37W
Package Power Dissipation Derating Factor Above +75°C
CerDIP Package . . . . . 13.7mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C $R_L \geq 100\Omega$
Operating Supply Voltage . . . . . ±12V to ±15V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = □V_{C}+ = +15V, V- = □V_{C}- = -15V, R_L = 100Ω, A_V = +1, R_F = 250Ω, $\overline{OE}$ = 0.8V, TOI = 0.8V or 2.0V,
Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{IN} = 0V	1	+25°C	-2.5	2.5	mV
			2, 3	+125°C, -55°C	-20	20	mV
Input Bias Current	$+I_B$	V_{IN} = 0V (Note 1)	1	+25°C	-5	5	µA
			2, 3	+125°C, -55°C	-20	20	µA
DC Gain Error (Small Signal)	SSGE	V_{IN} = ±100mV, R_L = 100Ω	1	+25°C	-	0.43	%
			2, 3	+125°C, -55°C	-	0.75	%
DC Gain Error (Large Signal)	$LSGE_1$	V_{IN} = ±5.0V, R_L = 1kΩ	1	+25°C	-	0.43	%
			2, 3	+125°C, -55°C	-	0.75	%
	$LSGE_2$	V_{IN} = ±10V, R_L = 1kΩ	1	+25°C	-	0.43	%
			2, 3	+125°C, -55°C	-	0.75	%
DC Voltage Gain	A_V	For All Gain Error Conditions (Note 2)	1	+25°C	233	-	V/V
			2, 3	+125°C, -55°C	133	-	V/V
DC Transimpedance	A_R	For All Gain Error Conditions (Note 3)	1	+25°C	58	-	V/mA
			2, 3	+125°C, -55°C	33	-	V/mA
Output Voltage Swing	$\pm V_{OUT1}$	V_{IN} = ±15V, R_L = 1kΩ	1	+25°C	11.5	-11.5	V
			2, 3	+125°C, -55°C	10.5	-10.5	V
	$\pm V_{OUT2}$	V_{IN} = ±10V, R_L = 100Ω	1	+25°C	9.0	-9.0	V
			2, 3	+125°C, -55°C	8.0	-8.0	V
Output Current	$\pm I_{OUT}$	V_{IN} = ±10V, R_L = 100Ω	1	+25°C	90	-90	mA
			2, 3	+125°C, -55°C	80	-80	mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V+ = ▯V_C+ = +15V, V- = ▯V_C- = -15V, R_L = 100Ω, A_V = +1, R_F = 250Ω, $\overline{OE}$ = 0.8V, TOI = 0.8V or 2.0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logic Input Voltage	V_{IH}	Pins $\overline{OE}$, TOI (Note 4)	1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
	V_{IL}	Pins $\overline{OE}$, TOI	1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
Power Supply Rejection Ratio	$PSRR_1$	V+ = +10V, +20V V- = -15V	1	+25°C	50	-	dB
			2, 3	+125°C, -55°C	50	-	dB
	$PSRR_2$	V- = -10V, -20V V+ = +15V	1	+25°C	50	-	dB
			2, 3	+125°C, -55°C	50	-	dB
Power Supply Current	$+I_{CC}$	V_{IN} = 0V, R_L = 1kΩ	1	+25°C	-	16	mA
			2, 3	+125°C, -55°C	-	22	mA
	$-I_{CC}$	V_{IN} = 0V, R_L = 1kΩ	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-22	-	mA

NOTES:

1. Inverting (FB) input is a low impedance point; Bias Current and Offset Current are not specified for this terminal.
2. DC Voltage Gain = $\frac{1}{\text{Gain Error}}$, for all Gain Error conditions.
3. DC Transimpedance = $\frac{R_F}{\text{Gain Error}}$, R_F = 250Ω, for all Gain Error conditions.
4. Please refer to the Truth Table in the Applications Information section.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Specifications in Table 3

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V+ = ▯V_C+ = +15V, V- = ▯V_C- = -15V, R_L = 1kΩ, A_V = +1, R_F = 250Ω, $C_L \leq$ 10pF, $\overline{OE}$ = 0.8V, TOI = 0.8V or 2.0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = 0V to +10V	1, 2	+25°C	1000	-	V/µs
	-SR	V_{OUT} = 0V to -10V	1, 2	+25°C	1000	-	V/µs
Rise and Fall Time	T_R	V_{OUT} = 0V to +200mV,	1, 2	+25°C	-	7.0	ns
	T_F	V_{OUT} = 0V to -200mV	1, 2	+25°C	-	7.0	ns
Full Power Bandwidth	FPBW	V_{PEAK} = 2V	1, 3	+25°C	79.5	-	MHz

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V+ = |V_C+ = +15V, V- = |V_C- = -15V, R_L = 1kΩ, A_V = +1, R_F = 250Ω, C_L ≤ 10pF, $\overline{OE}$ = 0.8V, TOI = 0.8V or 2.0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Power Consumption	PC	V_{IN} = 0V	1, 4	-55°C to +125°C	-	660	mW

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Measured between 10% and 90% points.
3. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
4. Power Consumption based upon Quiescent Supply Current test maximum.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
63 x 93 x 19 mils ± 1 mils
1600 x 2370 x 483µm ± 25.4µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride (Si3N4) over (Silox, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
$6.6 \times 10^4 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up): V_{EE}

TRANSISTOR COUNT: 64

PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5004/883