Data Sheet | January 25, 2006 | FN7312.5

450MHz Differential Twisted-Pair Drivers

The EL5173 and EL5373 are single and triple high bandwidth amplifiers with a fixed gain of 2. They are primarily targeted for applications such as driving twisted-pair lines in component video applications. The inputs can be in either single-ended or differential form but the outputs are always in differential form.

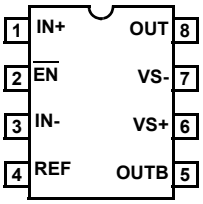
The output common mode level for each channel is set by the associated REF pin, which have a -3dB bandwidth of over 190MHz. Generally, these pins are grounded but can be tied to any voltage reference.

All outputs are short circuit protected to withstand temporary overload condition.

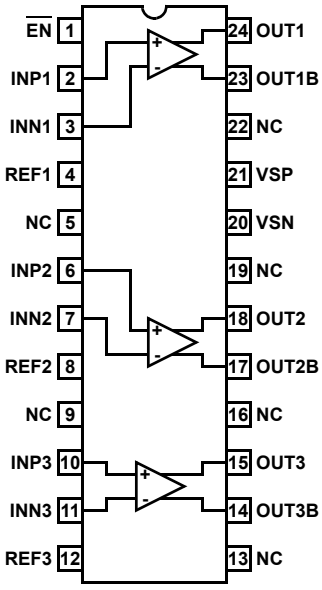
The EL5173 and EL5373 are specified for operation over the full -40°C to +85°C temperature range.

Pinouts

EL5173
(8 LD SO, MSOP)
TOP VIEW



EL5373
(24 LD QSOP)
TOP VIEW



Features

- Fully differential inputs and outputs
- Differential input range ±2.3V
- 450MHz 3dB bandwidth at fixed gain of 2
- 900V/µs slew rate (EL5173)
- 1100V/µs slew rate (EL5373)
- Single 5V or dual ±5V supplies
- 40mA maximum output current
- Low power - 12mA per channel
- Pb-free plus anneal available (RoHS compliant)

Applications

- Twisted-pair drivers
- Differential line drivers
- VGA over twisted-pairs
- ADSL/HDSL drivers
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5173IS	5173IS	-	8 Ld SO	MDP0027
EL5173IS-T7	5173IS	7”	8 Ld SO	MDP0027
EL5173IS-T13	5173IS	13”	8 Ld SO	MDP0027
EL5173ISZ (Note)	5173ISZ	-	8 Ld SO (Pb-free)	MDP0027
EL5173ISZ-T7 (Note)	5173ISZ	7”	8 Ld SO (Pb-free)	MDP0027
EL5173ISZ-T13 (Note)	5173ISZ	13”	8 Ld SO (Pb-free)	MDP0027
EL5173IY	i	-	8 Ld MSOP	MDP0043
EL5173IY-T7	i	7”	8 Ld MSOP	MDP0043
EL5173IY-T13	i	13”	8 Ld MSOP	MDP0043
EL5173IYZ (Note)	BAAYA	-	8 Ld MSOP (Pb-free)	MDP0043
EL5173IYZ-T7 (Note)	BAAYA	7”	8 Ld MSOP (Pb-free)	MDP0043
EL5173IYZ-T13 (Note)	BAAYA	13”	8 Ld MSOP (Pb-free)	MDP0043
EL5373IU	EL5373IU	-	24 Ld QSOP	MDP0040
EL5373IU-T7	EL5373IU	7”	24 Ld QSOP	MDP0040
EL5373IU-T13	EL5373IU	13”	24 Ld QSOP	MDP0040
EL5373IUZ (Note)	EL5373IUZ	-	24 Ld QSOP (Pb-free)	MDP0040
EL5373IUZ-T7 (Note)	EL5373IUZ	7”	24 Ld QSOP (Pb-free)	MDP0040
EL5373IUZ-T13 (Note)	EL5373IUZ	13”	24 Ld QSOP (Pb-free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S+ to V_S-) 12.6V
Supply Voltage Slew Rate . . . . . 1V/µs max.
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +135°C
Recommended Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, T_A = 25°C, V_{IN} = 0V, R_{LD} = 200Ω, C_{LD} = 1pF, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth			450		MHz
BW	±0.1dB Bandwidth			60		MHz
SR	Slew Rate - EL5173	V_{OUT} = $2V_{P-P}$, 20% to 80%	750	900		V/µs
	Slew Rate - EL5373	V_{OUT} = $2V_{P-P}$, 20% to 80%	900	1100		V/µs
T_{STL}	Settling Time to 0.1%	V_{OUT} = $2V_{P-P}$		10		ns
OS	Overshoot	V_{ODP-P} = 2V		10		%
T_{OVR}	Output Overdrive Recovery Time			10		ns
V_{REF}BW (-3dB)	V_{REF} -3dB Bandwidth	A_V =1, C_{LD} = 2.7pF		190		MHz
V_{REF}SR+	V_{REF} Slew Rate - Rise	V_{OUT} = $2V_{P-P}$, 20% to 80%		200		V/µs
V_{REF}SR-	V_{REF} Slew Rate - Fall	V_{OUT} = $2V_{P-P}$, 20% to 80%		125		V/µs
V_N	Input Voltage Noise	f = 10kHz		25		nV/√Hz
HD2	Second Harmonic Distortion	V_{OUT} = $2V_{P-P}$, 5MHz		84		dBc
HD2	Second Harmonic Distortion	V_{OUT} = $2V_{P-P}$, 20MHz		71		dBc
HD3	Third Harmonic Distortion	V_{OUT} = $2V_{P-P}$, 5MHz		62		dBc
HD3	Third Harmonic Distortion	V_{OUT} = $2V_{P-P}$, 20MHz		53		dBc
dG	Differential Gain at 3.58MHz	R_{LD} = 300Ω, A_V = 2		0.05		%
dθ	Differential Phase at 3.58MHz	R_{LD} = 300Ω, A_V = 2		0.08		°
e_S	Channel Separation - for EL5373 only	at 1MHz		90		dB
INPUT CHARACTERISTICS						
V_{OS}	Input Referred Offset Voltage			±3	±30	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB})	EL5173	-21	-11	-5	µA
		EL5373	-21	-13	-5	µA
I_{REF}	INput Bias Current at REF		1	2.3	5	µA
Gain	Gain Accuracy	V_{IN} = ±1V	1.97	1.99	2.01	V
R_{IN}	Differential Input Resistance			150		kΩ
C_{IN}	Differential Input Capacitance			1		pF
DMIR	Differential Mode Input Range		±2	±2.3		V
CMIR+	Common Mode Positive Input Range at V_{IN}+, V_{IN}-		3.1	3.4		V
CMIR-	Common Mode Negative Input Range at V_{IN}+, V_{IN}-			-4.5	-4.2	V
V_{REFIN}+	Reference Input - Positive	V_{IN}+ = V_{IN}- = 0V	3.3	3.7		V

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $T_A = 25°C$, $V_{IN} = 0V$, $R_{LD} = 200\Omega$, $C_{LD} = 1pF$, Unless Otherwise Specified **(Continued)**

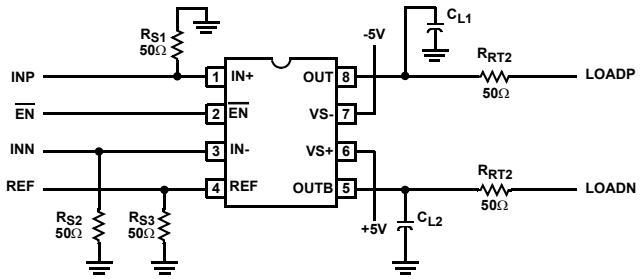
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REFIN}-$	Reference Input - Negative	$V_{IN}+ = V_{IN}- = 0V$		-3.3	-3	V
V_{REFOS}	Output Offset Relative to V_{REF}		-100	50	+100	mV
CMRR	Input Common Mode Rejection Ratio	$V_{IN} = \pm 2.5V$	60	80		dB
OUTPUT CHARACTERISTICS						
V_{OUT} (EL5173)	Positive Output Voltage Swing	$R_{LD} = 200\Omega$	3.3	3.67		V
	Negative Output Voltage Swing			-3.3	-3	V
V_{OUT} (EL5373)	Positive Output Voltage Swing	$R_{LD} = 200\Omega$	3.7	4		V
	Negative Output Voltage Swing			-3.7	-3.4	V
I_{OUT}(Max)	Maximum Output Current	$R_L = 10\Omega$ (EL5173)	±45	±55		mA
		$R_L = 10\Omega$ (EL5373)	±40	±50		mA
R_{OUT}	Output Impedance			60		mΩ
SUPPLY						
V_{SUPPLY}	Supply Operating Range	V_S+ to V_S-	4.75		11	V
$I_{S(ON)}$	Power Supply Current - Per Channel		9	12	14	mA
$I_{S(OFF)}+$ (EL5173)	Positive Power Supply Current - Disabled	$\overline{EN}$ pin tied to 4.8V	60	80	100	µA
$I_{S(OFF)}-$ (EL5173)	Negative Power Supply Current - Disabled		-150	-120	-90	µA
$I_{S(OFF)}+$ (EL5373)	Positive Power Supply Current - Disabled	$\overline{EN}$ pin tied to 4.8V	0.5	2	10	µA
$I_{S(OFF)}-$ (EL5373)	Negative Power Supply Current - Disabled		-150	-120	-90	µA
PSRR	Power Supply Rejection Ratio	V_S from ±4.5V to ±5.5V	60	73		dB
ENABLE						
t_{EN}	Enable Time			100		ns
t_{DS}	Disable Time			1.2		µs
V_{IH}	$\overline{EN}$ Pin Voltage for Power-Up				V_S+ -1.5	V
V_{IL}	$\overline{EN}$ Pin Voltage for Shut-Down		V_S+ -0.5			V
I_{IH-EN}	$\overline{EN}$ Pin Input Current High - Per Channel	At $V_{EN} = 5V$		40	60	µA
I_{IL-EN}	$\overline{EN}$ Pin Input Current Low - Per Channel	At $V_{EN} = 0V$	-5	-2.5		µA

Pin Descriptions

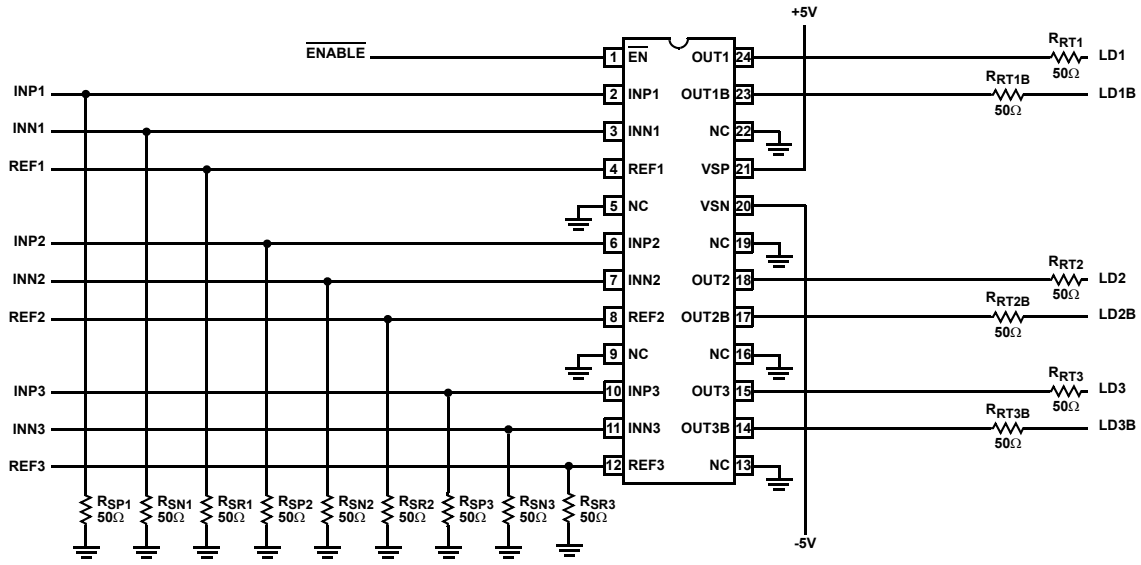
EL5173	EL5373	PIN NAME	PIN FUNCTION
1	2, 6, 10	IN+, INP1, 2, 3	Non-inverting inputs
2	1	$\overline{EN}$	$\overline{ENABLE}$
3	3, 7, 11	IN-, INN1, 2, 3	Inverting inputs, note that on EL5173, this pin is also the REF pin
4	4, 8, 12	REF1, 2, 3	Reference inputs, sets common-mode output voltage
5	14, 17, 23	OUT-, OUT1B, 2B, 3B	Inverting outputs
6	21	VS+, VSP	Positive supply
7	20	VS-, VSN	Negative supply
8	15, 18, 24	OUT+, OUT1, 2, 3	Non-inverting outputs
	5, 9, 13, 16, 19, 22	NC	No connect; grounded for best crosstalk performance

Connection Diagrams

EL5173



EL5373



Typical Performance Curves

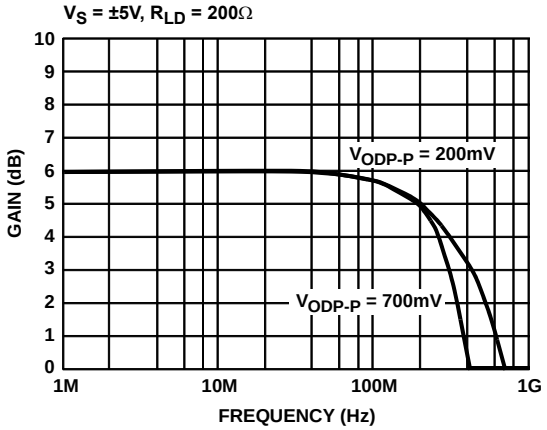


FIGURE 1. FREQUENCY RESPONSE

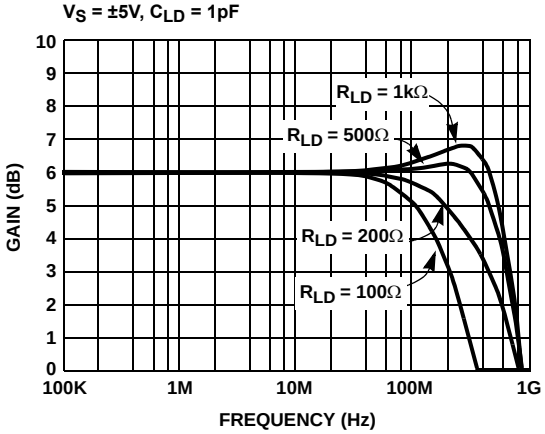


FIGURE 2. FREQUENCY RESPONSE vs R_{LD}

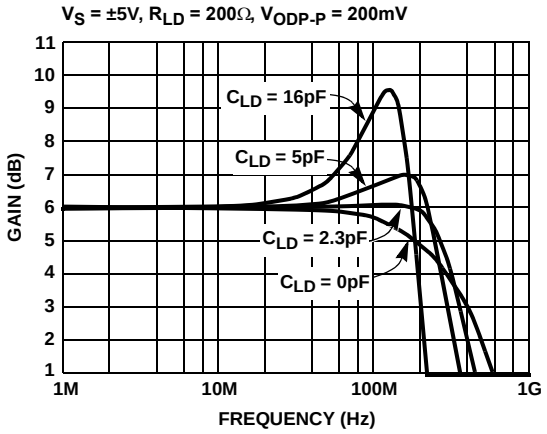


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LD}

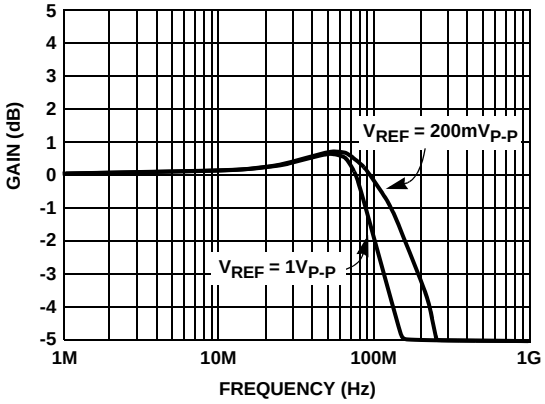


FIGURE 4. FREQUENCY RESPONSE vs V_{REF}

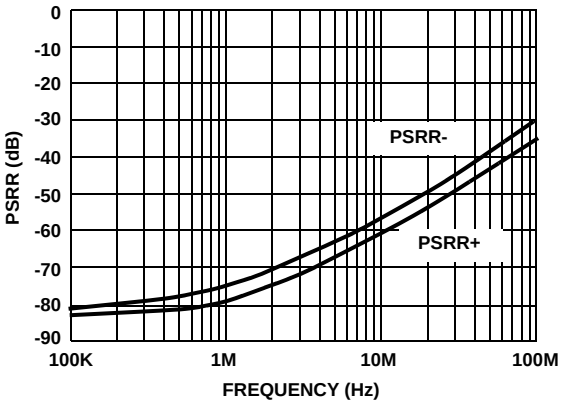


FIGURE 5. PSRR vs FREQUENCY

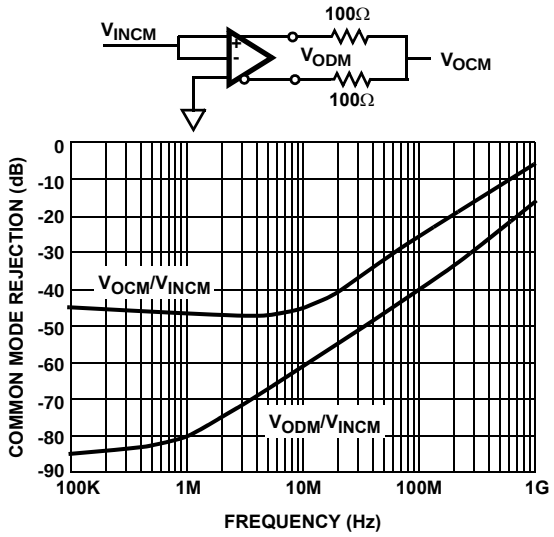


FIGURE 6. COMMON MODE REJECTION vs FREQUENCY

Typical Performance Curves (Continued)

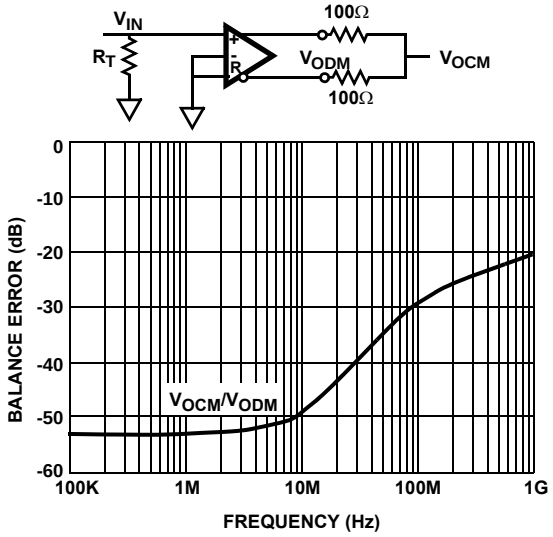


FIGURE 7. DIFFERENTIAL MODE OUTPUT BALANCE ERROR vs FREQUENCY

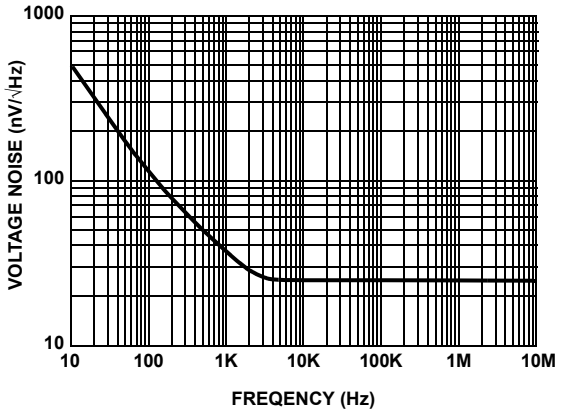


FIGURE 8. INPUT VOLTAGE NOISE vs FREQUENCY

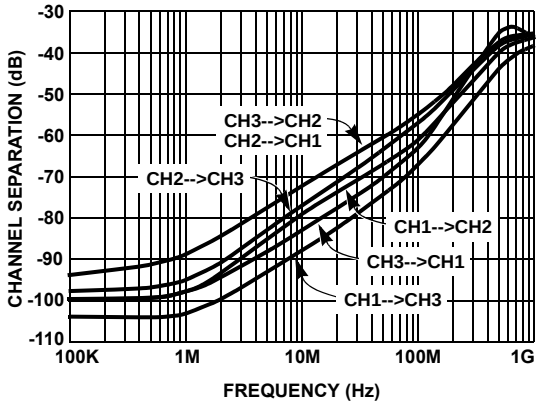


FIGURE 9. CHANNEL SEPARATION vs FREQUENCY

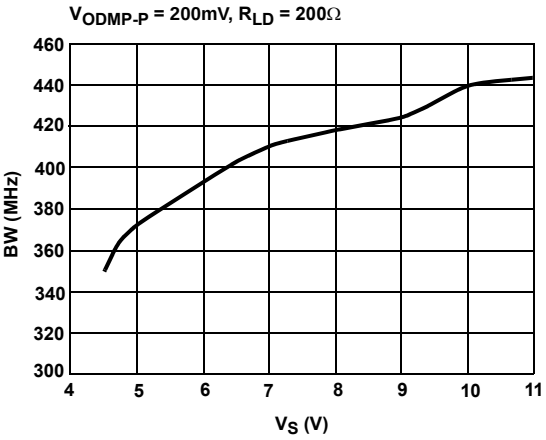


FIGURE 10. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE

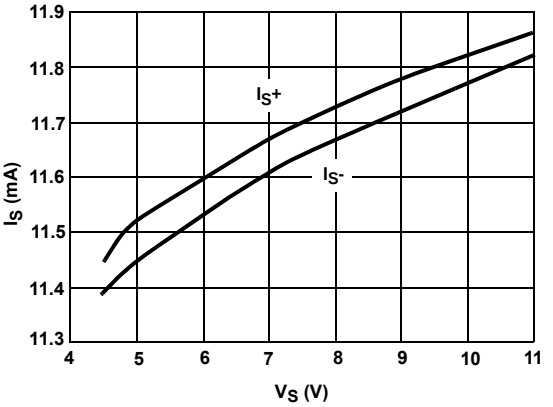


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

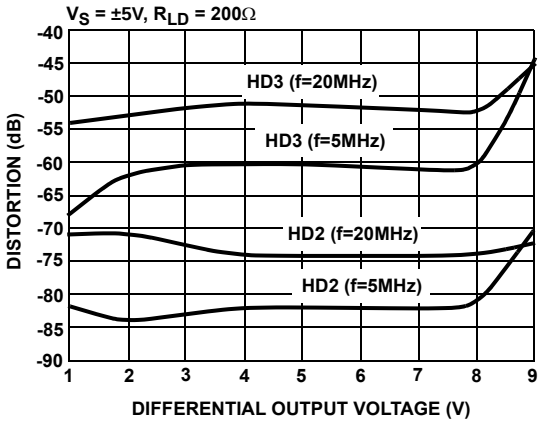


FIGURE 12. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

Typical Performance Curves (Continued)

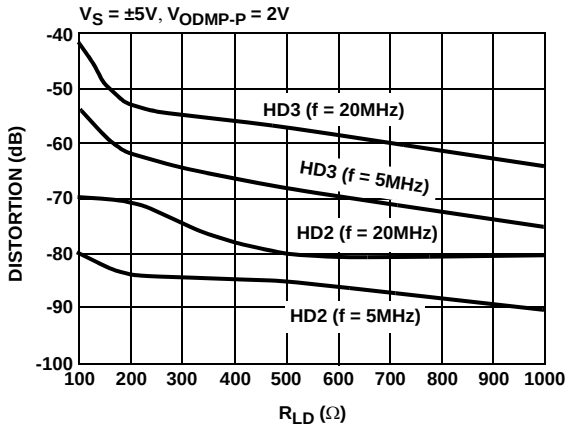


FIGURE 13. HARMONIC DISTORTION vs R_{LD}

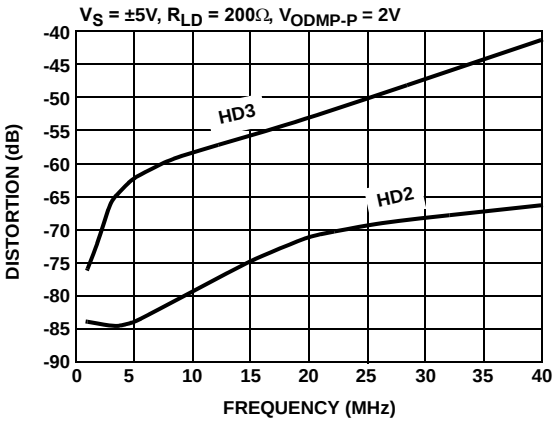


FIGURE 14. HARMONIC DISTORTION vs FREQUENCY

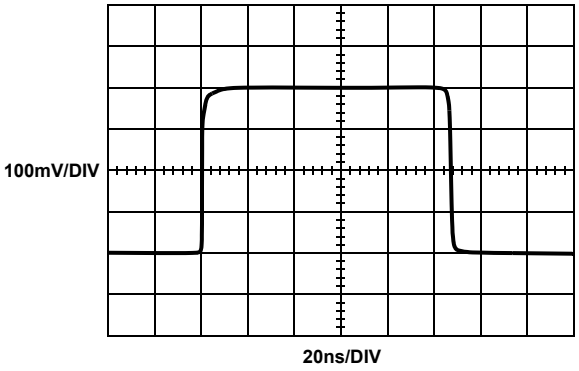


FIGURE 15. SMALL SIGNAL TRANSIENT RESPONSE

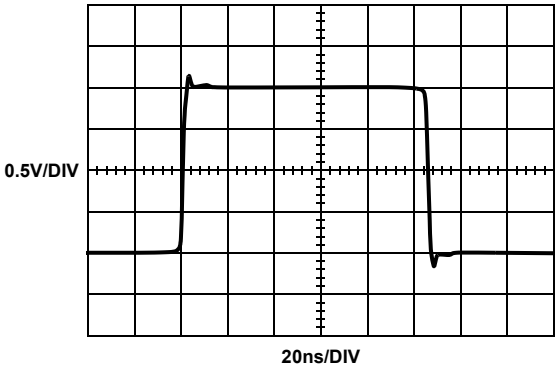


FIGURE 16. LARGE SIGNAL TRANSIENT RESPONSE

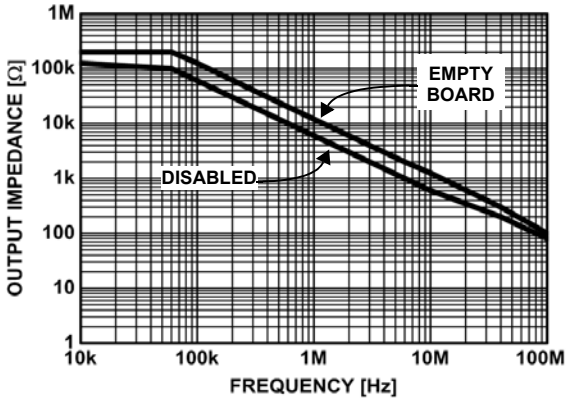


FIGURE 17. OUTPUT IMPEDANCE (DISABLED)

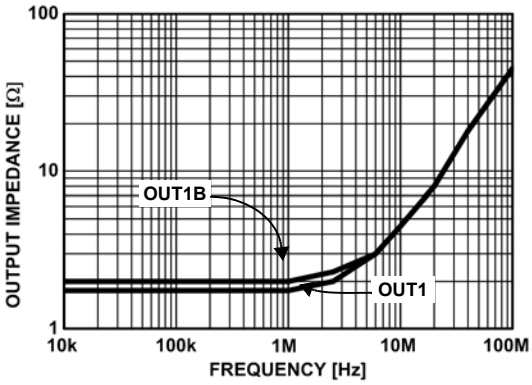


FIGURE 18. OUTPUT IMPEDANCE (ENABLED)

Typical Performance Curves (Continued)

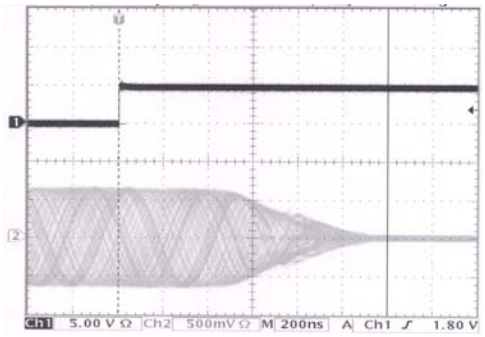


FIGURE 19. DISABLED RESPONSE

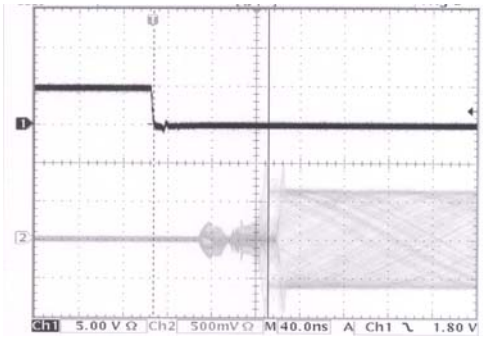


FIGURE 20. ENABLED RESPONSE

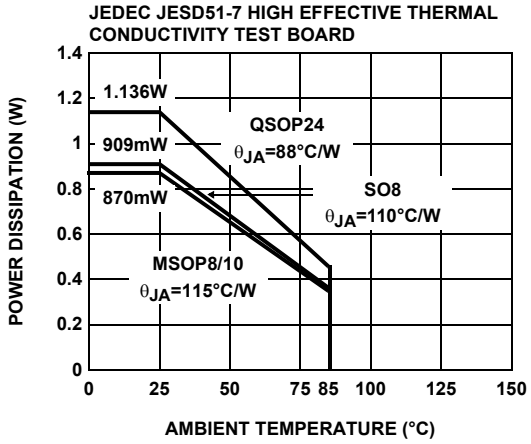


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

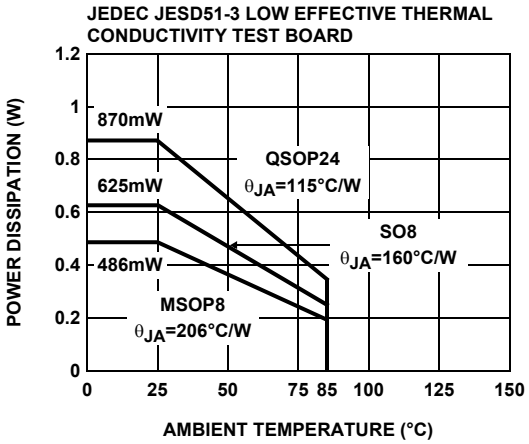
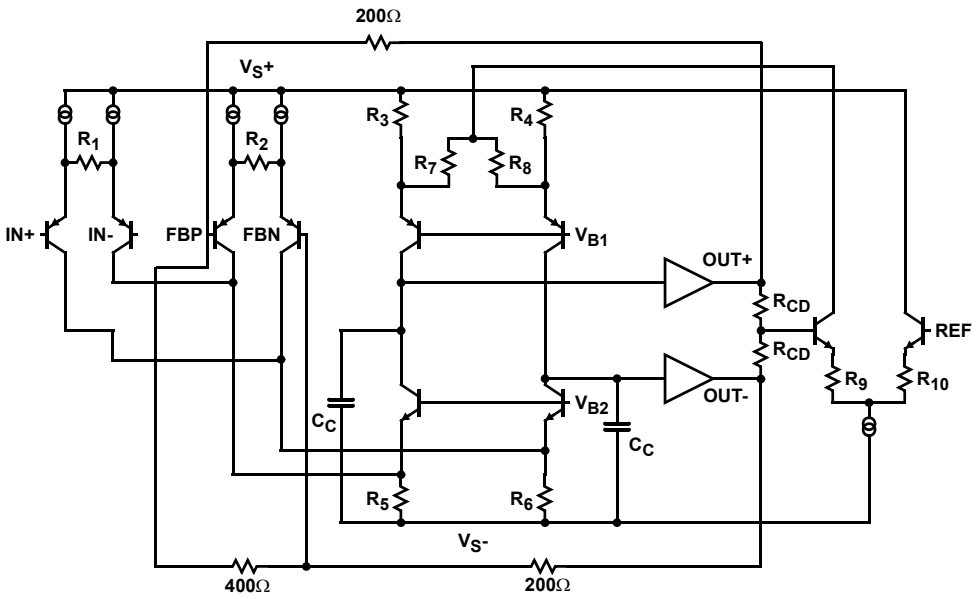


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5173 and EL5373 are wide bandwidth, low power and single/differential ended to differential output amplifiers. They have a fixed gain of 2. The EL5173 is a single channel differential amplifier. The EL5373 is a triple channel differential amplifier. The EL5173 and EL5373 have a –3dB bandwidth of 450MHz while driving a 200Ω differential load. The EL5173 and EL5373 are available with a power down feature to reduce the power while the amplifiers are disabled.

Input, Output and Supply Voltage Range

The EL5173 and EL5373 have been designed to operate with a single supply voltage of 5V to 10V or a split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.5V to 3.4V for ±5V supply. The differential mode input range (DMIR) between the two inputs is from –2.3V to +2.3V. The input voltage range at the REF pin is from –3.3V to 3.7V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal distorted.

The output of the EL5173 and EL5373 can swing from –3.3V to 3.6V at 200Ω differential load at ±5V supply. As the load resistance becomes lower, the output swing is reduced.

Differential and Common Mode Gain Settings

As shown at the simplified schematic, since the feedback resistors RF and the gain resistor are integrated with 200Ω and 400Ω, the EL5173 and EL5373 have a fixed gain of 2. The common mode gain is always one.

Driving Capacitive Loads and Cables

The EL5173 and EL5373 can drive 16pF differential capacitor in parallel with 200Ω differential load with less than 3.5dB of peaking. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL5173 and EL5373 can be disabled and placed their outputs in a high impedance state. The turn off time is about 1.2µs and the turn on time is about 100ns. When disabled, the amplifier's supply current is reduced to 40µA for I_S+ and 2.5µA for I_S- typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied logic signal is relative to V_S+ pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 1.5V below V_S+ will enable the amplifier. The amplifier will be disabled when the signal at $\overline{EN}$ pin is above V_S+ -0.5V.

Output Drive Capability

The EL5173 and EL5373 have internal short circuit protection. Its typical short circuit current is ±55mA. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed.

Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnect.

Power Dissipation

With the high output drive capability of the EL5173 and EL5373 it is possible to exceed the 125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = i \times \left(V_S \times I_{SMAX} + V_S \times \frac{\Delta V_O}{R_{LD}} \right)$$

Where:

- V_S = Total supply voltage
- I_{SMAX} = Maximum quiescent supply current per channel
- ΔV_O = Maximum differential output voltage of the application
- R_{LD} = Differential load resistance
- I_{LOAD} = Load current
- i = Number of channels

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as sort as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

Twisted pair cable driver

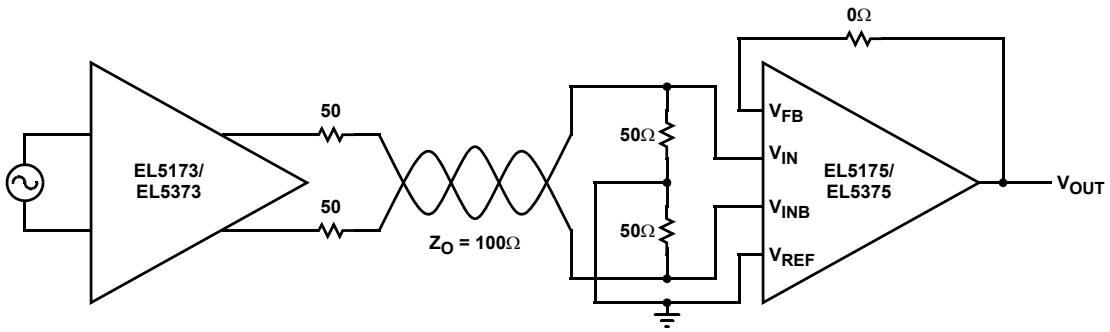
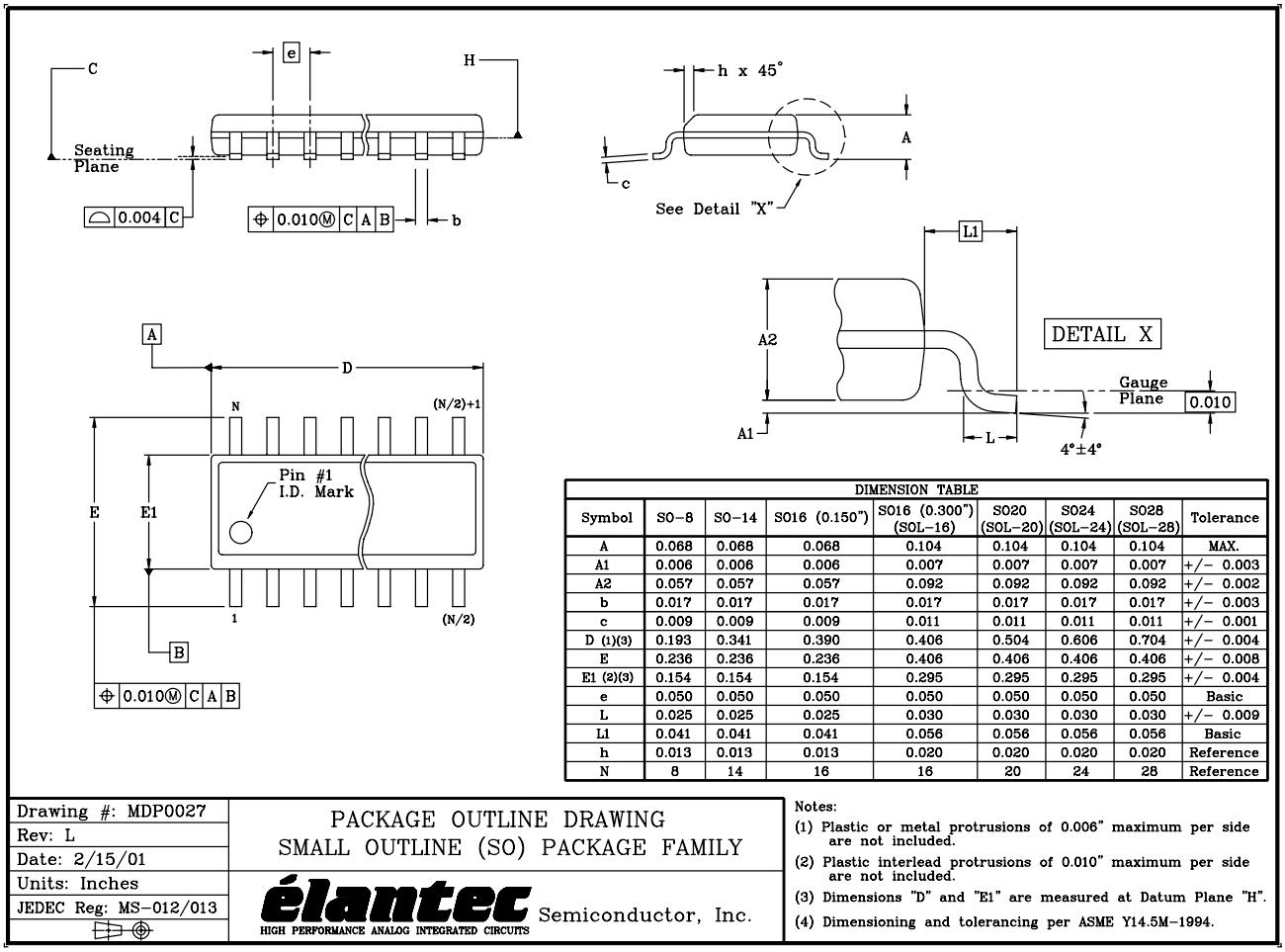


FIGURE 23. TWISTED PAIR CABLE DRIVER

SO Package Outline Drawing

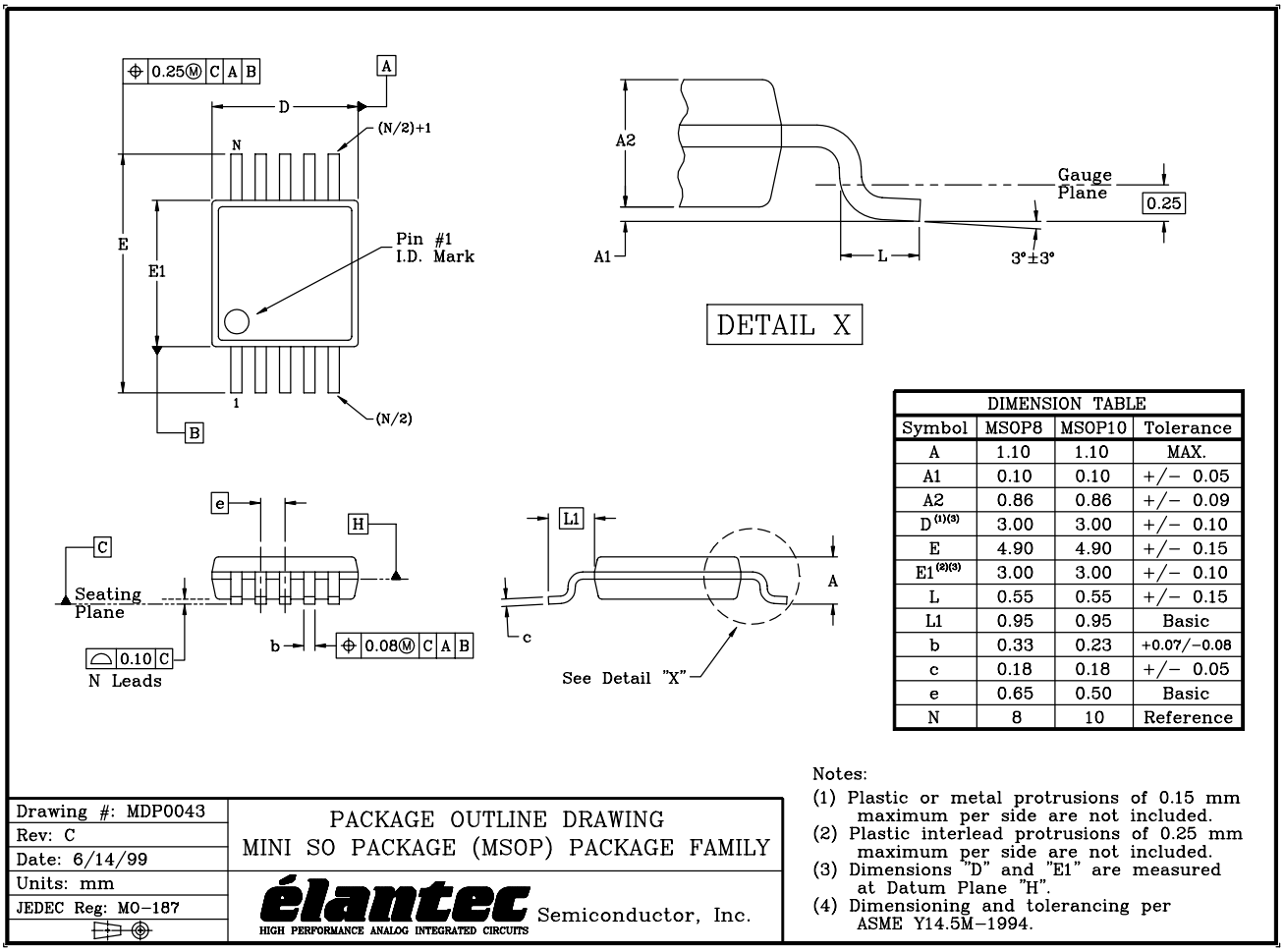


DIMENSION TABLE								
Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Units: Inches	
JEDEC Reg: MS-012/013	

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

MSOP Package Outline Drawing

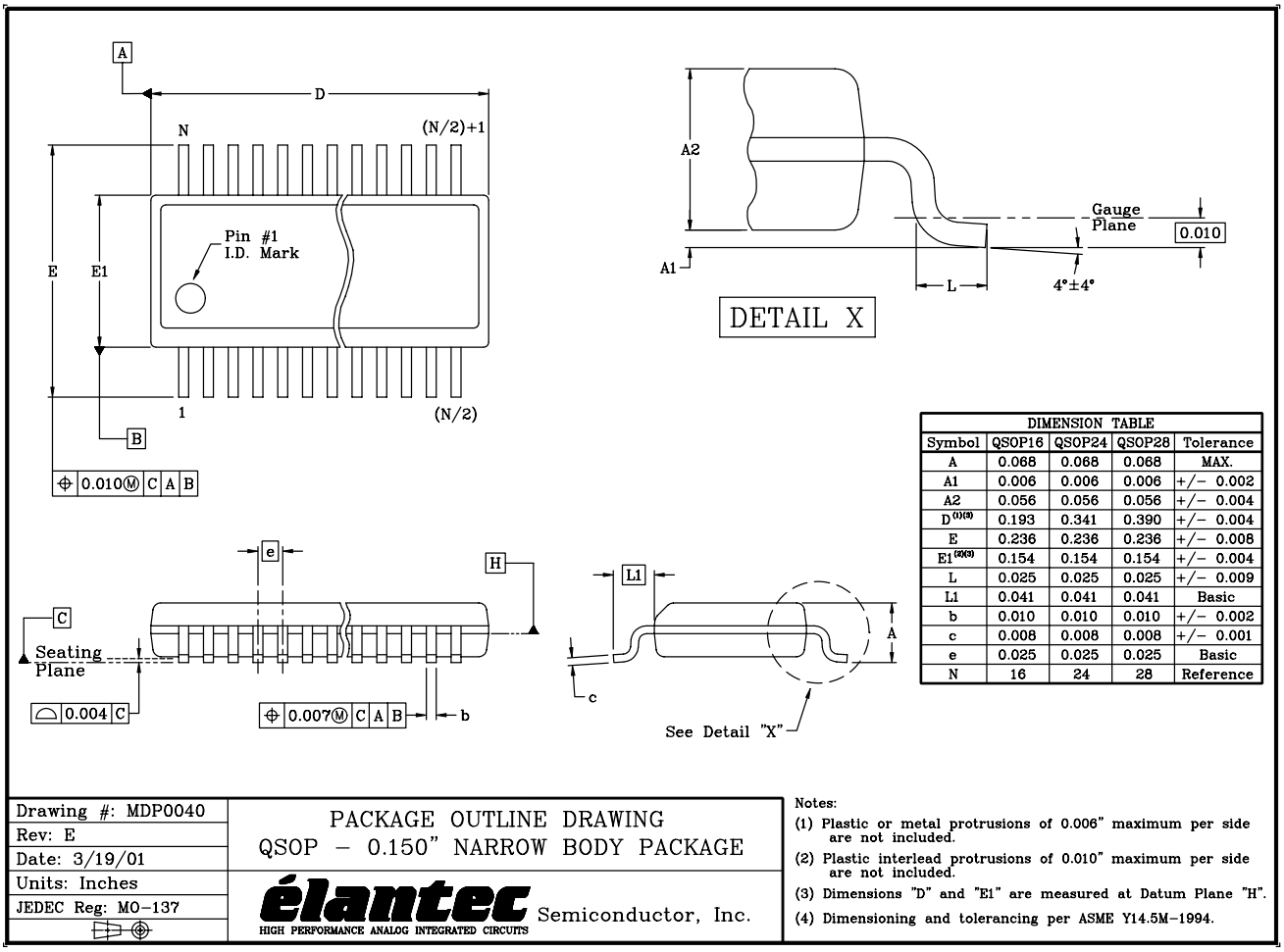


DIMENSION TABLE			
Symbol	MSOP8	MSOP10	Tolerance
A	1.10	1.10	MAX.
A1	0.10	0.10	+/− 0.05
A2	0.86	0.86	+/− 0.09
D (1)(3)	3.00	3.00	+/− 0.10
E	4.90	4.90	+/− 0.15
E1 (2)(3)	3.00	3.00	+/− 0.10
L	0.55	0.55	+/− 0.15
L1	0.95	0.95	Basic
b	0.33	0.23	+0.07/−0.08
c	0.18	0.18	+/− 0.05
e	0.65	0.50	Basic
N	8	10	Reference

Drawing #: MDP0043	PACKAGE OUTLINE DRAWING MINI SO PACKAGE (MSOP) PACKAGE FAMILY
Rev: C	
Date: 6/14/99	
Units: mm	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO-187	

Notes:
(1) Plastic or metal protrusions of 0.15 mm maximum per side are not included.
(2) Plastic interlead protrusions of 0.25 mm maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

QSOP Package Outline Drawing



DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/− 0.002
A2	0.056	0.056	0.056	+/− 0.004
D (1)(3)	0.193	0.341	0.390	+/− 0.004
E	0.236	0.236	0.236	+/− 0.008
E1 (2)(3)	0.154	0.154	0.154	+/− 0.004
L	0.025	0.025	0.025	+/− 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/− 0.002
c	0.008	0.008	0.008	+/− 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040	PACKAGE OUTLINE DRAWING
Rev: E	QSOP – 0.150" NARROW BODY PACKAGE
Date: 3/19/01	élantec Semiconductor, Inc.
Units: Inches	HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO-137	

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M–1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp