élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4083C

Current Mode Four Quadrant Multiplier

Features

- Novel current mode design
  Virtual ground current summing inputs
  Differential ground referenced current outputs
- High speed (both inputs)
  200 MHz bandwidth
  12 ns 1% settling time
- Low distortion
  THD < 0.03% @ 1 MHz
  THD < 0.1% @ 10 MHz
- Low noise (R_L = 50Ω)
  100 dB dynamic range
  10 Hz to 20 kHz
  73 dB dynamic range
  10 Hz to 10 MHz
- Wide supply conditions
  ±5 to ±15V operation
  Programmable bias current
- 0.2 dB gain tolerance to 25 MHz

Applications

- Four quadrant multiplication
- Gain control
- Controlled signal summing and multiplexing
- HDTV video fading and switching
- Mixing/modulating/demodulating (phase detection)
- Frequency doubling
- Division
- Squaring
- Square rooting
- RMS and power measurement
- Vector addition-RMS summing
- CRT focus and geometry correction
- Polynomial function generation
- AGC circuits

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4083CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL4083CS	−40°C to +85°C	8-Pin SO	MDP0027

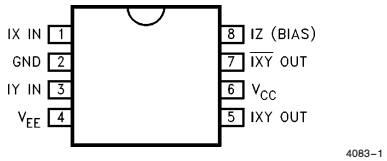
General Description

The 4083C makes use of an Elantec fully complimentary oxide isolated bipolar process to produce a patent pending current in, current out four quadrant multiplier. Input and output signal summing and direct interface to other current mode devices can be accomplished by simple connection to reduce component count and preserve bandwidth. The selection of an appropriate series resistor value allows an input to accept a voltage signal of any size and optimize dynamic range. The differential outputs offer significant performance improvements which greatly extend the usable gain control range at high frequencies. The bias current is programmable to accommodate the voltage and power dissipation constraints of the package and available systems supplies.

The devices can implement all the classic four quadrant multiplier applications and are uniquely well suited to gain control and signal summing of broadband signals.

Connection Diagram

EL4083
8-Pin SO/P DIP



Top View

Manufactured under U.S. Patent No. 5,389,840

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V_S+ and V_S-	+33V
$I_{Z(BIAS)}$	Z, Bias Current	+2.4 mA
I_X	X Input Current	±2.4 mA
I_Y	Y Input Current	±2.4 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	
	EL4083	−40°C to +85°C
T_J	Operating Junction Temperature	
	EL4083	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Power Supplies						
Operating Supply Voltage Range		±4.5		±16.5	I	V
I_{CC}	V_S = ±15V, I_Z = 0.2 mA	7.2	8.5	9.5	I	mA
I_{CC}	V_S = ±5V, I_Z = 1.6 mA	42.0	44.0	45	I	mA
I_{EE}	V_S = ±15V, I_Z = 0.2 mA	9.5	10.0	12	I	mA
I_{EE}	V_S = ±5V, I_Z = 1.6 mA	45	47	48	I	mA
Multiplier Performance						
Transfer Function (Note 5)	$(I_{XY}-I_{\overline{XY}}) = K(I_X \times I_Y)/I_Z$					
K Value		0.92	0.965	1.01	I	
Total Error (Note 1)	−2 mA < I_X, I_Y <2 mA		±0.5	±2	I	%FS
vs. Temp	T_{MIN} to T_{MAX}		±1.5	±3	IV	%FS
Linearity (Note 2)			0.25	0.5	I	%FS
Bandwidth (Note 3)	−3 dB (See Figure 2)	200	225		III	MHz
X Feedthrough DC to I_{XY} or $I_{\overline{XY}}$ (Note 5)	I_X = ±2 mA, I_Y = 0 (unnulled)		0.15	1.6	I	%FS
Y Feedthrough DC to I_{XY} or $I_{\overline{XY}}$ (Note 5)	I_Y = ±2 mA, I_X = 0 (unnulled)		0.15	1.6	I	%FS
AC Feedthrough, X to I_{XY} or $I_{\overline{XY}}$ (Note 4)	I_X = 4 mApp, I_Y = nulled					
	f = 3.58 MHz		−80		V	dB
	f = 100 MHz		−28		V	dB
AC Feedthrough, X to $(I_{XY}-I_{\overline{XY}})$ (Note 4)	I_X = 4 mApp, I_Y = nulled DC < f < 1 GHz		−50		V	dB
AC Feedthrough, Y to I_{XY} or $I_{\overline{XY}}$ (Note 4)	I_Y = 4 mApp, I_X = nulled					
	f = 3.58 MHz		−64		V	dB
	f = 100 MHz		−26		V	dB
AC Feedthrough, Y to $(I_{XY}-I_{\overline{XY}})$ (Note 4)	I_Y = 4 mApp, I_X = nulled DC < f < 1 GHz		−50		V	dB

TD is 3.7in

Electrical Characteristics — Contd. (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Inputs (I_X, I_Y)						
Full Scale Range	FRS = 1.25 × I_Z (Nominal)		±2		I	mA
Clipping Level	C_L = 2 × I_Z	2.85	3.2		I	mA
Z_{IN} (I_X)		30	40	48	I	Ω
Z_{IN} (I_Y)		30	36	48	I	Ω
Input Offset Voltages	at Input Pins, I_Z = 1.6 mA	−4		+4		mV
(V_{OSX},V_{OSY})	I_Z = 0.2 mA	−12		+12		mV
Input Offset Currents (Note 5)	R_{SX} = R_{SY} = 1K, V_X = V_Y = 0,		±10	±40	I	µA
I_{XOS}, I_{YOS}	T_{MIN} to T_{MAX}		±20		V	nA/°C
Nonlinearity						
I_X	I_Y = 2 mA, − 2 mA < I_X < 2 mA		0.1	0.6	I	%FS
I_Y	I_X = 2 mA, − 2 mA < I_Y < 2 mA		0.1	0.4	I	%FS
Distortion, I_X (to I_{XY} or $I_{\overline{XY}}$)	I_Y = 2 mA, − 2 mA < I_X < 2 mA					
	f = 3.58 MHz		−55		V	dB
	f = 100 MHz		−25		V	dB
Distortion, I_Y (to I_{XY} or $I_{\overline{XY}}$)	I_X = 2 mA, − 2 mA < Iy < 2 mA					
	f = 3.58 MHz		−56		V	dB
	f = 100 MHz		−26		V	dB
Distortion, I_X (to (I_{XY} − $I_{\overline{XY}}$)	I_Y = 2 mA, −2 mA < I_X < 2 mA					
	f = 3.58 MHz		−66		V	dB
	f = 100 MHz		−35		V	dB
Distortion, I_Y (to (I_{XY} − $I_{\overline{XY}}$)	I_X = 2 mA, −2 mA < I_Y < 2 mA					
	f = 3.58 MHz		−66		V	dB
	f = 100 MHz		−34		V	dB
Diff Gain	@3.58 MHz					
I_X	I_Z = 0.2 mA, I_Y = 0.25 mA		0.2		V	%
I_Y	I_Z = 0.2 mA, I_X = 0.25 mA		0.17		V	%
I_X	I_Z = 1.6 mA, I_Y = 2 mA		0.1		V	%
I_Y	I_Z = 1.6 mA, I_X = 2 mA		0.05		V	%
Diff Phase	@3.58 MHz					
I_X	I_Z = 0.2 mA, I_Y = 0.25 mA		0.5		V	deg °
I_Y	I_Z = 0.2 mA, I_X = 0.25 mA		0.5		V	deg °
I_X	I_Z = 1.6 mA, I_Y = 2 mA		0.05		V	deg °
I_Y	I_Z = 1.6 mA, I_X = 2 mA		0.05		V	deg °
Outputs (I_{XY}, I_{YX})						
Output I_{OS} (Note 5)	I_X = I_Y = 0		−15	±120	I	µA
Diff Output I_{OS} (Note 5)	I_X = I_Y = 0, (I_{XY}–$I_{\overline{XY}}$)		±0.1	±80	I	µA
Voltage Compliance		±1.5	±2.0		V	V
Max Output Current Swing		±2.85	±3.2		I	mA
Noise Spectral Density						
10 Hz < f < 10 MHz	R_L = 50Ω		125		V	pA/rootHz
I_Z (Bias)						
Current Range	Tested	0.2		1.6	I	mA
Input Voltage	I_Z = 0.2 mA			±25	I	mV
Input Voltage	I_Z = 1.6 mA			±25	I	mV

Note 1: Error is defined as the maximum deviation from the ideal transfer function expressed as a percentage of the full scale output.

Note 2: Linearity is defined as the error remaining after compensating for scale factor (gain) variation and input and output referred offset errors.

Note 3: Bandwidth is guaranteed using the squaring mode test circuit of Figure 4.

Note 4: Relative to full scale output with full scale sinewave on signal input and zero port input nulled. Specification represents feedthrough of the fundamental.

Note 5: Specifications are provisional for the EL4083.

TD is 5.8in

EL4083 Block Diagram

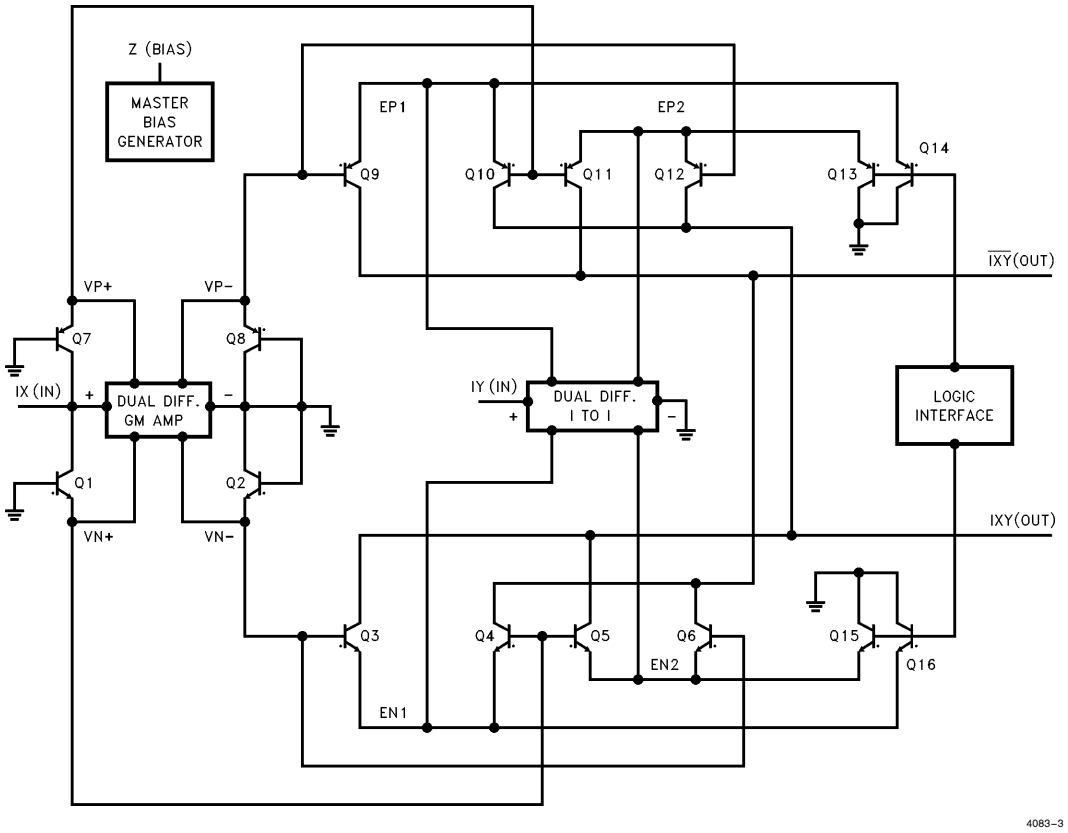


Figure 1

AC Test Fixture

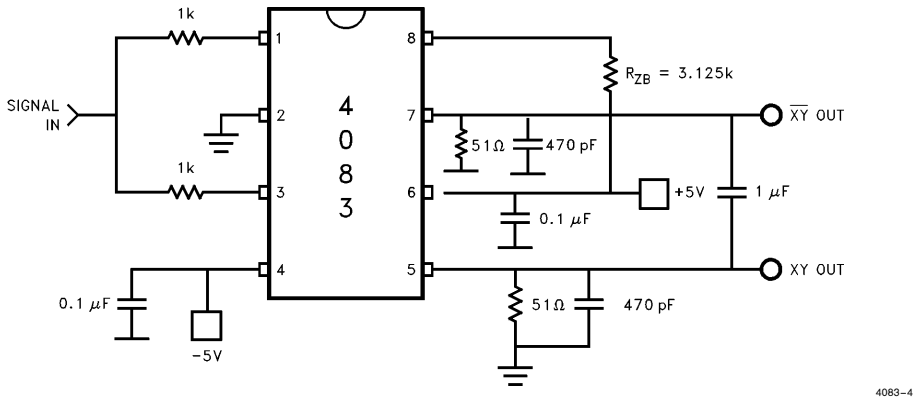


Figure 2. AC Bandwidth Test Fixture

Burn-In Circuit

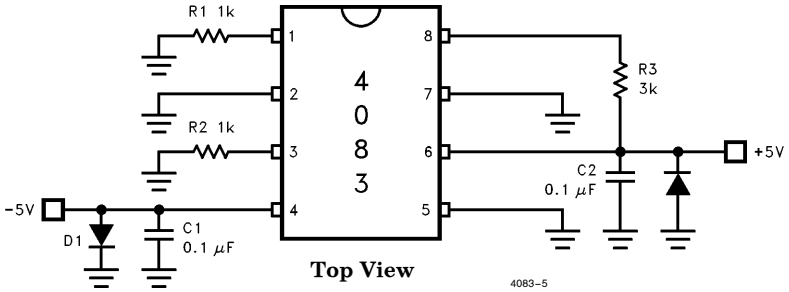


Figure 3. Burn-In Circuit P-DIP

8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

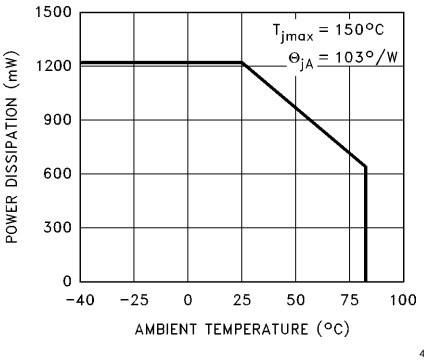


Figure 4

8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

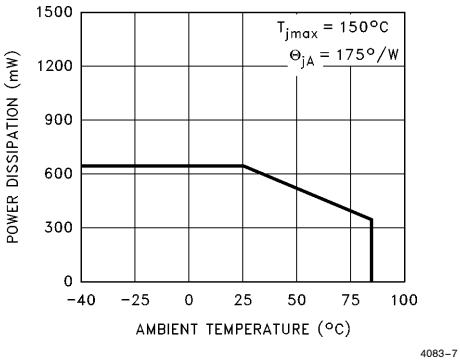


Figure 5

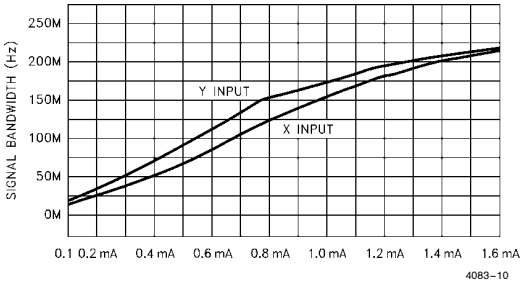


Figure 6. (I_X, I_Y Bandwidth vs I_Z)

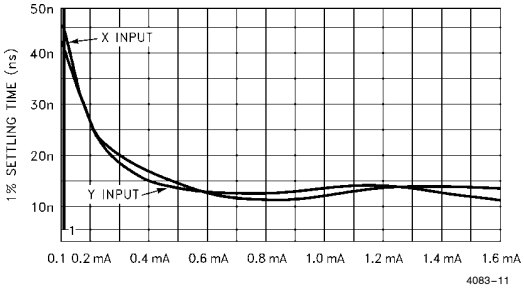


Figure 7. (I_X, I_Y 1% Settling Time vs I_Z)

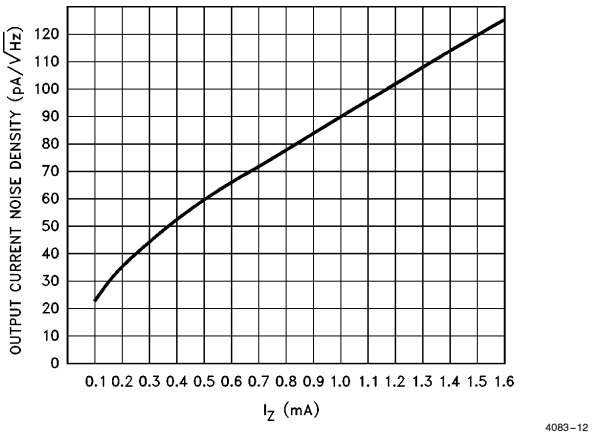
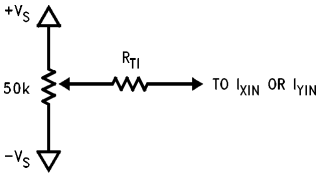


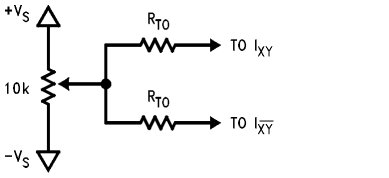
Figure 8. Output Noise Density vs I_Z Bias

Input Offset Trim(s)



$R_{TI} = (V_S \times 1.6\ mA)/(16\ \mu A \times I_Z)$

Output Offset Trim



$R_{TO} = (V_S \times 1.6\ mA)/(30\ \mu A \times I_Z)$

Figure 9. Optional External Trim Networks

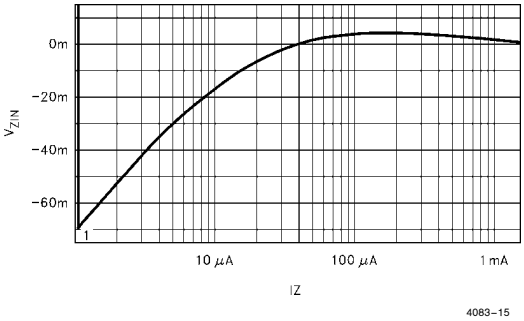


Figure 10. V_{ZIN} vs I_Z (Typical)

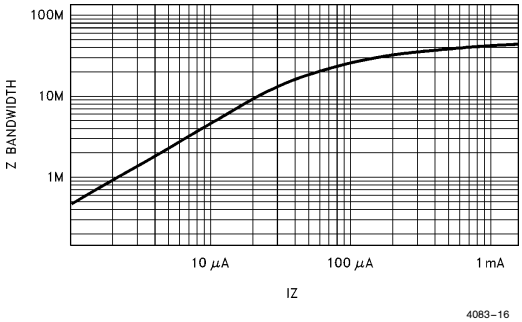


Figure 11. I_{ZIN} Bandwidth vs I_Z

General Operating Information

I_Z Input (Bias, Divisor) and Power Supplies

The I_Z pin is a low impedance ($<20\Omega$) virtual ground current input. It can accept positive current from a resistor connected to a positive voltage source or the positive supply. The instantaneous bias for the multiplier gain core is proportional to this current value. Negative applied current will put the multiplier portion of the circuit in a zero bias state and the voltage at the pin will be clamped at a diode drop below ground. The part will respond in a similar manner to currents from a current source such as the output of a transconductance amplifier or one of its own outputs. The overall transfer equation for the EL4083 is:

$$K(I_X \times I_Y)/I_Z = (I_{XY} - I_{\overline{XY}}),\ K \sim 1$$

As can be seen from the equation, the Z input can serve as a divisor input. However, it is different from the other two inputs in that the value of its current determines the supply current of the part and the bandwidth and compliance range of the outputs and other two inputs. Table 1 gives the equations describing these and other important relationships. These dependencies can complicate and/or limit the usefulness of this pin as a computational input. The I_Z dependence of the impedance of the multiplying inputs can be particularly troublesome. See the I_Z divider and the RMS#2 circuit sections of the application note for some ways of dealing with this.

The primary intended use for the Z input is as a programming pin similar in function to those on programmable op amps. This enables one to trade off power consumption against bandwidth and settling time and allow the part to function within its power dissipation rating over its full operational supply range ($\pm4.5V$ – $\pm16.5V$). The E4083 has been designed to function well for I_Z values in the range of 200 $\mu A < I_Z < 1.6$ mA which corresponds to I_X and I_Y signal bandwidths of about 50 MHz to over 200 MHz. Higher values of I_Z may cause problems at temperature extremes while lower values down to zero will progressively degrade the input referred D.C. offsets and reduce speed. Below about 50 μA of bias current the internal servo amplifier loop which maintains the I_Z pin at ground will lose regulation and the voltage at the pin will start to move negative (see Figure 10). This is accompanied by a significant increase in input impedance of the pin. Figure 11 shows the A.C. bandwidth of the I_Z input as a function of the D.C. value of I_Z. Figures 6 and 7 show the bandwidth and 1% settling time of the multiplying inputs, I_X and I_Y, as functions of I_Z.

I_X and I_Y (Multiplier) Inputs and Offset Trimming

The I_X and I_Y pins are low impedance (I_Z dependent) virtual ground current inputs that accept bipolar signals. The input referred clip value is equal to $I_Z \times 2$ while the full scale value has been chosen to be $1.25 \times I_Z$ to maintain excellent distortion and linearity performance. Operating at higher full scale values will degrade these two pa-

Table 1. Basic Design Equations and Relationships

Positive Supply Current	$I_S+ = 3.4\text{ mA} + I_Z \times 26$
Negative Supply Current	$I_S- = 4.5\text{ mA} + I_Z \times 27$
Power Dissipation (See Figures 4 and 5)	$PWR = (+V_S - (-V_S)) \times (4\text{ mA} + I_Z \times 26.5)$
Multipling Input(s) Impedance	$R_{ZX} = R_{ZY} = (32\Omega) \times 1.6\text{ mA}/I_Z$
Multiplying Input(s) Clip Point	$I_X\text{ (clip)} = I_Y\text{ (clip)} = I_Z \times 2$
Multiplying Input(s) Full Scale Value	$I_X\text{ (fs)} = I_Y\text{ (fs)} = I_Z \times 1.25\text{ (nominal)}$
Multiplying Input Resistor Values	$R_X = V_X\text{ (peak)}/I_X\text{ (fs)}$
(In Terms of Peak Input Signal)	$R_Y = V_Y\text{ (peak)}/I_Y\text{ (fs)}$
Full Scale Output (Single Ended)	$I_{XY} = I_{\overline{XY}} = I_X\text{ (fs)} \times I_Y\text{ (fs)}/(I_Z \times 2)$
Full Scale Output (Differential)	$(I_{XY} - I_{\overline{XY}}) = I_X\text{ (fs)} \times I_Y\text{ (fs)}/I_Z$
I_Z (Bias) Input Voltage vs I_Z	(See Figure 10)
I_Z Signal Bandwidth vs I_Z	(See Figure 11)
I_X, I_Y Signal Bandwidth vs I_Z	(See Figure 6)
I_X, I_Y 1% Settling Time vs I_Z	(See Figure 7)

General Operating Information

— Contd.

rameters and, to some extent, bandwidth while improving the signal to noise performance, feedthrough and control range.

The EL4083 is fundamentally different from conventional voltage mode multipliers in that the available input range can be tailored to accommodate voltage sources of almost any size by selecting appropriate input series resistor values. If desired, one can interface with voltages that are much greater than the supplies from which the part is powered. Current source signals can be connected directly to the multiplier inputs. The parts' dynamic range can also be tailored to a large extent for a current signal by the appropriate selection of I_Z. These inputs act in the same manner as a virtual ground input of an operational amplifier and thus can serve as a summing node for any number of voltage and/or current signals. Outputs of components such as current output DACs, transconductance amplifiers and current conveyors can be directly connected to the inputs.

Ideally, a multiplier should give zero output if either one of its multiplying inputs is zero. A nonzero output under these conditions is caused by a combination of input and output referred offsets. An output referred offset can be thought of as a fixed value added to the output and thus only affects D.C. accuracy. An input referred offset at a multiplying input allows signal to feedthrough from the other multiplying input to the output(s). The EL4083 is trimmed during testing at Elantec for X and Y input referred offset for I_Z = 1.6 mA. The internal trim networks provide a current to each input which nulls the feedthrough caused by internal device mismatches. These current values are ratioed to the value of I_Z so that the input referred nulls are largely maintained at different values of I_Z. However, there will be some mistracking in the trim networks so that the input referred null point will deviate away from zero at values of I_Z lower than 1.6 mA. Figure 9 shows optional external input and output referred offset trim networks which can be used as needed to improve performance. As mentioned, the output referred offset only affects D.C. accuracy which may not be an issue in A.C. applications. In gain control applications one may only need to null feedthrough with respect to the gain control input.

In gain control (VCA) applications the X input should be used as the control input and the signal applied to the Y input since it has slightly higher bandwidth and better linearity and distortion performance.

Current Outputs (I_{XY}, $I_{\overline{XY}}$), Feedthrough and Distortion

Another unique feature of the EL4083 is the differential ground referenced current output structure. These outputs can drive 50Ω terminated lines and reactive loads such as transformers, baluns, and LC tank and filter circuits directly.* Unlike low impedance follower buffers, these outputs do not interact with the load to produce ringing or instability. If a high level low impedance output is required, the outputs can be recovered differentially and converted to a single ended output with a fast op amp such as the EL2075 (see Figure 19). The outputs can also drive current input devices such as CMF amps, current conveyors and its own inputs directly by simple connection.

Figures 12 and 14 show the nulled gain and feedthrough characteristics of the I_{XY} and $I_{\overline{XY}}$ outputs which are virtually identical and differ only in phase. Figure 12 is with the A.C. signal applied to the X input with Y used as the gain control and in Figure 14 these signals are reversed. Note that in both cases the signal feedthrough rolls up and peaks near the cutoff frequency. This is quite typical of the performance of all previous four quadrant multipliers. Figures 13 and 15 show the corresponding gain/feedthrough characteristics for the differentially recovered output signal I_{XY}-$I_{\overline{XY}}$. Note that in this case the peak feedthrough at high frequencies is lower by more than 40 dB.

* See EL2082 Data Sheet—Receiver IF Amplifier (Figure 19). The EL2082 also has a current output.

General Operating Information

— Contd.

Figures 16 and 17 show the total harmonic distortion for the single-ended and differential recovered outputs for a full scale A.C. input signal on one input and a full scale D.C. control signal on the other. Note that above about one megahertz to the cutoff frequency the THD of the differentially recovered signal is as much as 10 dB lower than the single-ended signals.

General Operating Information — Contd.

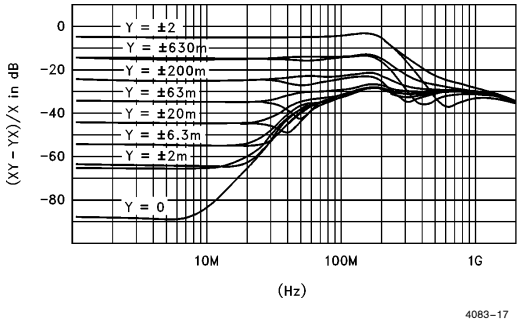


Figure 12. Nulled I_{XY} and $I_{\overline{XY}}$ Frequency Response (Signal on XIN, Gain Controlled by YIN)

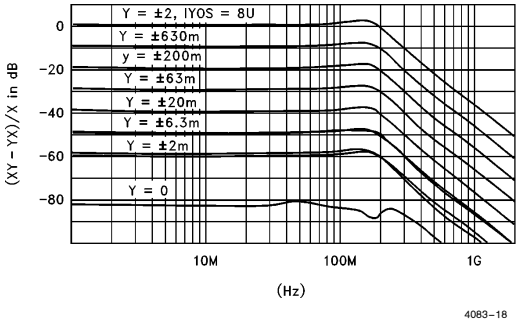


Figure 13. Nulled (I_{XY}-$I_{\overline{XY}}$) Frequency Response (Signal on XIN, Gain Controlled by YIN)

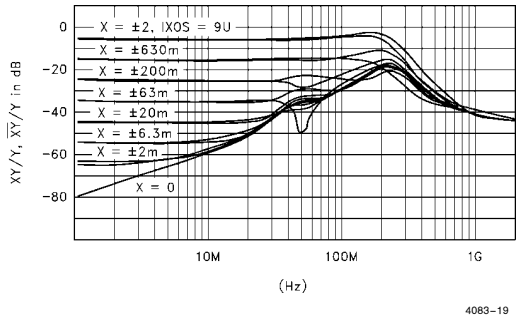


Figure 14. Nulled I_{XY} and $I_{\overline{XY}}$ Frequency Response (Signal on YIN, Gain Controlled by XIN)

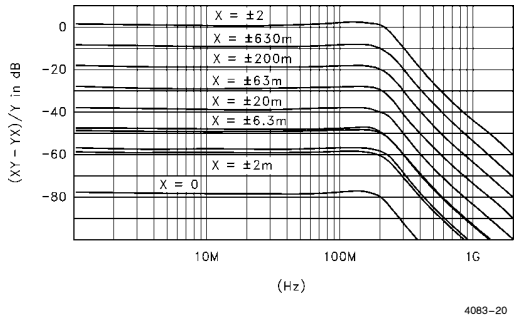


Figure 15. Nulled (I_{XY}–$I_{\overline{XY}}$) Frequency Response (Signal on YIN, Gain Controlled by XIN)

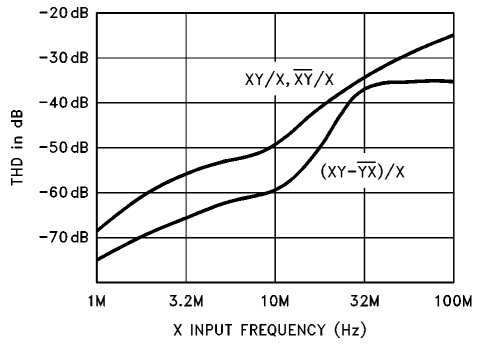


Figure 16. (Full Level XIN THD vs Frequency)

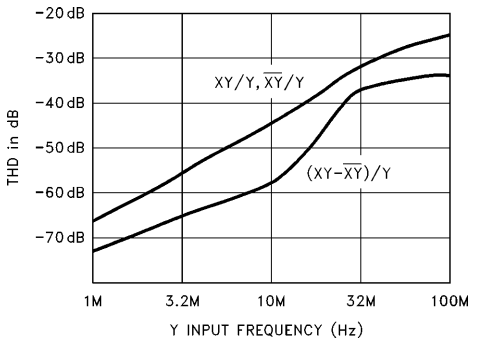


Figure 17. (Full Level YIN THD vs Frequency)

Applications

Basic Product Functions

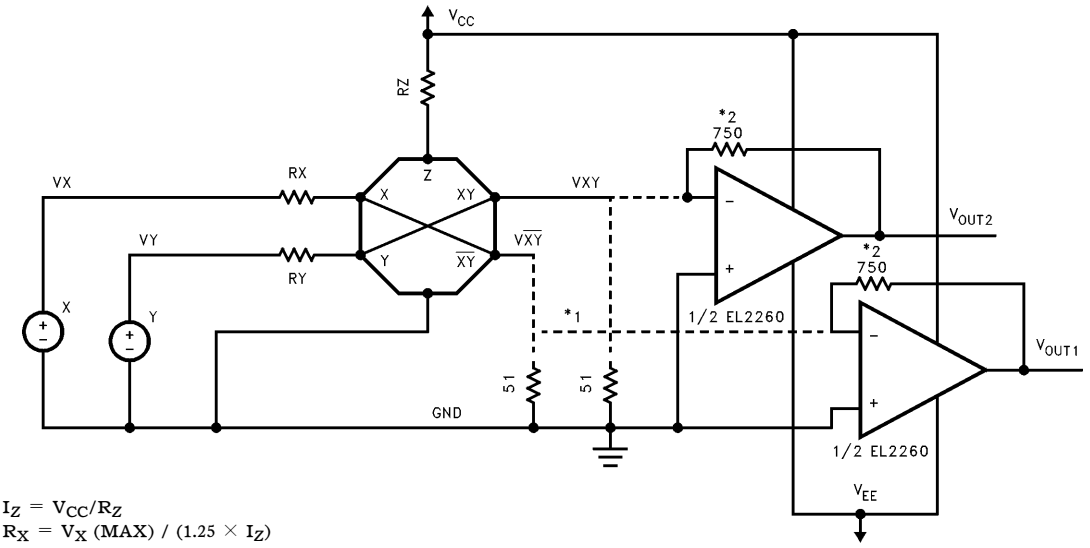
Figures 18 and 19 are the basic schematics for many of the applications of the EL4083. These can perform signal mixing, frequency doubling, modulation, demodulation, gain control/voltage-controlled amplification, multiplication and squaring. Figure 18 has resistively terminated differential outputs and has the widest bandwidth. The figure also shows the option of using the EL2260 dual CMF amplifier to recover the outputs differentially at very low impedance. This has a maximum 3 dB bandwidth of 130 MHz and settles to 1% in 25 ns. Figure 19 uses an EL2075 at the outputs as a differential to single ended converter with gain to take advantage of the performance enhancements of the differentially recovered output mentioned above and to provide a high level low impedance drive. The −3 dB bandwidth of this circuit is over 150 MHz using good layout techniques. However, to achieve this bandwidth one must restrict the output swing to little more than 1 Vpp to avoid running into the 500V/µs minimum slew rate of the EL2075. Table 2 shows the input signal assignments for the applications listed above.

Table 2. Input Signal Assignments for Figures 18 and 19 Circuits

Application	V_X	V_Y
Mixer	Signal 1	Signal 2
Frequency Doubler	Signal	Signal
Modulator	Modulating Signal	Carrier
Demodulator	Local Oscillator	Modulated Signal
Gain Control/VCA	Gain Control	Signal
Multiplier	Signal 1	Signal 2
Squarer	Signal	Signal

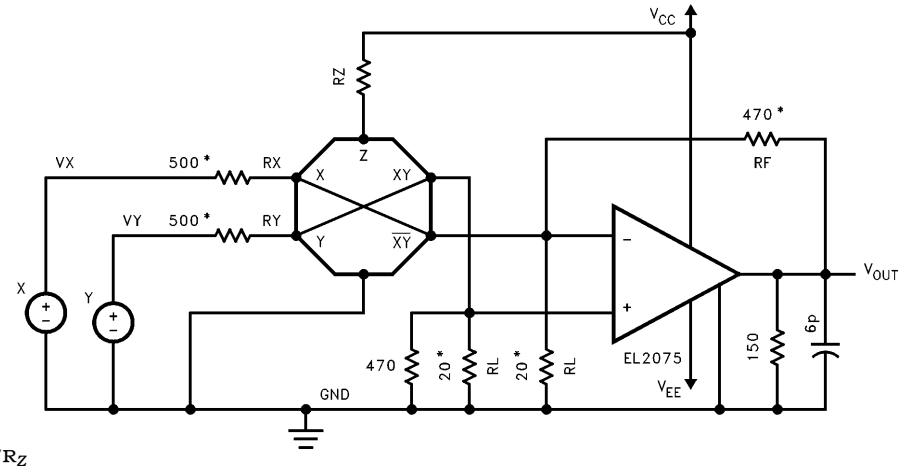
*X means not connected if function is not used.

Applications — Contd.



$I_Z = V_{CC}/R_Z$
$R_X = V_X$ (MAX) / (1.25 × I_Z)
$R_Y = V_Y$ (MAX) / (1.25 × I_Z)
*1. 51Ω Resistors omitted when using EL2260
*2. Optimum value of RF determined by supplies and amount or tolerable peaking
(−3 dB BW ~ 90 MHz @ V_S = ±5V, BW ~ 150 MHz @ ±15V)

Figure 18. Basic Schematic (Dual Diff Outs)



$I_Z = V_{CC}/R_Z$
$R_X = V_X$ (MAX) / (1.25 × I_Z)
$R_Y = V_Y$ (MAX) / (1.25 × I_Z)
*Optimized for Wide Bandwidth

Figure 19. Basic Schematic (Single Ended Converted)
(150 MHz VCA)

Other Applications

Elantec has also published an applications note covering other applications of the EL4083. These include dividers, squaring and square rooting circuits, several RMS and power measurement circuits, and a wideband AGC circuit. Also presented are two polynomial computation examples for video and some HDTV quality fader and summing circuits. The EL4083 has been found flexible enough to easily implement all of the classic four quadrant multiplier applications and also offer interesting new applications possibilities.

EL4083 Macromodel

This macromodel is compatible with PSPICE (copywritten by Microsim Corporation) . It has been designed to work accurately for fixed values of I_Z (bias) in the range of 200 μA to 1.6 mA. The additional simulation burden imposed by including provision for a time varying I_Z was thought not worthwhile. The value of I_Z is specified to the model by the parameter NS. The relation between I_Z and NS is; $I_Z = 200\ \mu A \times NS$. All other inputs can accept time varying signals.

The model will provide good transient and frequency response and settling time estimates as well as time domain switching results. Input and output impedance and overload responses are correctly modeled. The D.C. current drawn from supplies for a given value of I_Z is also correct.

Noise, PSRR and the temperature dependence of A.C. parameters such as frequency response and settling time are not modeled. Linearity and distortion results from the model will be worse than the real part by about a factor of three and do not show the correct frequency dependence.

The macromodel is constructed from simple controlled sources, passive components and stripped transistor and diode models. As such it should be usable, perhaps with slight modification, on all but student or demonstration simulators where the model's size may be a problem.

Macromodel

```
*EL4083 Macromodel
*Revision A, August 22, 1994
*
*Connection: IZ(BIAS)
*         |  IX(in)
*         |  |  IY(in)
*         |  |  |  VEE
*         |  |  |  |  VCC
*         |  |  |  |  |  IXY
*         |  |  |  |  |  |  /IXY
*         |  |  |  |  |  |  |
.subckt EL4083 ZIN XIN YIN VEE VCC IXY IYX
.MODEL M1MP5DIODE D TT=60p IS=1f CJO=300f
VJ=600m XTI=3 EG=1.11 RS=80m
.MODEL M2MDCAP D TT=100n IS=2e-17 CJO=1p
VJ=800m RS=300
.MODEL M3MNPN1 NPN CJC=1.3p TF=120p IS=1.04f
BF=120 CJS=480f
.MODEL M4MPNP1 PNP CJC=1.79p TF=50.166666666667p
IS=1f BF=90 CJS=480f
C1 N9 N7 9p
C2 N7 0 350f
C3 N19 N16 9p
C4 N16 0 350f
D1 0 N15 M2MDCAP 12
D10 0 N26 M1MP5DIODE 1
D11 N26 N27 M1MP5DIODE 1
D12 N29 N30 M1MP5DIODE 1
D13 0 N31 M1MP5DIODE 1
D14 VBP N34 M1MP5DIODE 2
D15 N34 VBP M1MP5DIODE 2
D16 0 N34 M2MDCAP 12.5
D17 N35 0 M2MDCAP 12.5
D18 N35 VBN M1MP5DIODE 2
D19 VBN N35 M1MP5DIODE 2
D2 N15 0 M2MDCAP 12
D20 N42 N10 M2MDCAP 4
D21 N10 0 M2MDCAP 4
D22 0 N20 M2MDCAP 4
D23 N20 N45 M2MDCAP 4
D3 0 N12 M1MP5DIODE 8
D4 N55 N13 M1MP5DIODE 8
D5 0 N25 M2MDCAP 6
D6 N25 0 M2MDECAP 6
D7 0 N22 M1MP5DIODE 8
D8 N54 N23 M1MP5DIODE 8
D9 0 N28 M1MP5DIODE 1
EV94 0 VBN 0 N45 1
```

Macromodel — Contd.

```
EV95 VBP 0 N42 0 1
EV96 N54 0 N21 0 650m
EV97 N55 0 N11 0 650m
EV98 N27 0 N28 0 1
EV99 N29 0 SWIN 0 1
FI10 VN-VEE VFI10 1
FI11 VCC VP-VFI11 1
FI12 VCC N39 VFI12 1
FI13 N37 VEE VFI13 1
FI14 VCC N38 VFI14 1
FI15 N36 VEE VFI15 1
FI16 N45 VEE VFI16 1
FI17 VCC N42 VFI17 1
FI18 N37 N36 VFI18 500m
FI19 N38 N39 VFI19 500m
FI20 VN+ VN- VFI20 500m
FI21 VP+ VP- VFI21 500m
FI22 0 N21 VFI22 1
FI23 N21 0 VFI23 1
FI24 N24 0 VFI24 2
FI25 N14 0 VFI25 2
FI26 N11 0 VFI26 1
FI27 0 N11 VFI27 1
FI28 VCC VEE VFI28 21
FI 29 N28 ZB1 VFI29 1
FI5 N33 0 VFI5 1
FI6 0 N33 VFI6 1
FI7 N35 N34 VFI7 1
FI8 VN+ VEE VFI8 1
FI9 VCC VP+ VFI9 1
IIBGN 0 VEE 2.2m
IIBGP VCC 0 2.46m
IIISWB N32 VEE 629u
IIISWI SWIN VEE 555u
IIZSU N28 VEE 10u
L1 N7 IXA 71n
L2 XIN N7 4n
L3 N16 IYA 71n
L4 YIN N16 4n
L5 N46 IYX 4n
L6 N47 IXY 4n
Q10 N10 VP+ [VEE] M4MPNP1 2
Q10 N46 VN+ N36[VEE] M3MNPN1 2
Q11 N47 VN+ N37 [VEE] M3MNPN1 2
Q12 N46 VN- N37 [VEE] M3MNPN1 2
Q13 0 N34 N56 [VEE] M4MPNP1 400m
Q14 0 N34 N57 [VEE] M4MPNP1 400m
Q15 0 N35 N58 [VEE] M3MNPN1 400m
Q16 0 N35 N59 [VEE] M3MNPN1 400m
Q2 0 N10 VP- [VEE] M4MPNP1 2
Q3 0 N20 VN+ [VEE] M3MNPN1 2
Q4 0 N20 VN- [VEE] M3MNPN1 2
Q5 N46 VP- N39 [VEE] M4MPNP1 2
Q6 N47 VP+ N39 [VEE] M4MPNP1 2
Q7 N46 VP+ N38 [VEE] M4MPNP1 2
Q8 N47 VP- N38 [VEE] M4MPNP1 2
Q9 N47 VN- N36 [VEE] M3MNPN1 2
R1 N15 N7 60 TC=824u 7.67u
R10 N16 N17 450 TC=0 0
R11 YIN N16 100 TC=0 0
R12 0 SWIN 500 TC=824u 7.67u
R13 N56 N38 35 TC=0 0
R14 N57 N39 35 TC=0 0
R15 N37 N58 35 TC=0 0
R16 N36 N59 35 TC=0 0
R17 N46 IYX 100 TC=0 0
R18 N47 IXY 100 TC=0 0
R2 N11 IXC 6.25 TC=0 0
R3 N9 IXC 4.5 TC=0 0
R4 N7 IXA 1.5K TC=0 0
R5 XIN N7 100 TC=0 0
R6 N25 N16 156 TC=824u 7.67u
R7 N21 IYC 6.25 TC=0 0
R8 ITC N19 45 TC=0 0
R9 N17 IYA 45 TC=0 0
RSU VEE 0 16K TC=0 0
VFI10 N43 N44 0.0
VFI11 N40 N41 0.0
VFI12 ZB4 ZB5 0.0
VFI13 ZB5 ZB6 0.0
VFI14 ZB3 ZB4 0.0
VFI15 ZB6 ZB7 0.0
VFI16 N44 ZB9 0.0
VFI17 N41 ZB8 0.0
VFI18 IYB IYC 0.0
VFI19 IYA IYB 0.0
VFI20 IXB IXC 0.0
VFI21 IXA IXB 0.0
VFI22 N22 N24 0.0
VFI23 N23 N24 0.0
VFI24 ZB2 ZB3 0.0
VFI25 ZB1 ZB2 0.0
VFI26 N13 N14 0.0
VF127 N12 N14 0.0
VFI28 ZB9 VEE 0.0
VFI29 ZIN N26 0.0
VF15 N30 N32 0.0
VFI6 N31 N32 0.0
VFI7 N33 0 0.0
VFI8 ZB8 N43 0.0
VFI9 ZB7 N40 0.0
.ENDS
```

EL4083C
Current Mode Four Quadrant Multiplier

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