Data Sheet

CADEKA
Amplify the Human Experience

COMLINEAR® CLC1004, CLC1014, CLC3004

Single and Triple, 750MHz Amplifiers with Disable

FEATURES

- 0.1dB gain flatness to 200MHz
- 0.02%/0.01° differential gain/phase
- 750MHz -3dB bandwidth at G = 2
- 350MHz large signal bandwidth
- 1,400V/µs slew rate
- 4nV/√Hz input voltage noise
- 100mA output current
- 20ns enable time
- Stable for gains of 2V/V or larger
- Fully specified at 5V and ±5V supplies
- CLC1004: Pb-free SOT23-6
- CLC1014: Pb-free SOT23-5
- CLC3004: Pb-free SOIC-16

APPLICATIONS

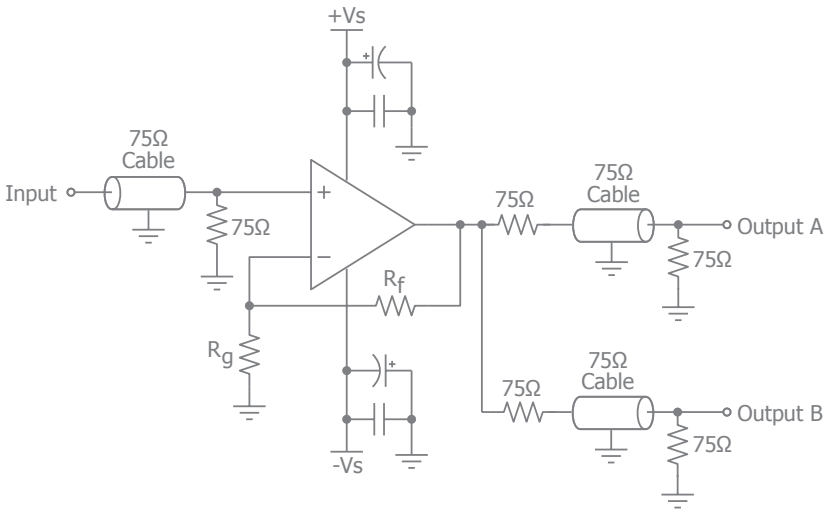
- RGB video line drivers
- High definition video driver
- Video switchers and routers
- ADC buffer
- Active filters
- Cable drivers
- Imaging applications
- Radar/communication receivers

General Description

The COMLINEAR CLC1004 (single with disable), CLC1014 (single), and CLC3004 (triple with disable) are high-performance, voltage feedback amplifiers that provide 750MHz gain of 2 bandwidth, ±0.1dB gain flatness to 200MHz, and 1,400V/µs slew rate. This high performance exceeds the requirements of high-definition television (HDTV) and other multimedia applications. These COMLINEAR high-performance amplifiers also provide ample output current to drive multiple video loads.

The COMLINEAR CLC1004, CLC1014, and CLC3004 are designed to operate from ±5V or +5V supplies. The CLC1004 and CLC3004 offer a fast enable/disable feature to save power. While disabled, the outputs are in a high-impedance state to allow for multiplexing applications. The combination of high-speed, low-power, and excellent video performance make these amplifiers well suited for use in many general purpose, high-speed applications including video line driving and imaging applications.

Typical Application - Driving Multiple Video Loads

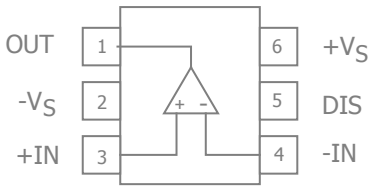


Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1004IST6X	SOT23-6	Yes	Yes	-40°C to +85°C	Reel
CLC1004IST6	SOT23-6	Yes	Yes	-40°C to +85°C	Rail
CLC1014IST5X	SOT23-5	Yes	Yes	-40°C to +85°C	Reel
CLC1014IST5	SOT23-5	Yes	Yes	-40°C to +85°C	Rail
CLC3004ISO16X	SOIC-16	Yes	Yes	-40°C to +85°C	Reel
CLC3004ISO16	SOIC-16	Yes	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

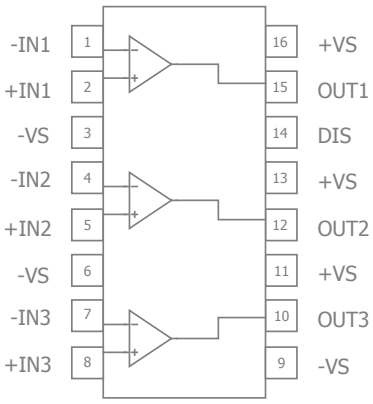
CLC1004 Pin Configuration



CLC1004 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	DIS	Disable pin. Enabled if pin is grounded, left floating or pulled below V_{ON}, disabled if pin is pulled above V_{OFF}.
6	$+V_S$	Positive supply

CLC3004 Pin Configuration



CLC3004 Pin Configuration

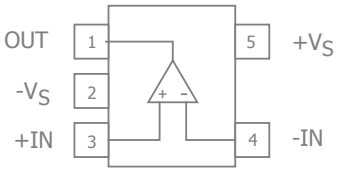
Pin No.	Pin Name	Description
1	-IN1	Negative input, channel 1
2	+IN1	Positive input, channel 1
3	$-V_S$	Negative supply
4	-IN2	Negative input, channel 2
5	+IN2	Positive input, channel 2
6	$-V_S$	Negative supply
7	-IN3	Negative input, channel 3
8	+IN3	Positive input, channel 3
9	$-V_S$	Negative supply
10	OUT3	Output, channel 3
11	$+V_S$	Positive supply
12	OUT2	Output, channel 2
13	$+V_S$	Positive supply
14	DIS	Disable pin. Enabled if pin is grounded, left floating or pulled below V_{ON}, disabled if pin is pulled above V_{OFF}.
15	OUT1	Output, channel 1
16	$+V_S$	Positive supply

Disable Pin Truth Table

Pin	High	Low*
DIS	Disabled	Enabled

*Default Open State

CLC1014 Pin Configuration



CLC1014 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V
Continuous Output Current		100	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
6-Lead SOT23		177		°C/W
16-Lead SOIC		68		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOT23-5	SOT23-6	SOIC-16
Human Body Model (HBM)	2kV	2kV	2kV
Charged Device Model (CDM)	1kV	1kV	1kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	4.5		12	V

Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = R_g =150Ω, R_L = 150Ω to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		600		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 1V_{pp}		400		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		150		MHz
$BW_{0.1dBLS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 1V_{pp}		120		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		1.2		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		10		ns
OS	Overshoot	V_{OUT} = 0.2V step		2		%
SR	Slew Rate	1V step		750		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		-72		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		-85		dBc
THD	Total Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		70		dB
D_G	Differential Gain	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.08		%
D_P	Differential Phase	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.04		°
IP3	Third Order Intercept	V_{OUT} = 1V_{pp}, 10MHz		38		dBm
SFDR	Spurious Free Dynamic Range	V_{OUT} = 1V_{pp}, 5MHz		63		dBc
e_n	Input Voltage Noise	> 1MHz		4		nV/√Hz
i_n	Input Current Noise	> 1MHz		4		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz, V_{OUT} = 1V_{pp}		70		dB
DC Performance						
V_{IO}	Input Offset Voltage			0		mV
dV_{IO}	Average Drift			4		µV/°C
I_b	Input Bias Current			3.2		µA
dI_b	Average Drift			20		nA/°C
PSRR	Power Supply Rejection Ratio	DC		56		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2		65		dB
I_S	Supply Current	per channel		11		mA
Disable Characteristics						
T_{ON}	Turn On Time			20		ns
T_{OFF}	Turn Off Time			40		ns
OFF_{IOS}	Off Isolation	5MHz		-78		dB
V_{OFF}	Power Down Input Voltage	DIS pin, disabled if pin is pulled above V_{OFF} = V_s - 2V	Disabled if > (V_s - 2V)			V
V_{ON}	Enable Input Voltage	DIS pin, enabled if pin is grounded, left open, or pulled below V_{ON} = V_s - 4V	Enabled if < (V_s - 4V)			V
I_{SD}	Disable Supply Current	CLC1004; DIS pin is pulled to V_S		0.4		mA
		CLC3004; DIS pin is pulled to V_S		0.4		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4.5		MΩ
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			1.5 to 3.5		V
CMRR	Common Mode Rejection Ratio	DC		50		dB

Electrical Characteristics at +5V continued

T_A = 25°C, V_s = +5V, R_f = R_g =150Ω, R_L = 150Ω to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.1		Ω
V_{OUT}	Output Voltage Swing	R_L = 150Ω		1.5 to 3.5		V
I_{OUT}	Output Current			±100		mA

Notes:

1. 100% tested at 25°C

Electrical Characteristics at ±5V

T_A = 25°C, V_S = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		750		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		350		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		200		MHz
$BW_{0.1dBLS}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 2V_{pp}		120		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 2V step; (10% to 90%)		1.3		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		10		ns
OS	Overshoot	V_{OUT} = 0.2V step		1.5		%
SR	Slew Rate	2V step		1400		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		-71		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		-82		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		70		dB
D_G	Differential Gain	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.02		%
D_P	Differential Phase	NTSC (3.58MHz), AC-coupled, R_L = 150Ω		0.01		°
IP3	Third Order Intercept	V_{OUT} = 2V_{pp}, 10MHz		41		dBm
SFDR	Spurious Free Dynamic Range	V_{OUT} = 1V_{pp}, 5MHz		65		dBc
e_n	Input Voltage Noise	> 1MHz		4		nV/√Hz
i_n	Input Current Noise	> 1MHz		4		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz, V_{OUT} = 2V_{pp}		70		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-10	0	10	mV
dV_{IO}	Average Drift			4		µV/°C
I_b	Input Bias Current (1)		-20	3.2	20	µA
dI_b	Average Drift			20		nA/°C
PSRR	Power Supply Rejection Ratio (1)	DC	40	56		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2		70		dB
I_S	Supply Current (1)	per channel		12	17	mA
Disable Characteristics						
T_{ON}	Turn On Time			20		ns
T_{OFF}	Turn Off Time			40		ns
OFF_{IOS}	Off Isolation	5MHz		-78		dB
V_{OFF}	Power Down Input Voltage	DIS pin, disabled if pin is pulled above V_{OFF} = V_s - 1V	Disabled if > (V_s - 1V)			V
V_{ON}	Enable Input Voltage	DIS pin, enabled if pin is grounded, left open, or pulled below V_{ON} = V_s - 2V	Enabled if < (V_s - 2V)			V
I_{SD}	Disable Supply Current (1)	CLC1004; DIS pin is pulled to V_S		0.4	0.8	mA
		CLC3004; DIS pin is pulled to V_S		0.4	0.9	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4.5		MΩ
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			±3.2		V
CMRR	Common Mode Rejection Ratio (1)	DC	40	60		dB

Electrical Characteristics at ±5V continued

T_A = 25°C, V_s = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.1		Ω
V_{OUT}	Output Voltage Swing	R_L = 150Ω (1)	±3.0	±3.8		V
I_{OUT}	Output Current			±220		mA

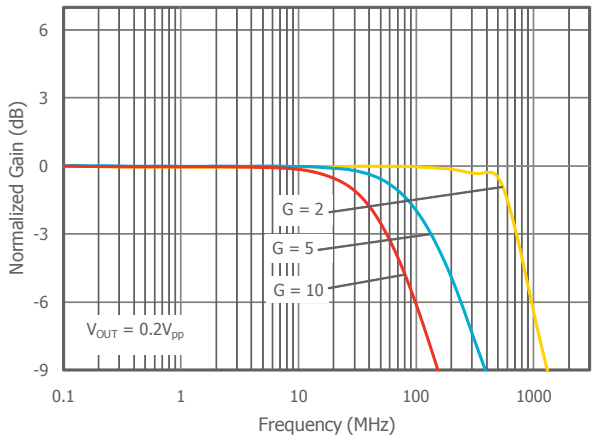
Notes:

1. 100% tested at 25°C

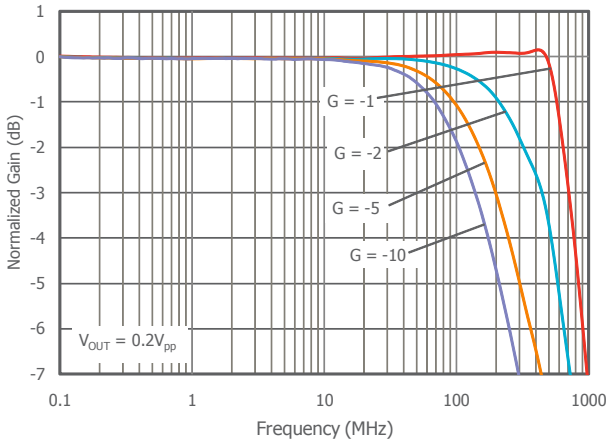
Typical Performance Characteristics

T_A = 25°C, V_s = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

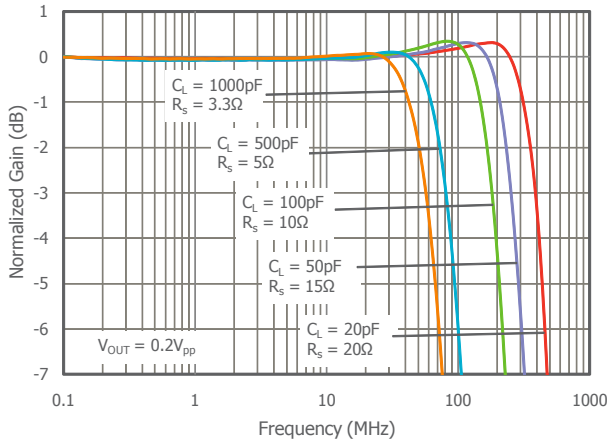
Non-Inverting Frequency Response



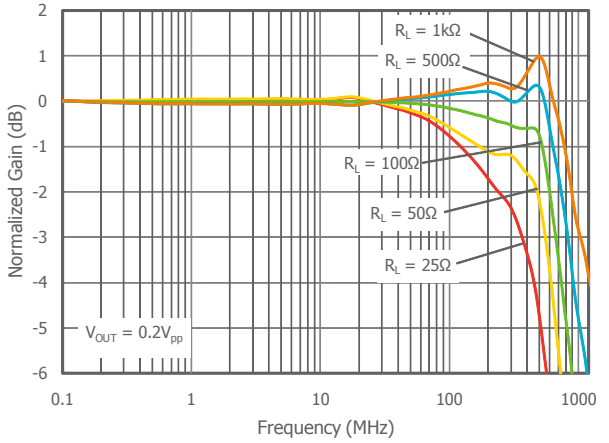
Inverting Frequency Response



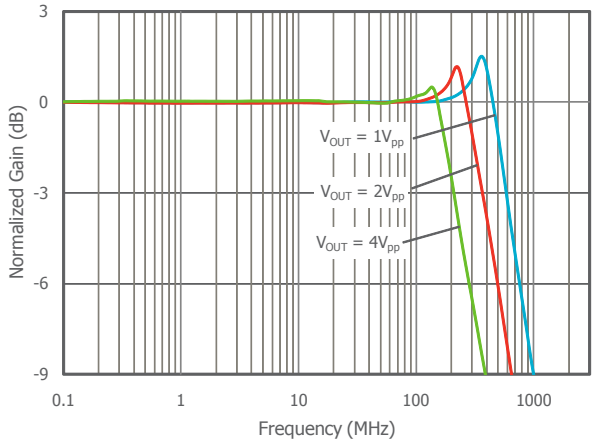
Frequency Response vs. C_L



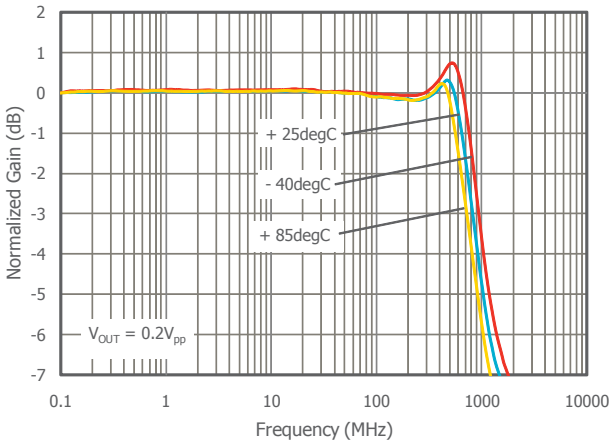
Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



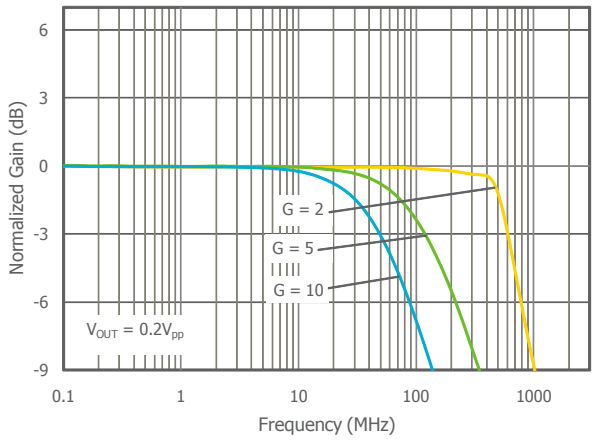
Frequency Response vs. Temperature



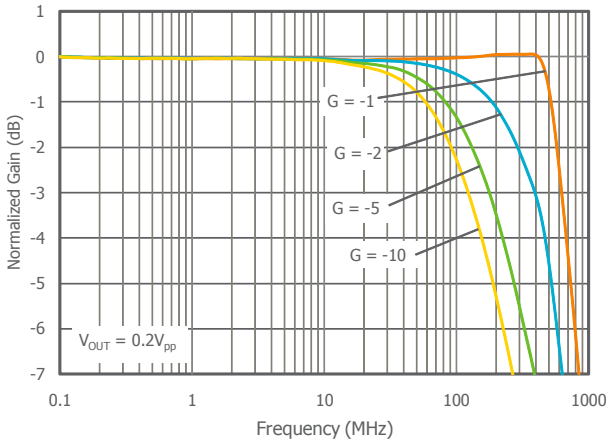
Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

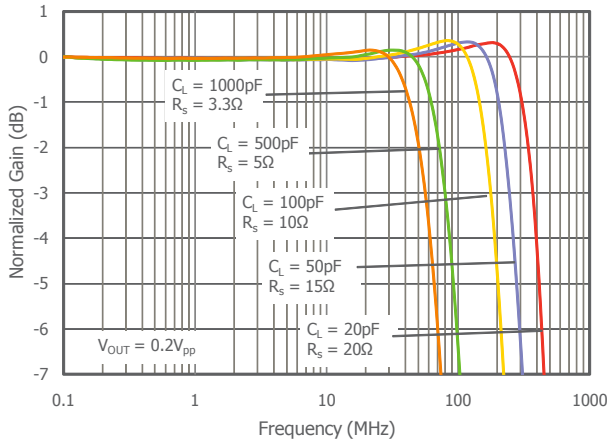
Non-Inverting Frequency Response at V_S = 5V



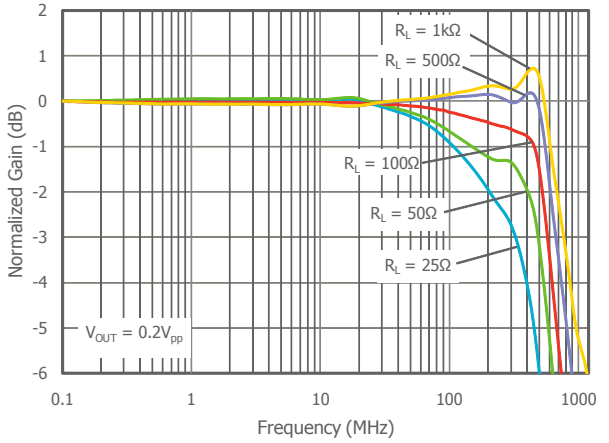
Inverting Frequency Response at V_S = 5V



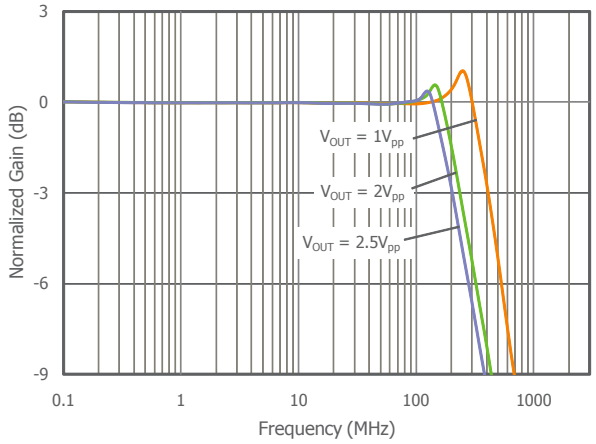
Frequency Response vs. C_L at V_S = 5V



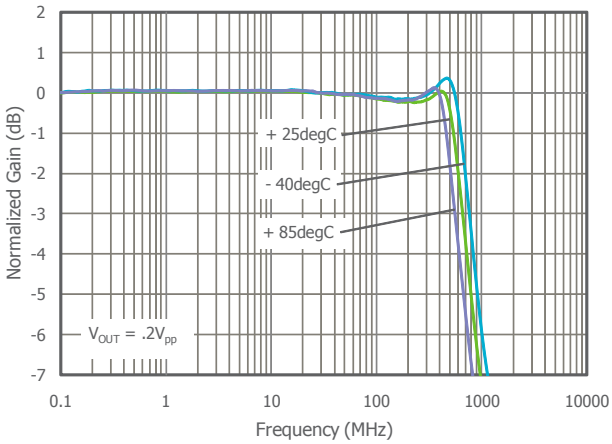
Frequency Response vs. R_L at V_S = 5V



Frequency Response vs. V_{OUT} at V_S = 5V



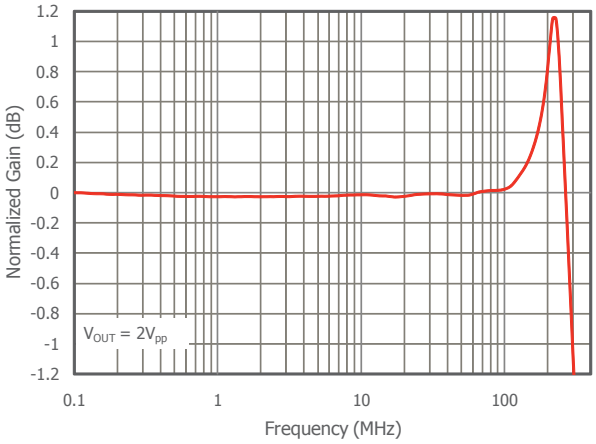
Frequency Response vs. Temperature at V_S = 5V



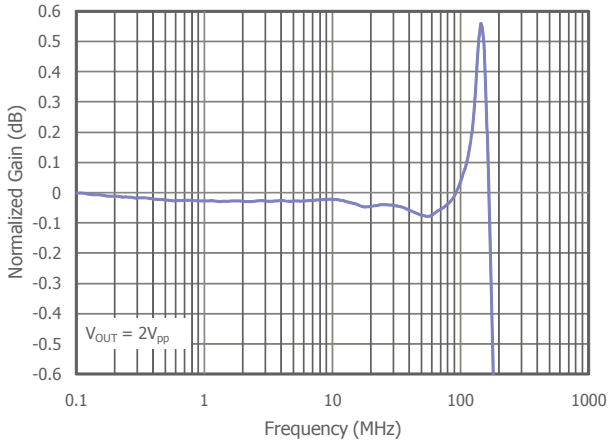
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

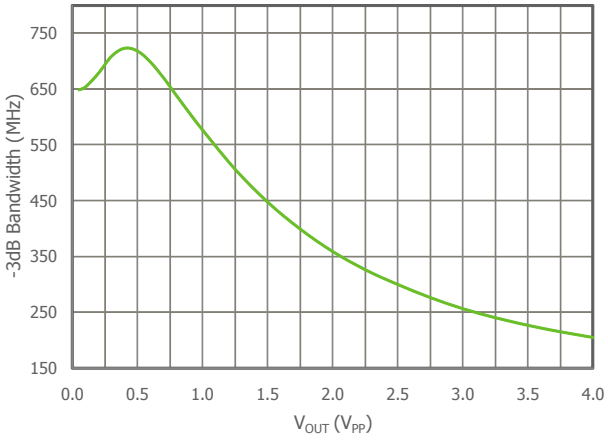
Gain Flatness



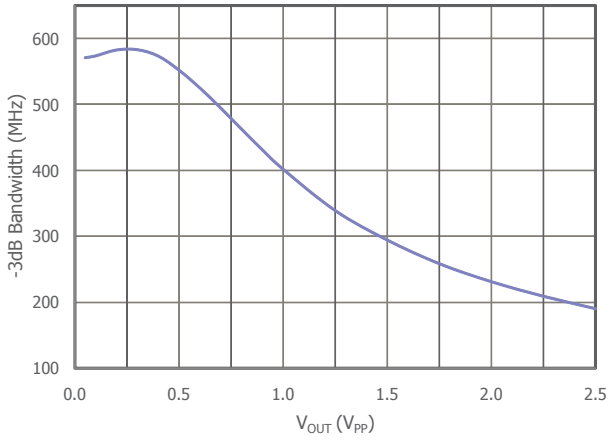
Gain Flatness at V_S = 5V



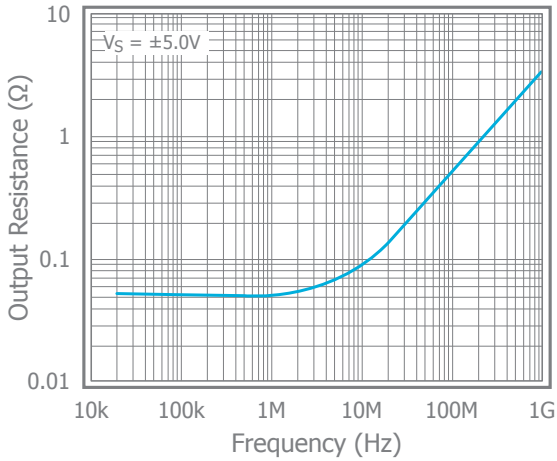
-3dB Bandwidth vs. V_{OUT}



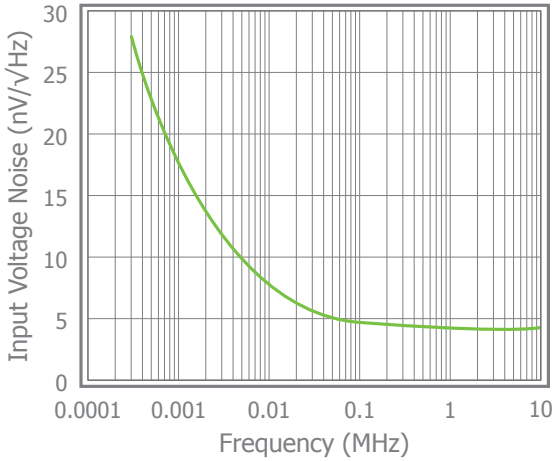
-3dB Bandwidth vs. V_{OUT} at V_S = 5V



Closed Loop Output Impedance vs. Frequency



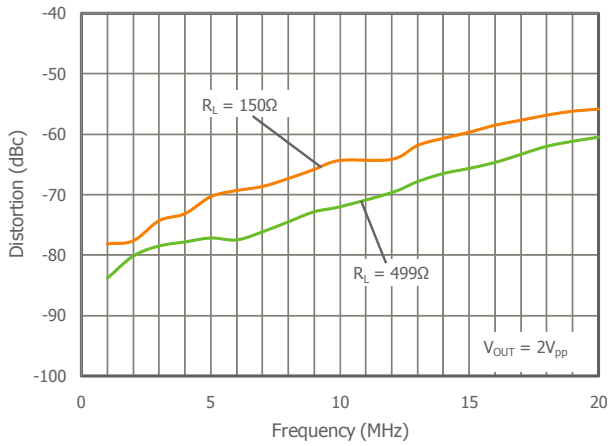
Input Voltage Noise



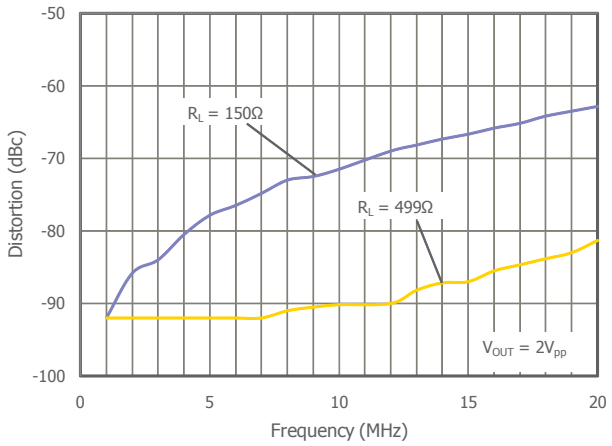
Typical Performance Characteristics - Continued

T_A = 25°C, V_s = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

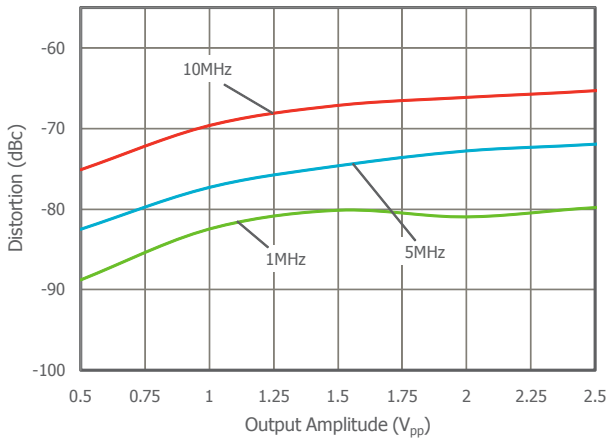
2nd Harmonic Distortion vs. R_L



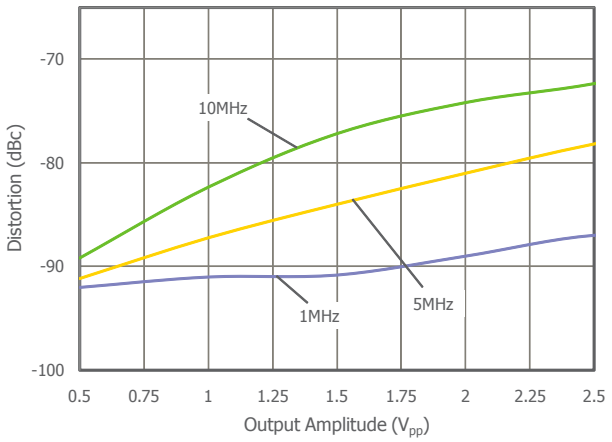
3rd Harmonic Distortion vs. R_L



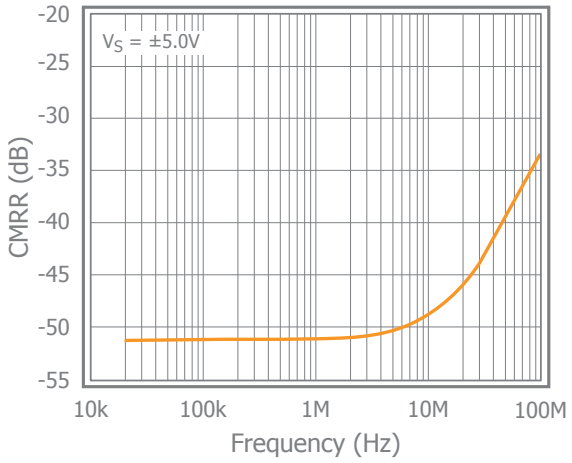
2nd Harmonic Distortion vs. V_{OUT}



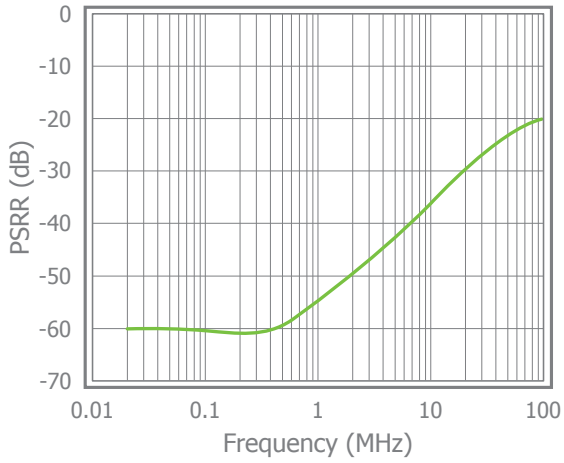
3rd Harmonic Distortion vs. V_{OUT}



CMRR vs. Frequency



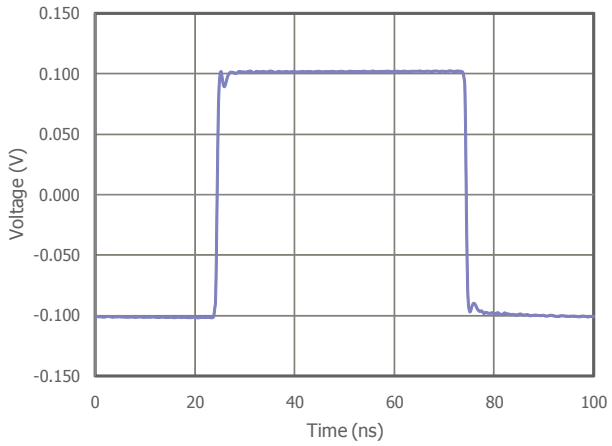
PSRR vs. Frequency



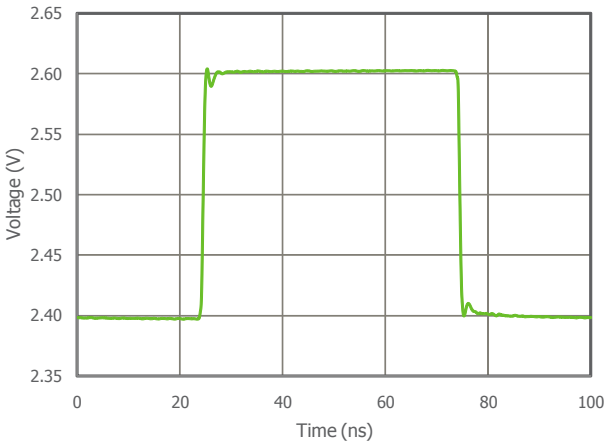
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

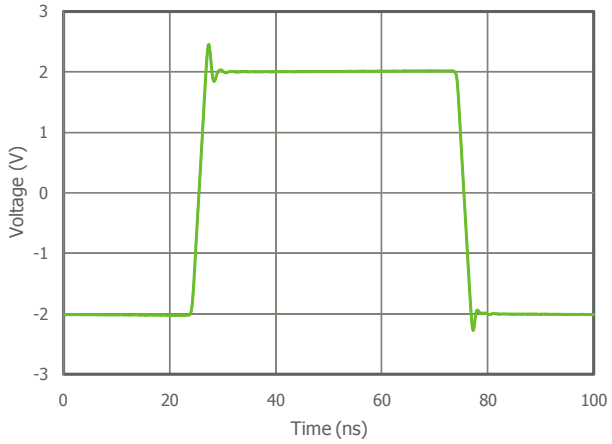
Small Signal Pulse Response



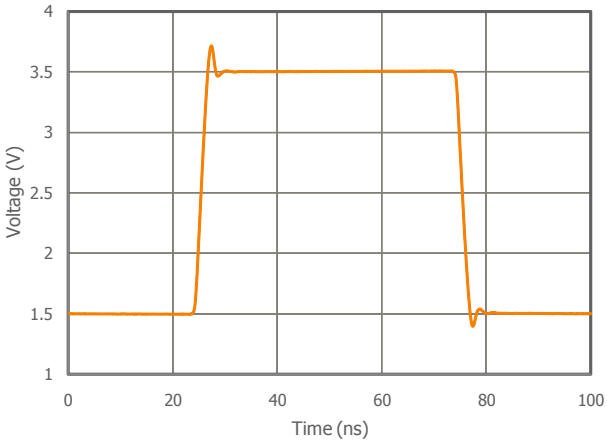
Small Signal Pulse Response at V_S = 5V



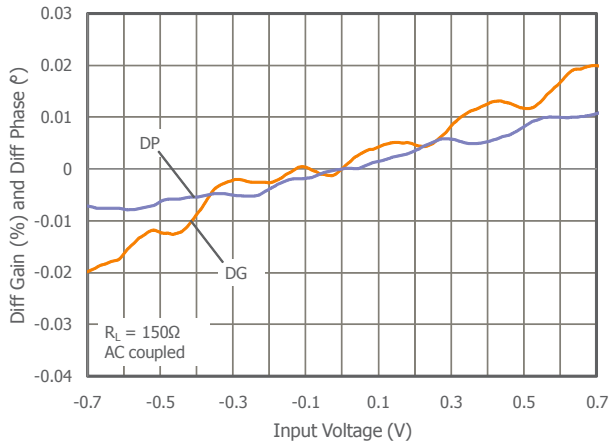
Large Signal Pulse Response



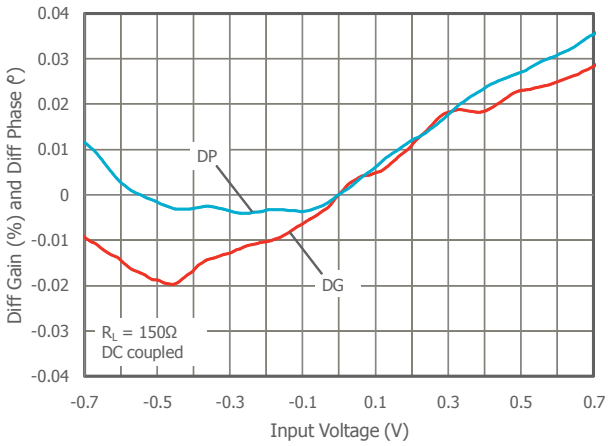
Large Signal Pulse Response at V_S = 5V



Differential Gain & Phase AC Coupled Output



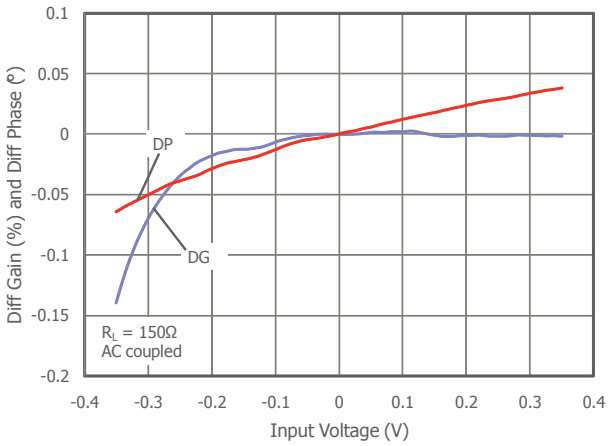
Differential Gain & Phase DC Coupled Output



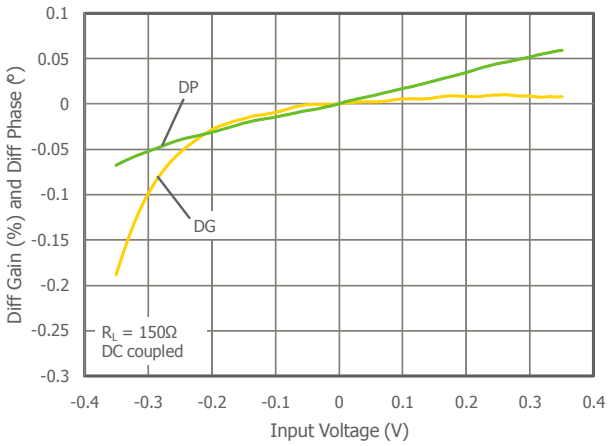
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = ±5V, R_f = R_g =150Ω, R_L = 150Ω, G = 2; unless otherwise noted.

Differential Gain & Phase AC Coupled Output at V_S = ±2.5V



Differential Gain & Phase DC Coupled at V_S = ±2.5V



Application Information

Basic Operation

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

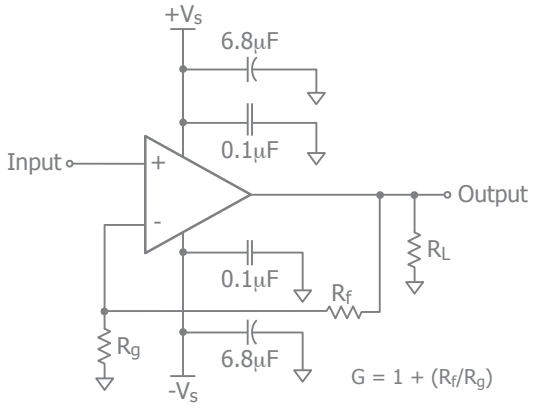


Figure 1. Typical Non-Inverting Gain Circuit

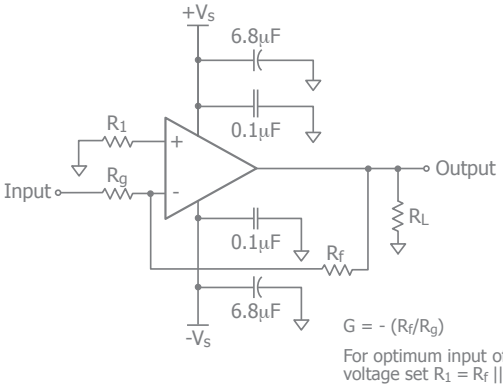


Figure 2. Typical Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 1000 ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$P_D = P_{supply} - P_{load}$

Supply power is calculated by the standard power equation.

$P_{supply} = V_{supply} \times I_{RMS\ supply}$

$V_{supply} = V_{S+} - V_{S-}$

Power delivered to a purely resistive load is:

$P_{load} = ((V_{LOAD})_{RMS^2})/Rload_{eff}$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 3 would be calculated as:

$R_L \,||\, (R_f + R_g)$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$

$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

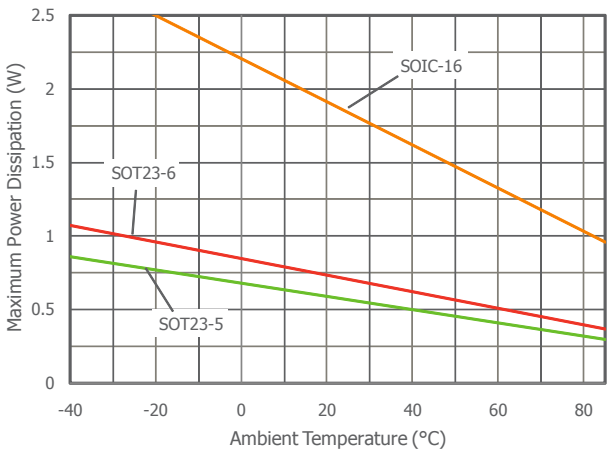


Figure 3. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 4.

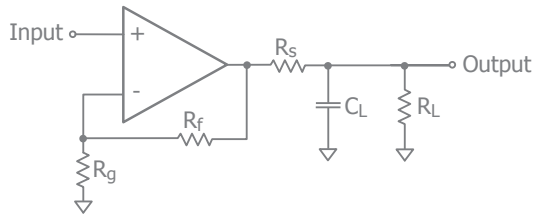


Figure 4. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in <=1dB peaking in the frequency response. The Frequency Response vs. C_L plots, on page 7, illustrates the response of the CLCx004.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
20	20	400
50	15	270
100	10	195
500	5	80
1000	3.3	58

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLCx004 will typically recover in less than 20ns from an overdrive condition. Figure 5 shows the CLC1004 in an overdriven condition.

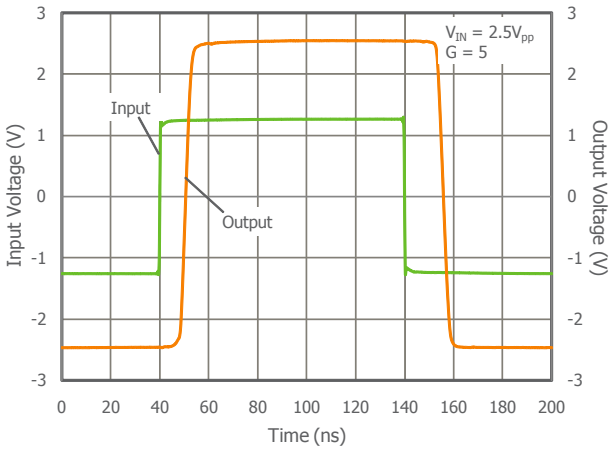


Figure 5. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1004, CLC1014
CEB012	CLC3004

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-14. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.

2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

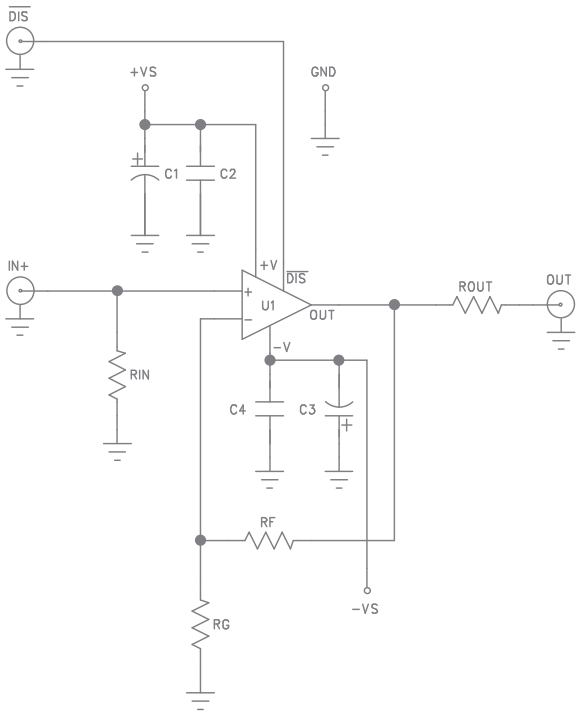


Figure 9. CEB002 Schematic

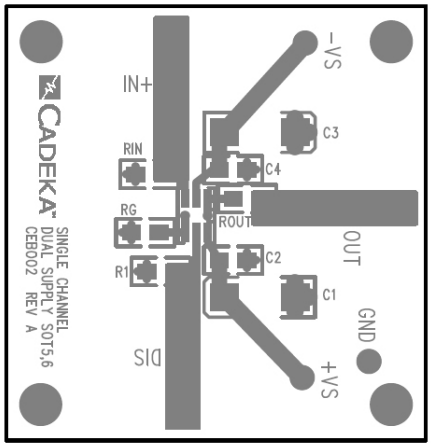


Figure 10. CEB002 Top View

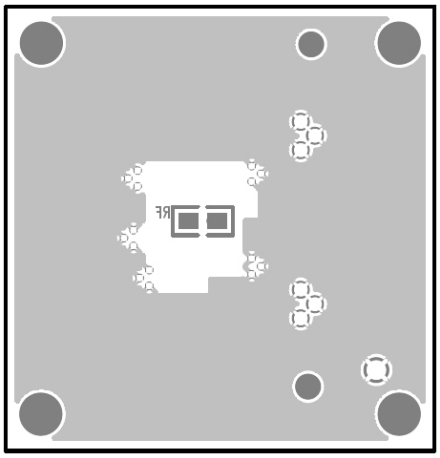


Figure 11. CEB002 Bottom View

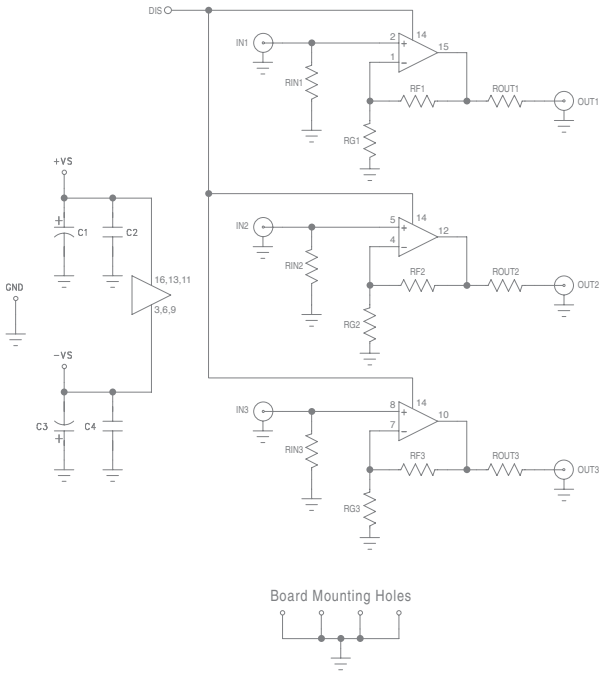


Figure 12. CEB012 Schematic

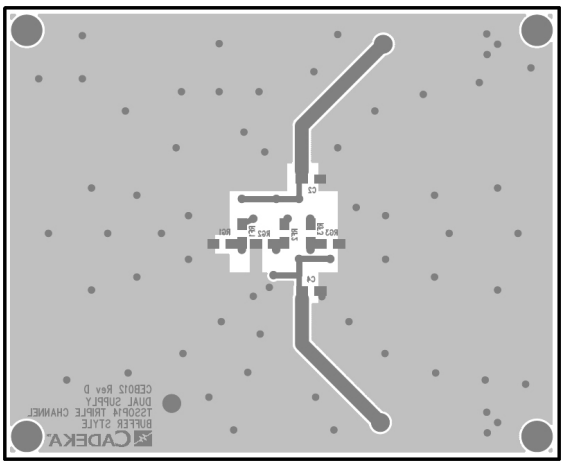


Figure 14. CEB012 Bottom View

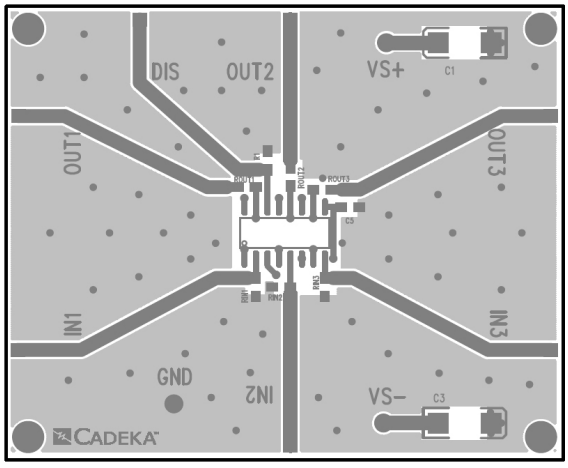
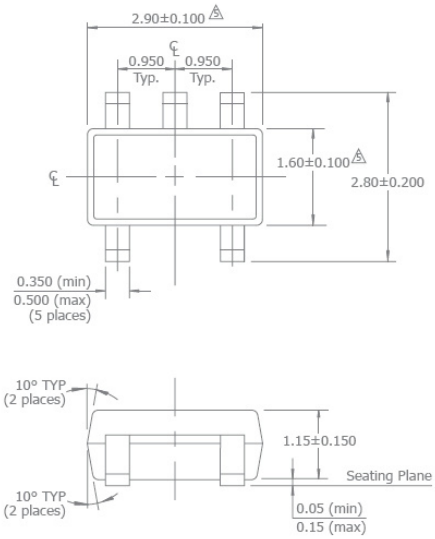


Figure 13. CEB012 Top View

Mechanical Dimensions

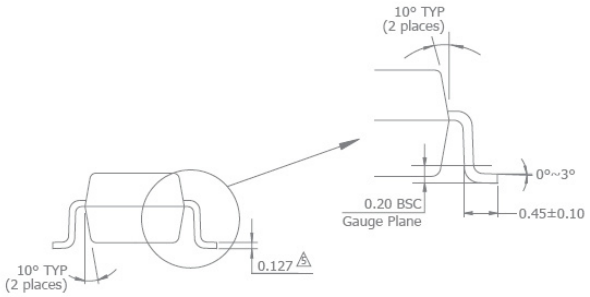
SOT23-5 Package



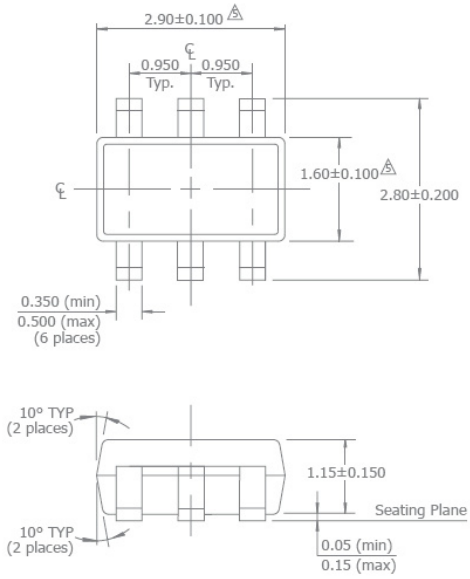
NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.

Ⓑ Dimension are exclusive of mold flash and gate burr.
Ⓑ Dimension are exclusive of solder plating.



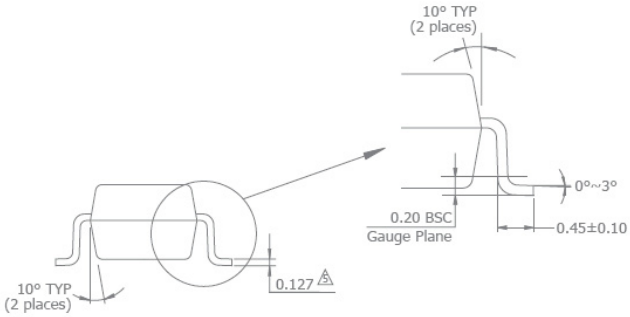
SOT23-6 Package



NOTES:

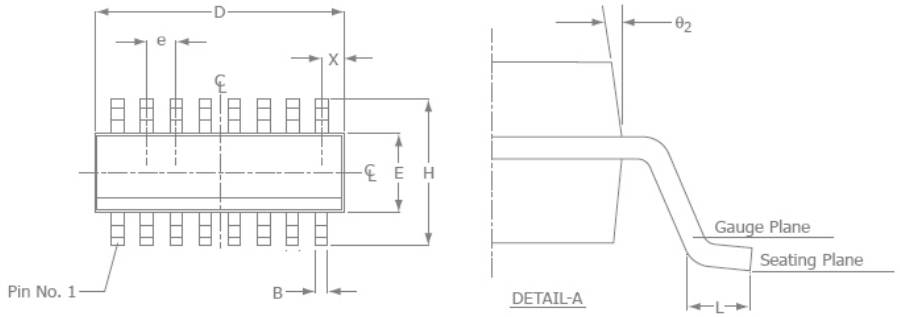
1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.

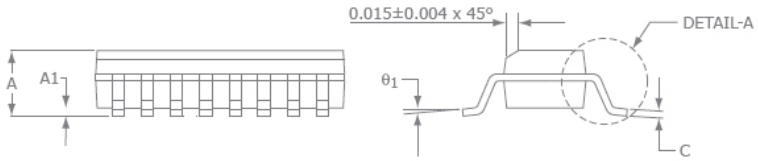
Ⓑ Dimension are exclusive of mold flash and gate burr.
Ⓑ Dimension are exclusive of solder plating.



Mechanical Dimensions

SOIC-16 Package





SOIC-16		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 Ref	
θ_1	0°	8°
θ_2	7° BSC	

NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

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