BURR - BROWN®

OPA644

Low Distortion Current Feedback OPERATIONAL AMPLIFIER

FEATURES

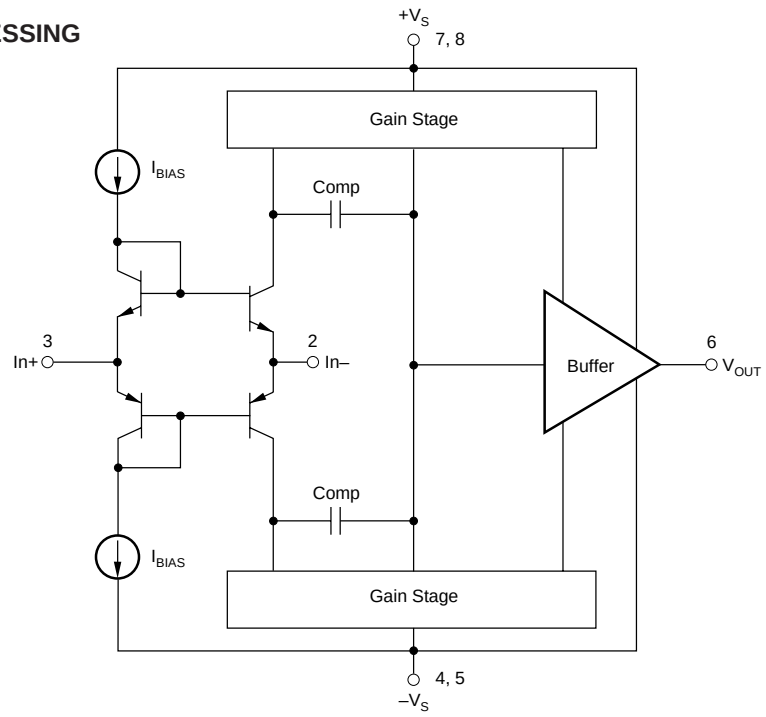
- SLEW RATE: 2500V/μs
- VERY LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.008%/0.009°
- LOW DISTORTION AT 5MHz: –85dBc
- HIGH BANDWIDTH: 500MHz
- HIGH OPEN LOOP TRANSIMPEDANCE: 2.0MΩ
- HIGH LINEARITY
- FAST 12-BIT SETTLING: 21ns to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- COMMUNICATIONS
- ADC/DAC GAIN AMPLIFIER
- RF AMPLIFICATION
- MEDICAL IMAGING
- AUDIO AMPLIFICATION

DESCRIPTION

The OPA644 is a wideband precision current feedback operational amplifier featuring exceptionally high open loop transimpedance and high slew rate. The current feedback architecture allows for excellent large signal bandwidth, even at high gains. The high transimpedance allows this op amp to be used in applications requiring 16 bits or more of accuracy. This extra transimpedance at high bandwidths gives very low distortion and low differential gain and phase errors. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA644 offers exceptional performance in monolithic form.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1187D
Printed in U.S.A. March, 1998

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used, unless otherwise noted.

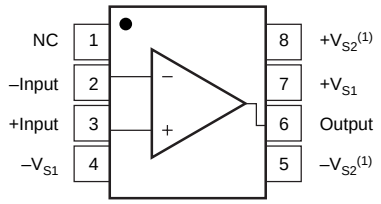
PARAMETER	CONDITIONS	OPA644U			OPA644UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±2.5	±6		±2	±3	mV
Average Drift			20			10		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±5.5V	40	65		60	75		dB
INPUT BIAS CURRENT(1)								
Non-Inverting			±20	±40		±15	±20	µA
Over Specified Temperature			±24	±90		±20	±50	µA
Inverting			±2	±25		*	±10	µA
Over Specified Temperature			±4	±35		±3	±25	µA
NOISE								
Input Voltage Noise Density								
f = 100Hz			10.3			*		nV/√Hz
f = 1kHz			2.9			*		nV/√Hz
f = 10kHz			1.9			*		nV/√Hz
f = 1MHz			1.9			*		nV/√Hz
f_B = 100Hz to 200MHz			33.6			*		µVrms
Inverting Input Bias Current								
Noise Density: f = 10MHz			15			*		pA/√Hz
Non-Inverting Input Current								
Noise Density: f = 10MHz			15			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.25		*	*		V
Over Specified Temperature		±1.8	±2.1		*	*		V
Common-Mode Rejection	V_{CM} = ±2V	35	55		45	65		dB
INPUT IMPEDANCE								
Non-Inverting			500 || 1.0			*		kΩ || pF
Inverting			20			46		Ω
Open-Loop Transimpedance	V_O = ±2V, R_L = 1kΩ	1.4	2.0		*	*		MΩ
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	G = +1V/V		500			*		MHz
	G = +2V/V		300			*		MHz
	G = +5V/V		180			*		MHz
	G = +10V/V		125			*		MHz
	G = +20V/V		80			*		MHz
Slew Rate(1)	G = +2, 2V Step		2500			*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		21			*		ns
0.1%	G = +2, 2V Step		16.5			*		ns
1%	G = +2, 2V Step		5.5			*		ns
Overload Recovery Time(2)			60			*		ns
Spurious Free Dynamic Range	G = –1, f = 5.0MHz		84			86		dBc
	V_O = 2Vp-p							
	G = –1, f = 20MHz							dBc
Differential Gain Error at 3.58MHz	G = +2V/V, V_O = 0V to 1.4V		0.008			*		%
	R_L = 150Ω							
Differential Phase Error at 3.58MHz	G = +2V/V, V_O = 0V to 1.4V		0.009			*		Degrees
	R_L = 150Ω							
Gain Flatness to 1dB	G = +1		250			*		MHz
OUTPUT								
Current Output		±40	±60		±50	±66		mA
Over Specified Temperature		±30	±45		±40	±50		mA
Voltage Output	No Load							
Over Specified Temperature		±3.0	±3.5		*	*		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.75	±3.25		*	*		V
Short Circuit Current			75				*	mA
Output Resistance	1MHz, G = +2V/V		0.2				*	Ω
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current	T_{MIN} to T_{MAX}		±18	±26		*	*	mA
TEMPERATURE RANGE								
Specification: U		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
U, UB 8-Pin SO-8			125			*		°C/W

* Specification same as OPA644U.

NOTES: (1) Slew rate is rate of change from 10% to 90% of the output voltage step. (2) Time for the output to resume linear operation after saturation.

PIN CONFIGURATION (All Packages)

Top View **SO-8**



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA644U, UB	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) The "B" grade of the SO-8 package will be marked with a "B" by pin 8.

ABSOLUTE MAXIMUM RATINGS

Power Supply	±5.5VDC
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	±1.2V
Input Voltage Range	±V_S
Storage Temperature Range: U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO-8 3s)	+260°C
Junction Temperature (T_J)	+175°C

ELECTROSTATIC DISCHARGE SENSITIVITY

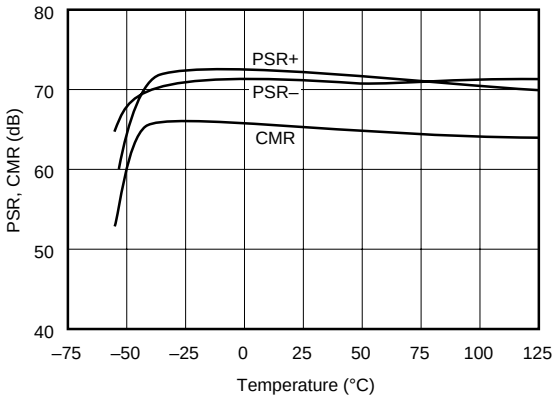
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

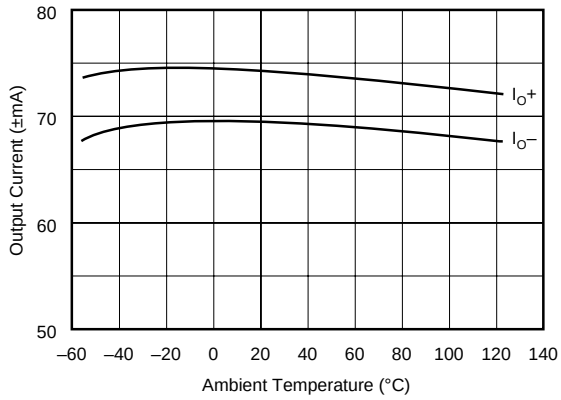
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

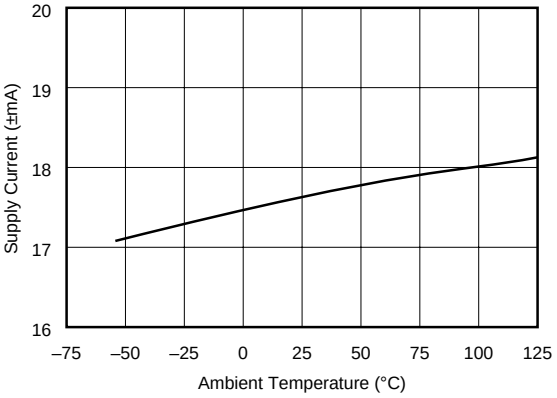
PSR AND CMR vs TEMPERATURE



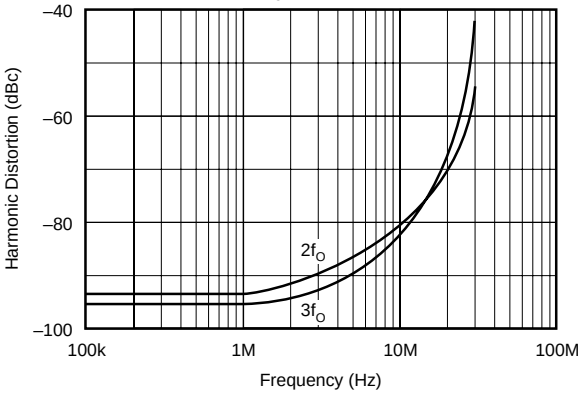
OUTPUT CURRENT vs TEMPERATURE



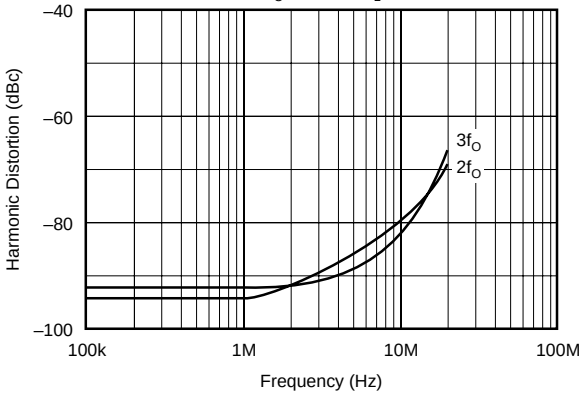
SUPPLY CURRENT vs TEMPERATURE



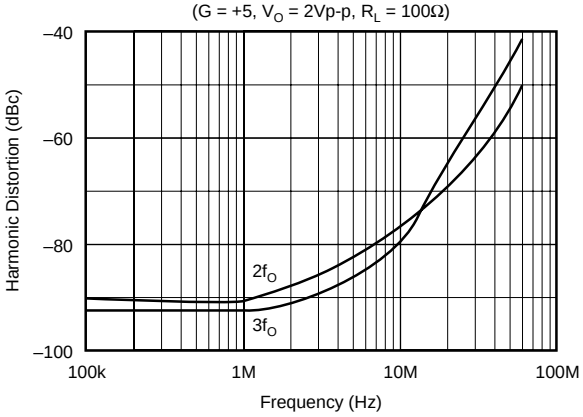
HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = 2Vp-p, R_L = 100Ω)



HARMONIC DISTORTION vs FREQUENCY
(G = –1, V_O = 2Vp-p, R_L = 100Ω)



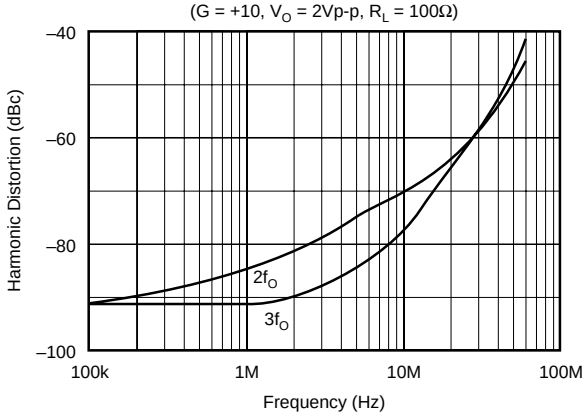
HARMONIC DISTORTION vs FREQUENCY
(G = +5, V_O = 2Vp-p, R_L = 100Ω)



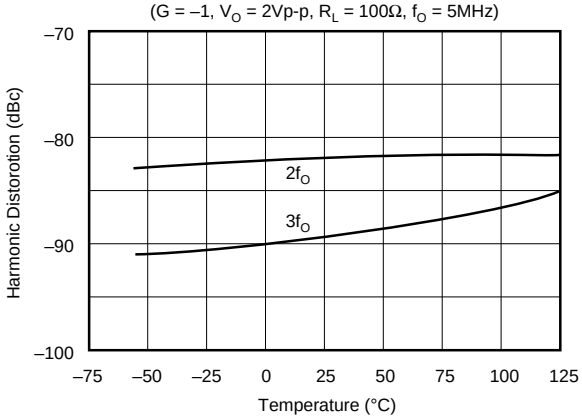
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

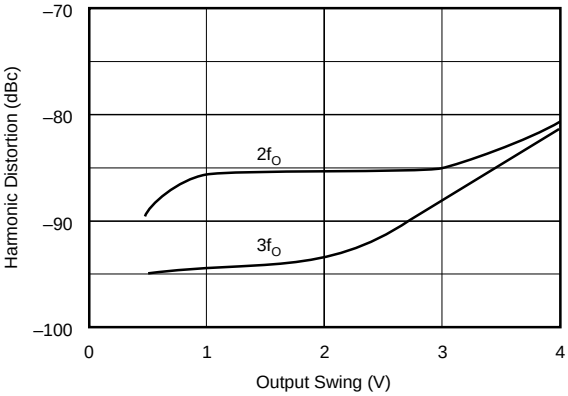
HARMONIC DISTORTION vs FREQUENCY
(G = +10, V_O = 2Vp-p, R_L = 100Ω)



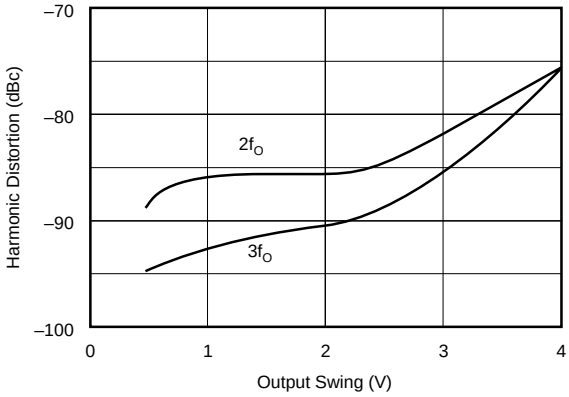
HARMONIC DISTORTION vs TEMPERATURE
(G = –1, V_O = 2Vp-p, R_L = 100Ω, f_O = 5MHz)



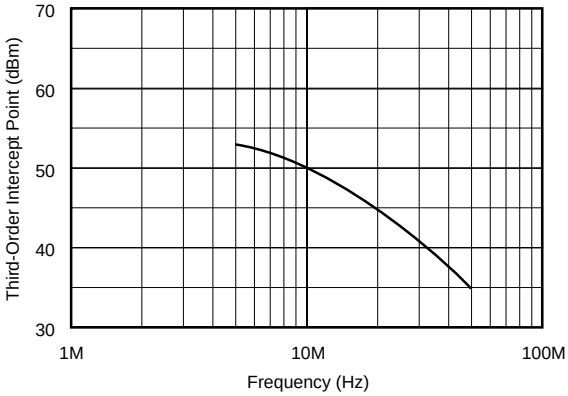
5MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = –1, R_L = 100Ω)



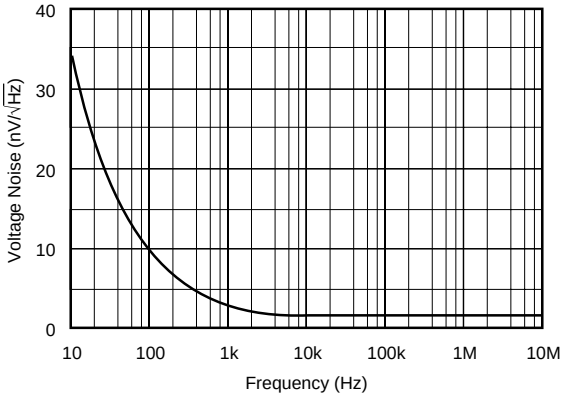
10MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = –1, R_L = 100Ω)



THIRD-ORDER INTERCEPT POINT vs FREQUENCY
(G = –1, R_L = 50Ω, R_{FB} = 402Ω)



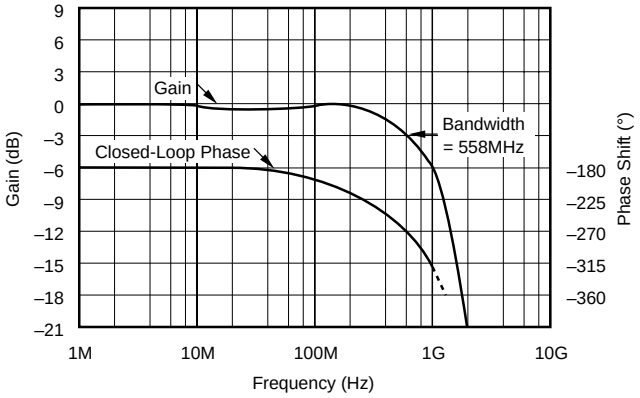
NON-INVERTING INPUT
VOLTAGE NOISE vs FREQUENCY
(G = +10)



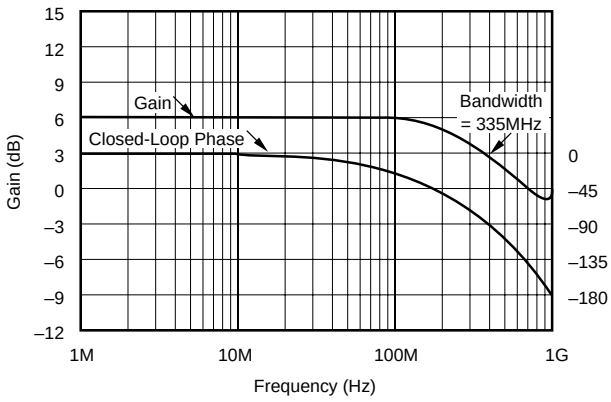
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used, unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

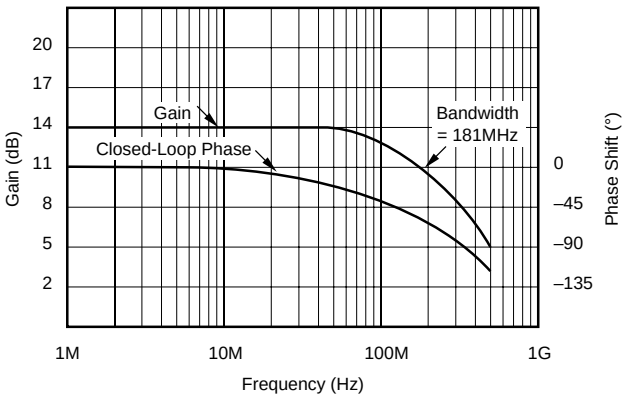
G = +1V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



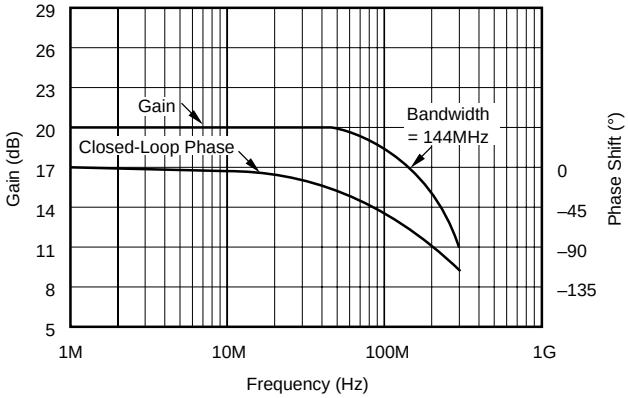
G = +2V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



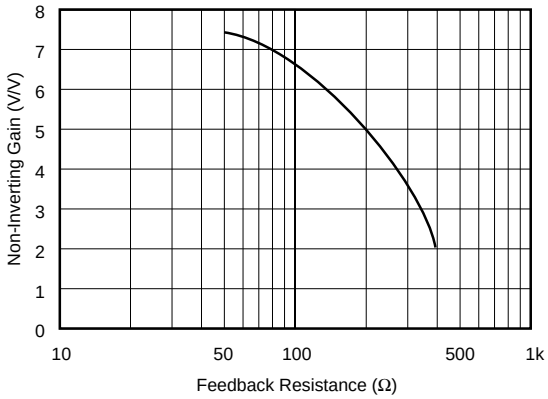
G = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



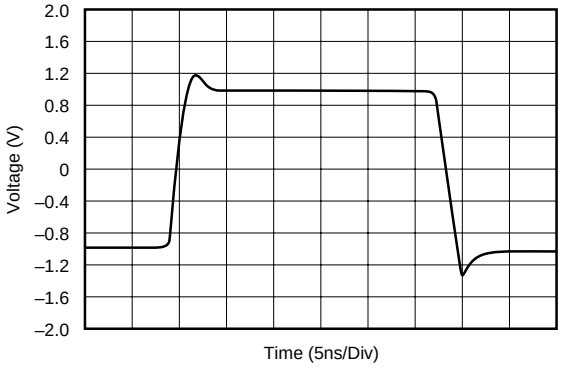
G = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



FEEDBACK RESISTOR
vs GAIN FOR OPTIMUM BANDWIDTH



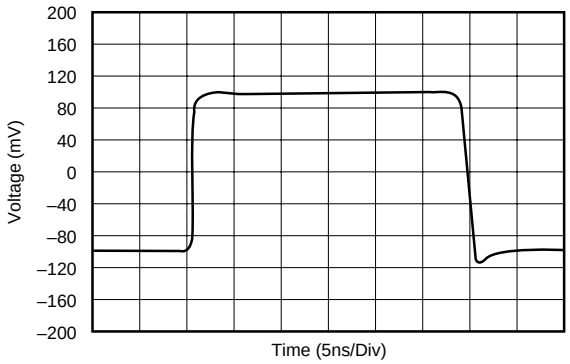
LARGE SIGNAL TRANSIENT RESPONSE
(G = +2, R_L = 100Ω)



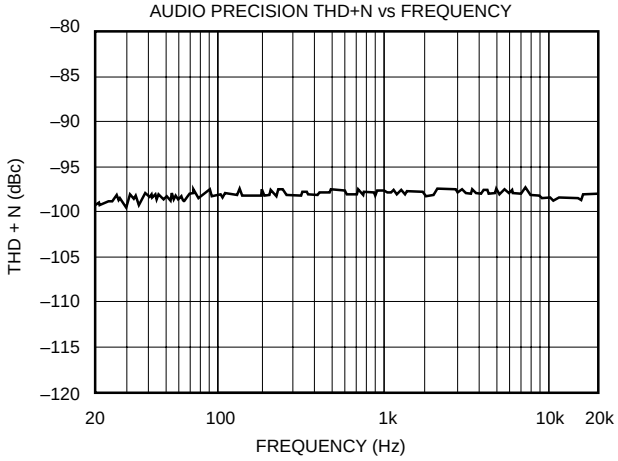
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless, otherwise noted. R_{FB} = 25Ω for a gain of +1.

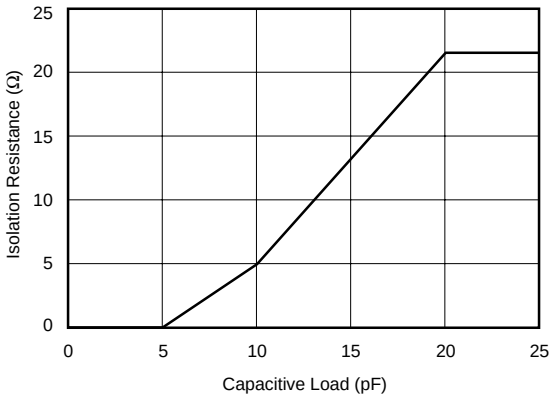
SMALL SIGNAL TRANSIENT RESPONSE
(G = +2, R_L = 100Ω)

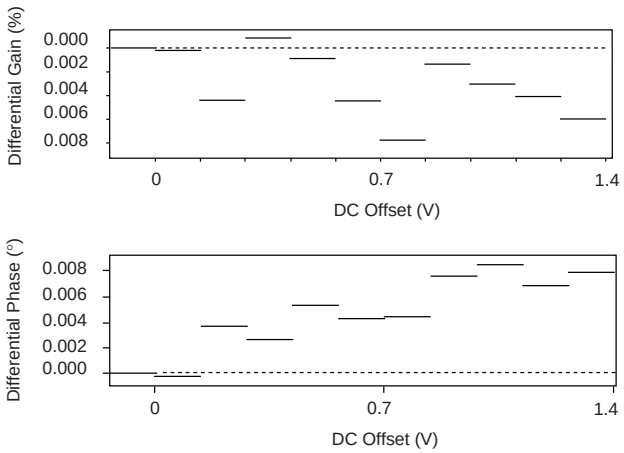


AUDIO PRECISION THD+N vs FREQUENCY



RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD





APPLICATIONS INFORMATION

THEORY OF OPERATION

This current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and: (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA644 provides the traditional strength of excellent large signal response with the unusual addition of very high open-loop transimpedance. This high open-loop transimpedance allows the OPA644 to be used in applications requiring 16 bits or more of accuracy and dynamic linearity.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open-loop transimpedance gain (T_O). The output signal generated is equal to T_O x I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

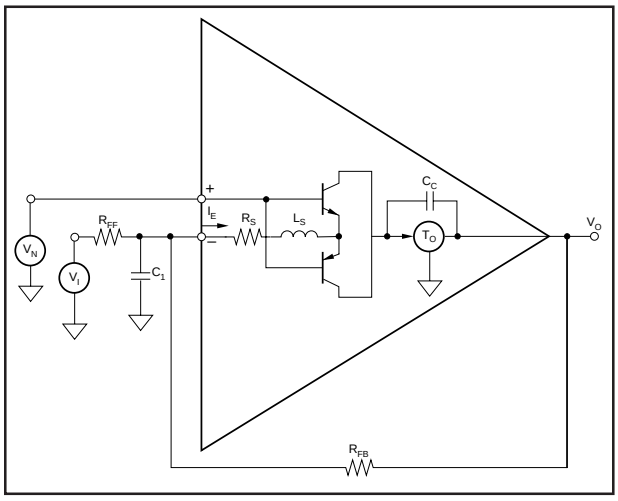


FIGURE 1. Equivalent Circuit.

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is ($1 + R_{FF}/R_I$).

Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA644 can be calculated using the following equations:

$$\text{Inverting Gain} = (-R_{FB}/R_{FF})/(1+1/\text{Loop Gain}) \quad (1)$$

$$\text{Non-inverting Gain} = (1 + R_{FB}/R_{FF})/(1 + 1/\text{Loop Gain}) \quad (2)$$

where: $\text{Loop Gain} = T(o)/(R_{FB}) \times (1/(1+T(o)/(R_{FB}/R_{FF}))$

At higher gains the small value inverting input impedance (R_{INV}) causes an apparent loss in bandwidth. This can be seen from the equation:

$$\text{Factual} = F_{IDEAL}/(1 + (R_{INV}/R_{FB})\ (1 + R_{FB}/R_{FF})) \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input voltage and current sources that influence DC operation. The output offset is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N\,(1 + R_{FB}/R_G) \pm V_{IO}\ (1 + R_{FB}/R_G) \pm Ib_I \times R_{FB} \quad (4)$$

If all terms are divided by the gain ($1 + R_F/R_G$) it can be observed that input referred offsets improve as gain increases.

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of equation 4 and applying the spectral noise values found in the Typical Performance Curve graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed-loop gain increases (by keeping R_F fixed and reducing R_I with $R_N = 0\Omega$).

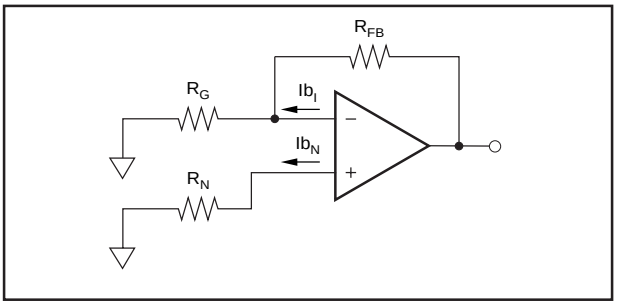


FIGURE 2. Output Offset Voltage Equivalent Circuit.

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB} (refer to Figure 1). This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF}. As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth. To maintain specified bandwidth, the following equations can be used to approximate R_F and R_I for any gain from ±1 to ±15:

R_{FB} = 424 ±8G (+ for inverting and – for non-inverting)

R_{FF} = (424 – 8G)/(G – 1) (non-inverting)

R_I = (424 + 8G)/G (inverting)

G = Closed-loop gain

WIRING PRECAUTIONS

Maximizing the OPA644's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA644, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply inductance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface-mount capacitors is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the demonstration board figure in the DEM-OPA64X data sheet for the recommended layout and component placements.

(2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the backside of the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the data sheet.

5) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA644U (SO-8 package) will offer the best AC performance.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA644's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA644 incorporates on-chip ESD protection diodes as shown in Figure 3. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

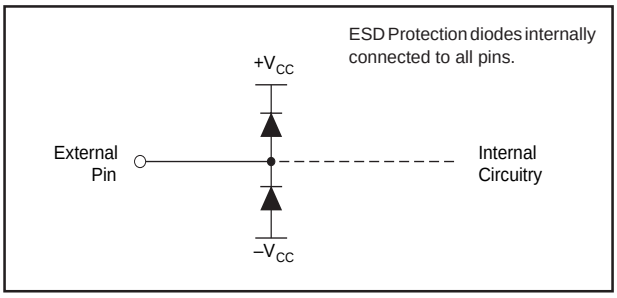


FIGURE 3. Internal ESD Protection.

All pins on the OPA644 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA644 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the machine model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA644.

OUTPUT DRIVE CAPABILITY

The OPA644 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA644 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA644 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

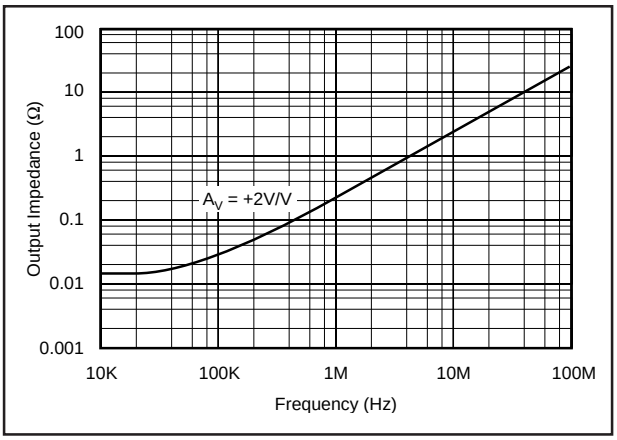


FIGURE 4. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA644 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 26mA = 260mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max $= (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA644's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

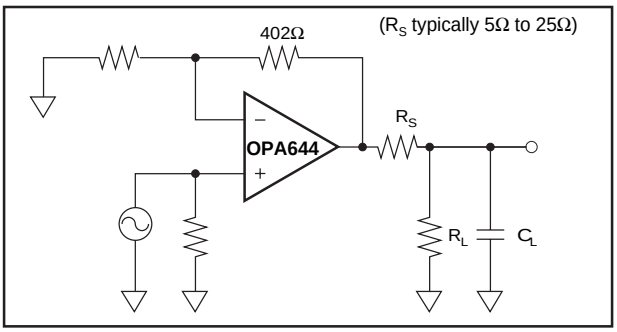


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA644 is internally compensated and is stable in unity gain with a phase margin of approximately 70°. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA644 in a good layout is very flat with frequency.

DISTORTION

The OPA644's harmonic distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

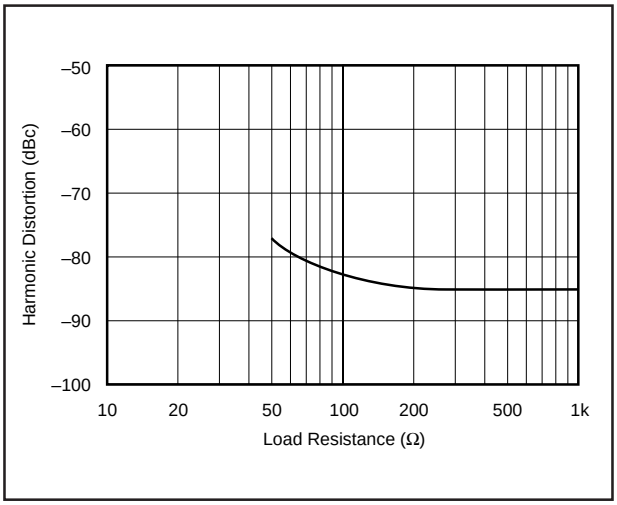


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA644 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 7 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA644 is 0.008% differential gain and 0.009° differential phase to both NTSC and PAL standards.

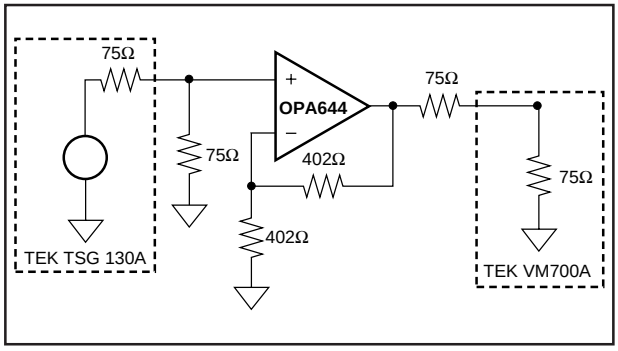


FIGURE 7. Configuration for Testing Differential Gain/Phase.

NOISE FIGURE

The OPA644's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA644's Noise Figure vs Source Resistance is shown in Figure 8.

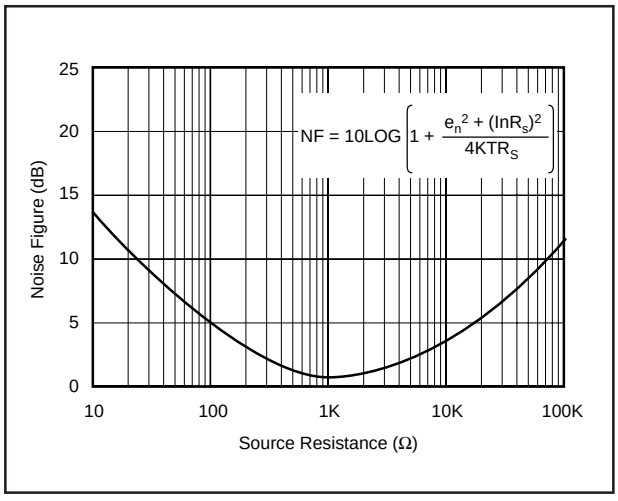


FIGURE 8. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA644. Contract Burr-Brown applications departments to receive a SPICE Diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X data sheet for details.

APPLICATIONS

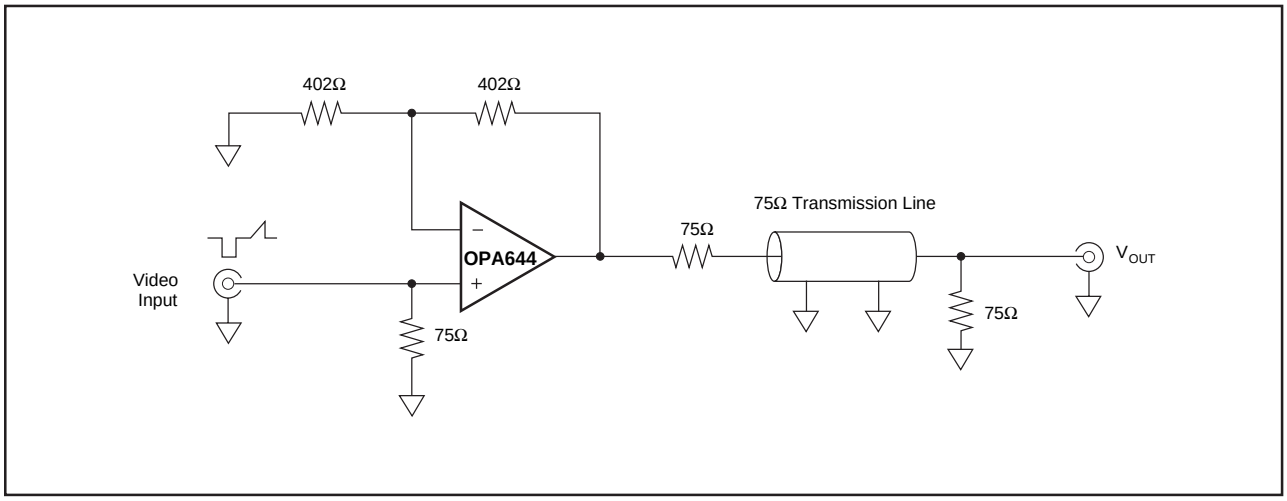


FIGURE 9. Low Distortion Video Amplifier.

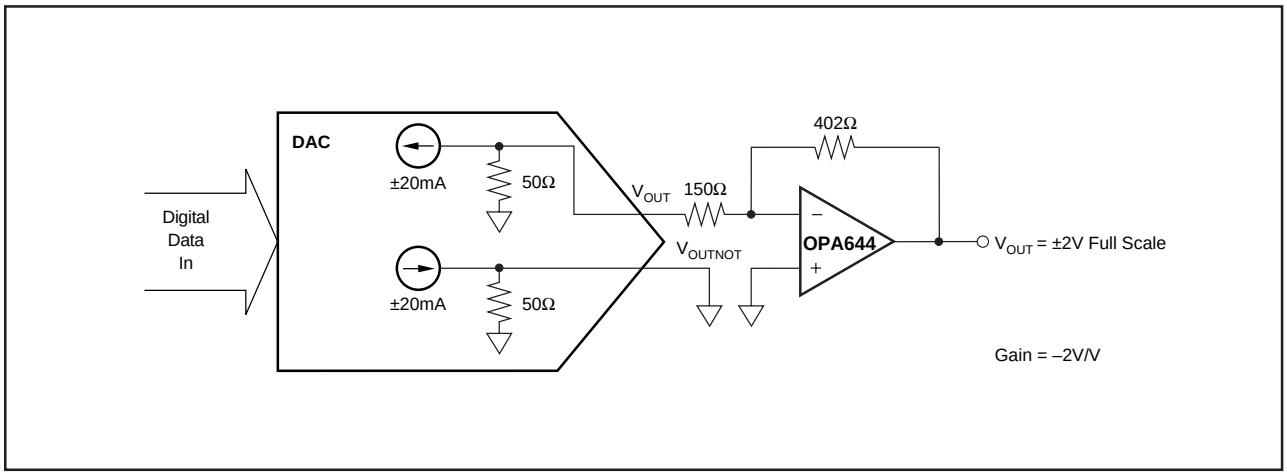


FIGURE 10. Output Amplification for a DDS DAC.

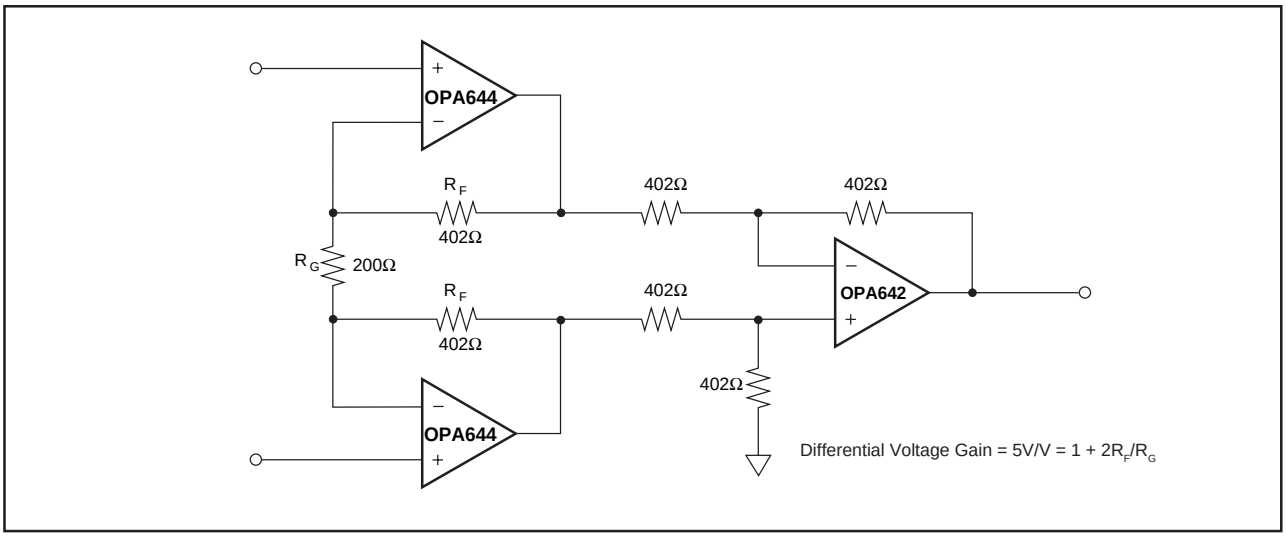


FIGURE 11. Wideband, Fast-Settling Instrumentation Amplifier.

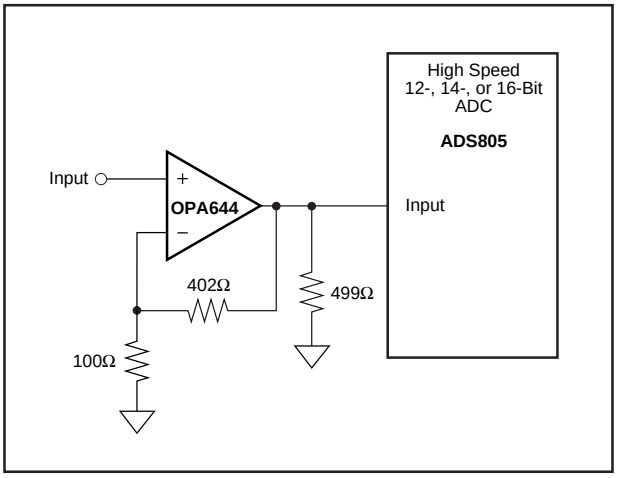


FIGURE 12. Low Distortion ADC Amplifier (G = +5V/V).