Data Sheet May 9, 2005 FN7118.3

10- and 12-Channel TFT-LCD Reference Voltage Generators

The EL5226 and EL5326 are designed to produce the reference voltages required in TFT-LCD applications. Each output is programmed to the required voltage with 10 bits of resolution. Reference pins determine the high and low voltages of the output range, which are capable of swinging to either supply rail. Programming of each output is performed using the I^2C serial interface.

A number of the EL5226 and EL5326 can be stacked for applications requiring more than 12 outputs. The reference inputs can be tied to the rails, enabling each part to output the full voltage range, or alternatively, they can be connected to external resistors to split the output range and enable finer resolutions of the outputs.

The EL5226 has 10 outputs and the EL5326 has 12 outputs and both are available in a 28-pin TSSOP package. They are specified for operation over the full -40°C to +85°C temperature range.

Features

- 10- to 12-channel reference outputs
- Accuracy of ±1%
- Supply voltage of 5V to 16.5V
- Digital supply 3.3V to 5V
- Low supply current of 10mA
- Rail-to-rail capability
- Pb-Free available (RoHS compliant)

Applications

- TFT-LCD drive circuits
- Reference voltage generators

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5226IR	28-Pin TSSOP	-	MDP0044
EL5226IR-T7	28-Pin TSSOP	7”	MDP0044
EL5226IR-T13	28-Pin TSSOP	13”	MDP0044
EL5226IRZ (See Note)	28-Pin TSSOP (Pb-free)	-	MDP0044
EL5226IRZ-T7 (See Note)	28-Pin TSSOP (Pb-free)	7”	MDP0044
EL5226IRZ-T13 (See Note)	28-Pin TSSOP (Pb-free)	13”	MDP0044
EL5326IR	28-Pin TSSOP	-	MDP0044
EL5326IR-T7	28-Pin TSSOP	7”	MDP0044
EL5326IR-T13	28-Pin TSSOP	13”	MDP0044
EL5326IRZ (See Note)	28-Pin TSSOP (Pb-free)	-	MDP0044
EL5326IRZ-T7 (See Note)	28-Pin TSSOP (Pb-free)	7”	MDP0044
EL5326IRZ-T13 (See Note)	28-Pin TSSOP (Pb-free)	13”	MDP0044

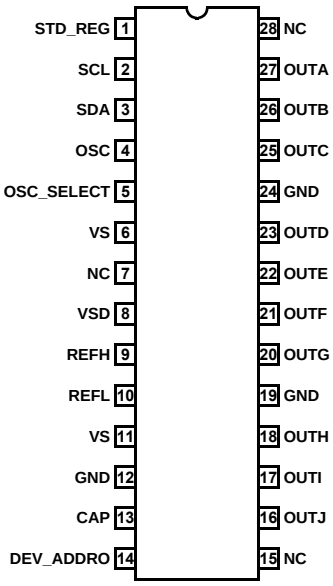
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-352-6832 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 2003, 2004, 2005. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

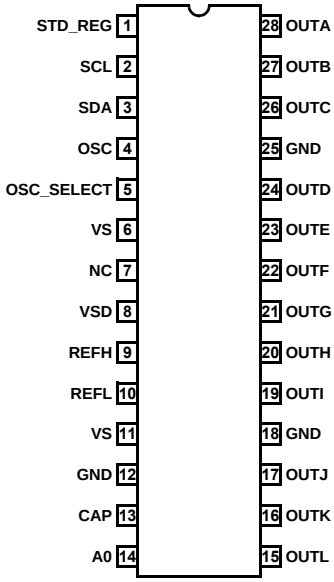
Downloaded from Elcodis.com electronic components distributor

Pinouts

EL5226
(28-PIN TSSOP)
TOP VIEW



EL5326
(28-PIN TSSOP)
TOP VIEW



Downloaded from Elcodis.com electronic components distributor

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND . . . . . +18V
Supply Voltage between V_{SD} and GND . . . . . V_S and +7V (max)
Maximum Continuous Output Current 30mA
Power Dissipation . . . . . See Curves
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 15V, V_{SD} = 5V, V_{REFH} = 13V, V_{REFL} = 2V, R_L = 1.5kΩ and C_L = 200pF to 0V, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_S	Supply Current	EL5226		9	11	mA
		EL5326		10	12	mA
I_{SD}	Digital Supply Current			0.9	3.2	mA
ANALOG						
V_{OL}	Output Swing Low	Sinking 5mA (V_{REFH} = 15V, V_{REFL} = 0)		50	150	mV
V_{OH}	Output Swing High	Sourcing 5mA (V_{REFH} = 15V, V_{REFL} = 0)	14.85	14.95		V
I_{SC}	Short Circuit Current	R_L = 10Ω	150	240		mA
PSRR	Power Supply Rejection Ratio	V_S+ is moved from 14V to 16V	45	65		dB
t_D	Program to Out Delay			4		ms
V_{AC}	Accuracy			20		mV
V_{DROOP}	Droop Voltage			1	2	mV/ms
R_{INH}	Input Resistance @ V_{REFH}, V_{REFL}			34		kΩ
REG	Load Regulation	I_{OUT} = 5mA step		0.5	1.5	mV/mA
DIGITAL						
V_{IH}	Logic 1 Input Voltage		V_{SD}- 20%			V
V_{IL}	Logic 0 Input Voltage				20%* V_{SD}	V
F_{CLK}	Clock Frequency				400	kHz

Downloaded from Elcodis.com electronic components distributor

Pin Descriptions

EL5226	EL5326	PIN NAME	PIN TYPE	PIN FUNTION
1	1	STD_REG	Logic Input	Selects mode, high = standard, low = register mode
2	2	SCL	Logic Input	I^2C clock
3	3	SDA	Logic Input	I^2C data
4	4	OSC	Input/Output	Oscillator pin for synchronizing multiple chips
5	5	OSC_SELECT	Logic Input	Selects internal / external OSC source, high = external, low = internal
6, 11	6, 11	VS	Analog Power	Power supply for analog circuit
7, 15, 28	7	NC		not connected
8	8	VSD	Digital Power	Power supply for digital circuit
9	9	REFH	Analog Reference Input	High reference voltage
10	10	REFL	Analog Reference Input	Low reference voltage
12, 19, 24	12, 18, 25	GND	Ground	Ground
13	13	CAP	Analog Bypass Pin	Decoupling capacitor for internal reference generator
14	14	DEV_ADDR0	Logic Input	I^2C device address input, bit 0
16	17	OUTJ	Analog Output	Channel J programmable output
17	19	OUTI	Analog Output	Channel I programmable output
18	20	OUTH	Analog Output	Channel H programmable output
20	21	OUTG	Analog Output	Channel G programmable output
21	22	OUTF	Analog Output	Channel F programmable output
22	23	OUTE	Analog Output	Channel E programmable output
23	24	OUTD	Analog Output	Channel D programmable output
25	26	OUTC	Analog Output	Channel C programmable output
26	27	OUTB	Analog Output	Channel B programmable output
27	28	OUTA	Analog Output	Channel A programmable output
	15	OUTL	Analog Output	Channel L programmable output
	16	OUTK	Analog Output	Channel K programmable output

Downloaded from Elcodis.com electronic components distributor

Typical Performance Curves

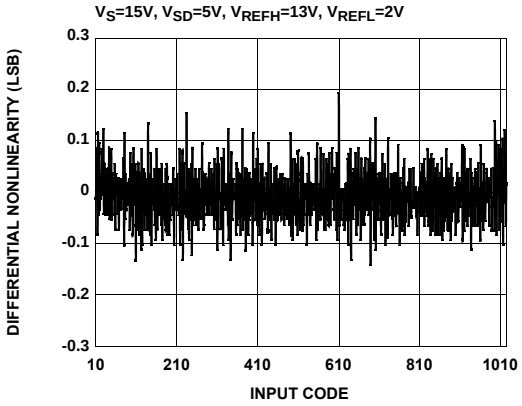


FIGURE 1. DIFFERENTIAL NONLINEARITY vs CODE

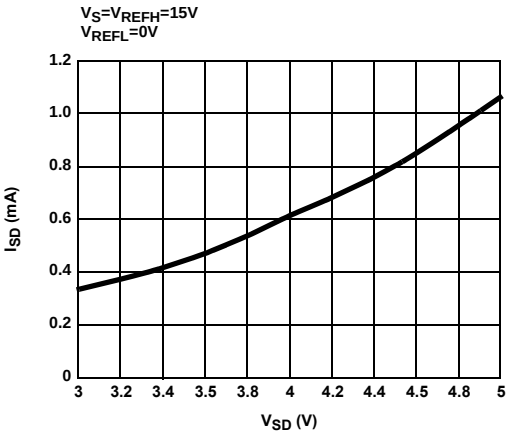


FIGURE 2. DIGITAL SUPPLY VOLTAGE vs DIGITAL SUPPLY CURRENT

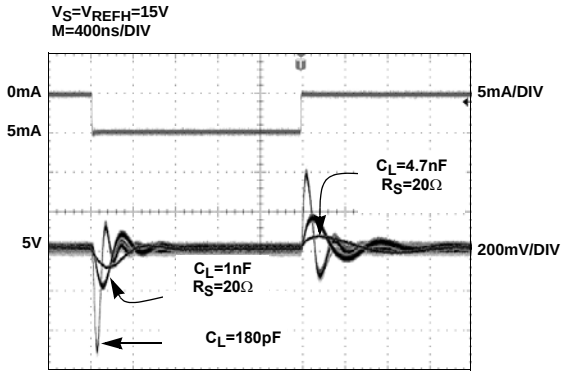


FIGURE 3. TRANSIENT LOAD REGULATION (SOURCING)

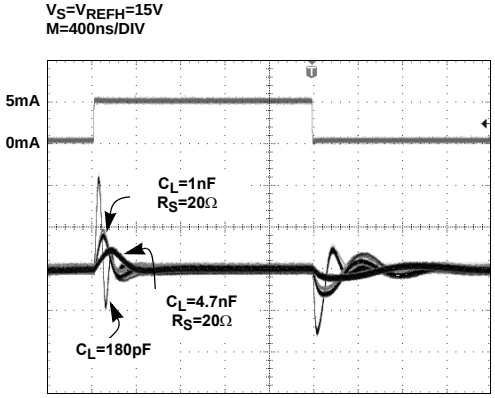


FIGURE 4. TRANSIENT LOAD REGULATION (SINKING)

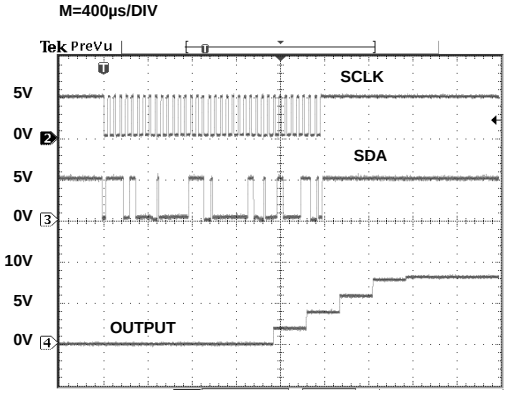


FIGURE 5. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

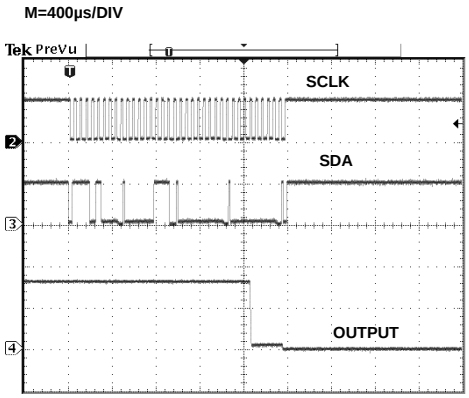


FIGURE 6. LARGE SIGNAL RESPONSE (FALLING FROM 8V TO 0V)

Downloaded from Elcodis.com electronic components distributor

Typical Performance Curves (Continued)

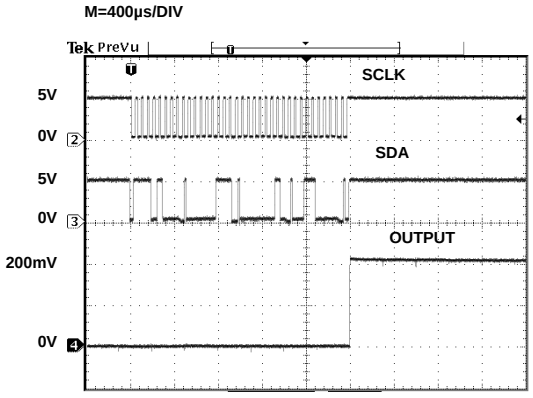


FIGURE 7. SMALL SIGNAL RESPONSE (RISING FROM 0V TO 200mV)

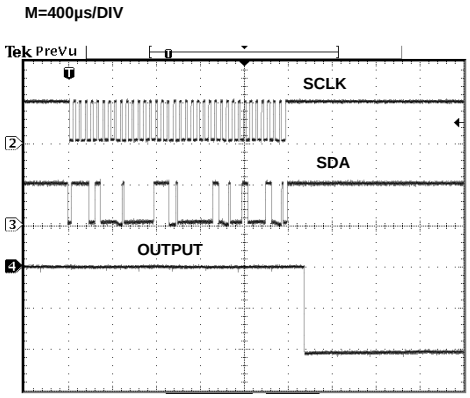


FIGURE 8. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 0V)

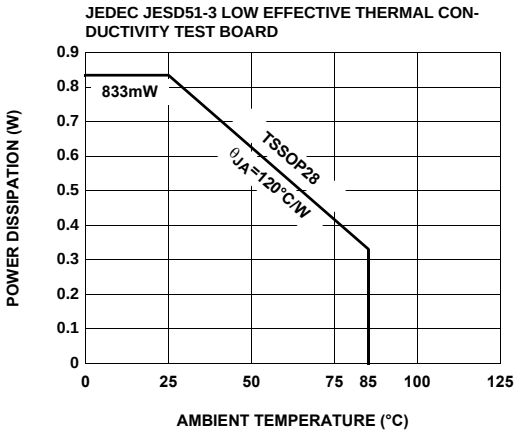


FIGURE 9. POWER DISSIPATION vs AMBIENT TEMPERATURE

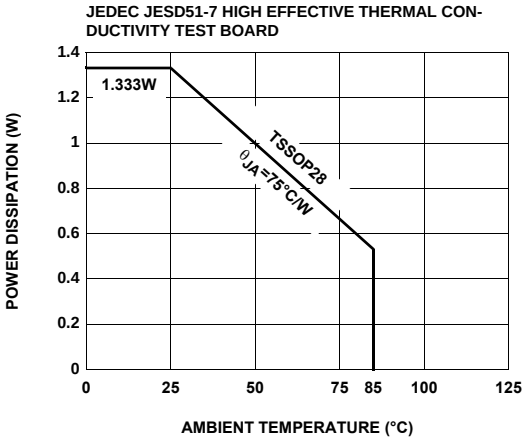


FIGURE 10. POWER DISSIPATION vs AMBIENT TEMPERATURE

Downloaded from Elcodis.com electronic components distributor

General Description

The EL5226 and EL5326 provide a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels. The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear; however, if the panel is to be used in more than one application, the final curve may differ for different applications. By using the EL5226 and EL5326, the V/T curve can be changed to optimize its characteristics according to the required application of the display product. Each of the eight reference voltage outputs can be set with a 10-bit resolution. These outputs can be driven to within 50mV of the power rails of the EL5226 and EL5326. As all of the output buffers are identical, it is also possible to use the EL5226 and EL5326 for applications other than LCDs where multiple voltage references are required that can be set to 10 bit accuracy.

Digital Interface

The EL5226 and EL5326 use a simple two-wire I^2C digital interface to program the outputs. The bus line SCLK is the clock signal line and bus SDA is the data information signal line. The EL5226 and EL5326 can support the clock rate up to 400kHz. External pull up resistor is required for each bus line. The typical value for these two pull up resistor is about 1kΩ.

START AND STOP CONDITION

The Start condition is a high to low transition on the SDA line while SCLK is high. The Stop condition is a low to high transition on the SDA line while SCLK is high. The start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition and to be free again a certain time after the stop condition. The two bus lines must be high when the buses are not in use. The I^2C Timing Diagram 2 shows the format.

DATA VALIDITY

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCLK line is low.

BYTE FORMAT AND ACKNOWLEDGE

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

The master puts a resistive high level on the SDA line during the acknowledge clock pulse. The peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse.

DEVICES ADDRESS AND W/R BIT

Data transfers follow the format shown in Timing Diagram 1. After the Start condition, a first byte is sent which contains the Device Address and write/read bit. This address is a 7-bit long device address and only two device addresses (74H and 75H) are allowed for the EL5226 and EL5326. The first 6 bits (A6 to A1, MSBs) of the device address have been factory programmed and are always 111010. Only the least significant bit A0 is allowed to change the logic state, which can be tied to V_{SD} or DGND. A maximum of two EL5226 and EL5326 may be used on the same bus at one time. The EL5226 and EL5326 monitor the bus continuously and waiting for the start condition followed by the device address. When a device recognizes its device address, it will start to accept data. An eighth bit is followed by the device address, which is a data direction bit (W/R). A "0" indicates a Write transmission and a "1" indicates a Read transmission.

The EL5226 and EL5326 can be operated as Standard mode and Register mode. See the I^2C Timing Diagram 1 for detail formats.

STANDARD MODE

The part operates at Standard Mode if pin 1 (STD/REG) is held high. The Standard Mode allows the user to program all outputs at one time. Two data bytes are required for 10-bit data for each channel output and there are a total of 20/24 data bytes for 10/12 channels. Data in data byte 1 and 2 is for channel A. Data in data byte 15 and 16 is for channel H. D9 to D0 are the 10-bit data for each channel. The unused bits in the data byte are "don't care" and can be set to either one or zero. See Table 1 for program sample for one channel setting:

TABLE 1.

DATA										
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CONDITION
0	0	0	0	0	0	0	0	0	0	Data value = 0
1	0	0	0	0	0	0	0	0	0	Data value = 512
0	0	0	0	0	1	1	1	1	1	Data value = 31
1	1	1	1	1	1	1	1	1	1	Data value = 1023

When the W/R bit is high, the master can read the data from the EL5226 and EL5326. See Timing Diagram 1 for detail formats.

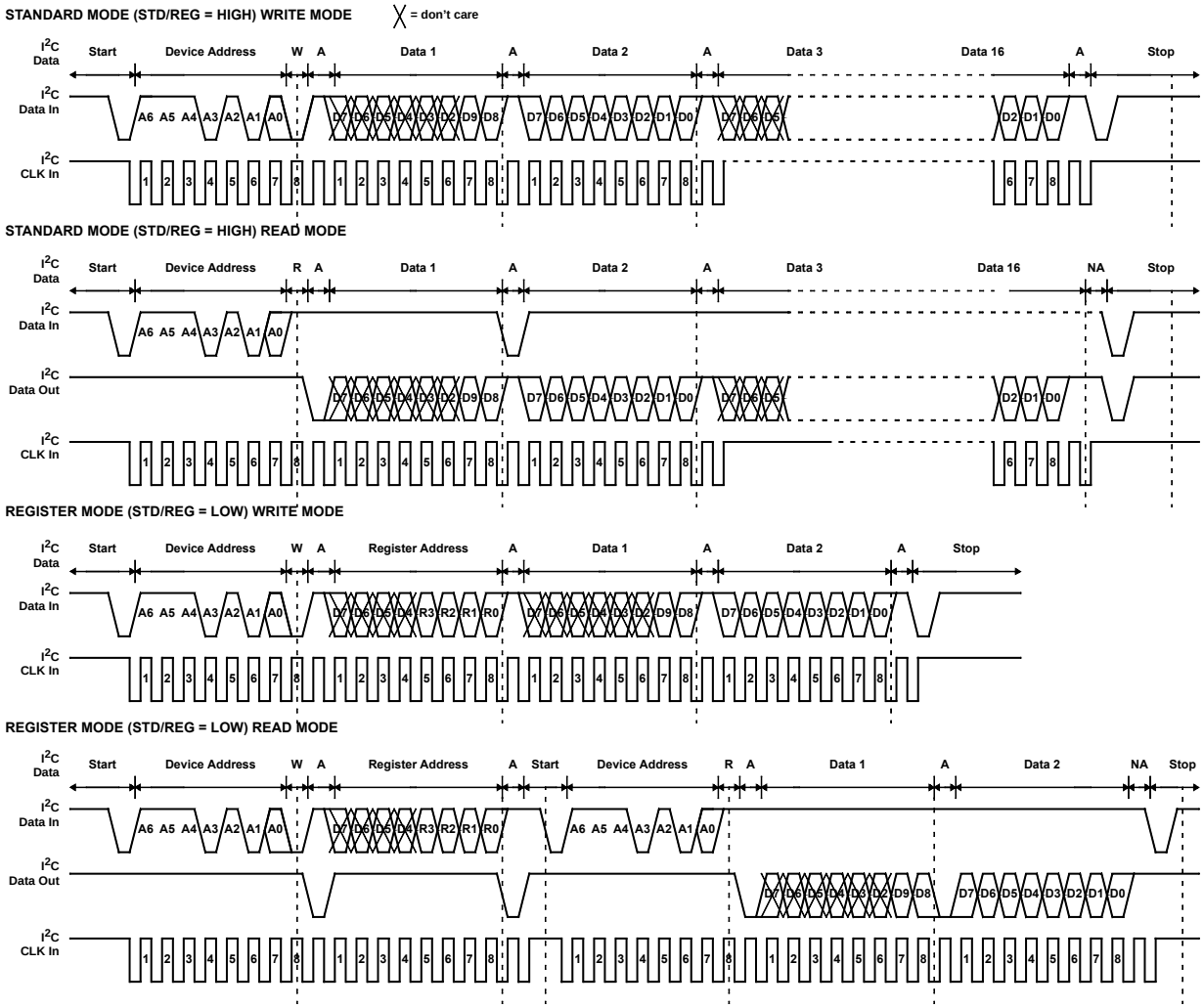
REGISTER MODE

The part operates at Register Mode if pin 1 (STD/REG) is held low. The Register Mode allows the user to program each output individually. Followed by the first byte, the second byte sets the register address for the programmed output channel. Bits R0 to R3 set the output channel address. For the unused bits in the R4 to R7 are "don't care". See Table 2 for program sample.

The EL5226 and EL5326 also allows the user to read the data at Register Mode. See Timing Diagram 1 for detail formats.

Downloaded from Elcodis.com electronic components distributor

I²C Timing Diagram 1



Downloaded from Elcodis.com electronic components distributor

REGISTER ADDRESS				DATA										
R3	R2	R1	R0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CONDITION
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Channel A, Value = 0
0	0	0	1	1	0	0	0	0	0	0	0	0	0	Channel B, Value = 512
0	0	1	0	0	0	0	0	0	1	1	1	1	1	Channel C, Value = 31
0	1	1	1	1	1	1	1	1	1	1	1	1	1	Channel H, Value = 1023

I^2C Timing Diagram 2

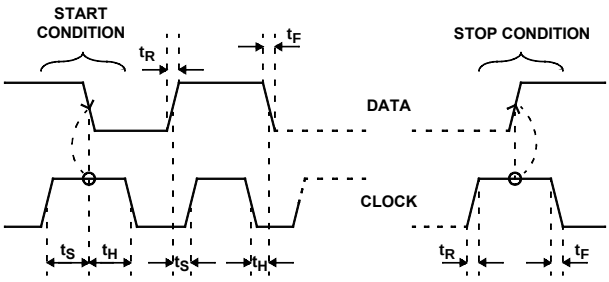


FIGURE 11. START, STOP & TIMING DETAILS OF I^2C INTERFACE

Analog Section

TRANSFER FUNCTION

The transfer function is:

$$V_{OUT(IDEAL)} = V_{REFL} + \frac{data}{1024} \times (V_{REFH} - V_{REFL})$$

where data is the decimal value of the 10-bit data binary input code.

The output voltages from the EL5226 and EL5326 will be derived from the reference voltages present at the V_{REFL} and V_{REFH} pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5226 and EL5326. GND < $V_{REFH} \leq V_S$ and GND ≤ $V_{REFL} \leq V_{REFH}$.

In some LCD applications that require more than 12 channels, the system can be designed such that one EL5226 or EL5326 will provide the Gamma correction voltages that are more positive than the V_{COM} potential. The second EL5226 or EL5326 can provide the Gamma correction voltage more negative than the V_{COM} potential. The Application Drawing shows a system connected in this way.

CLOCK OSCILLATOR

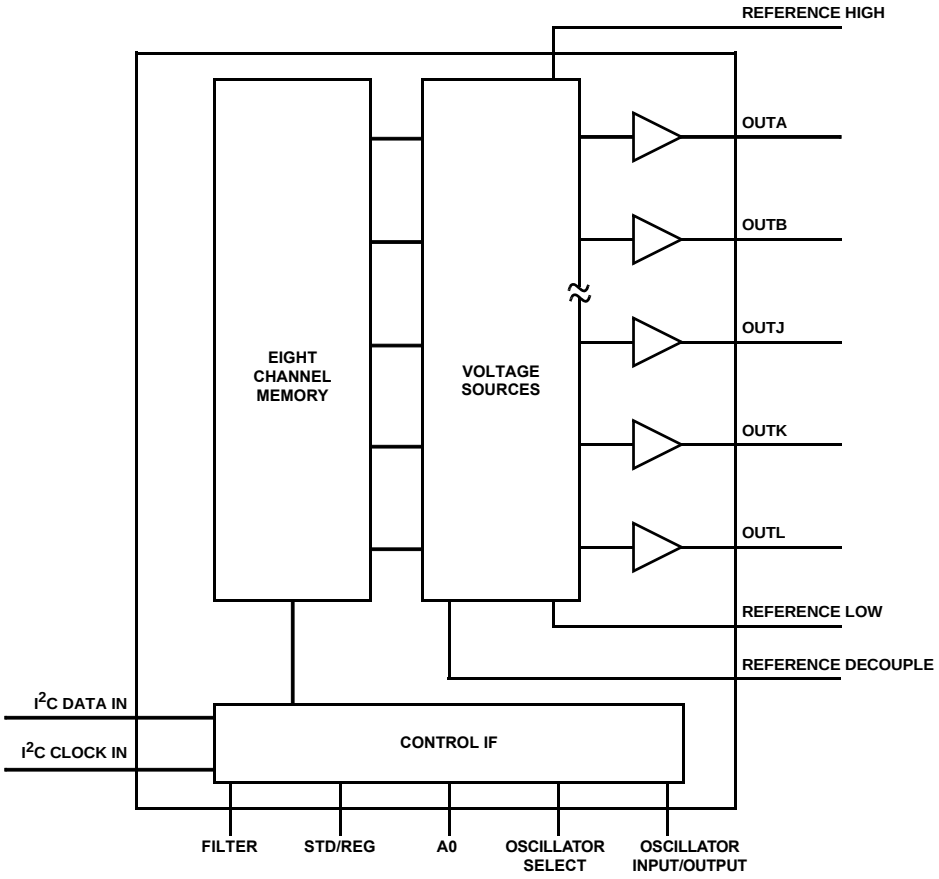
The EL5226 and EL5326 require an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labeled OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the OSC pin. In a 2 chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock Mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the OSC pin will be in a high impedance condition to prevent contention. By setting pin 32 to high, the chip is on external clock mode. Setting pin 32 to low, the chip is on internal clock mode.

Downloaded from Elcodis.com electronic components distributor

Block Diagram



CHANNEL OUTPUTS

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 50mV of the power rails, (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 48µs. In the worst-case scenario this will be 480µs for EL5226 and 576µs for EL5236, when the data has just missed the cycle.

When a large change in output voltage is required, the change will occur in 2V steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16V can take between 4.8ms and 5.3ms for EL5226 and between 6.9ms to 7.48ms for EL5236 depending on the absolute timing relative to the update cycle.

POWER DISSIPATION

With the 30mA maximum continues output drive capability for each channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

Downloaded from Elcodis.com electronic components distributor

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = V_S \times I_S + \Sigma[(V_S - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma(V_{OUT}i \times I_{LOAD}i)$$

when sinking.

Where:

- i = 1 to total 12
- V_S = Supply voltage
- I_S = Quiescent current
- $V_{OUT}i$ = Output voltage of the i channel
- $I_{LOAD}i$ = Load current of the i channel

By setting the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

POWER SUPPLY BYPASSING AND PRINTED CIRCUIT BOARD LAYOUT

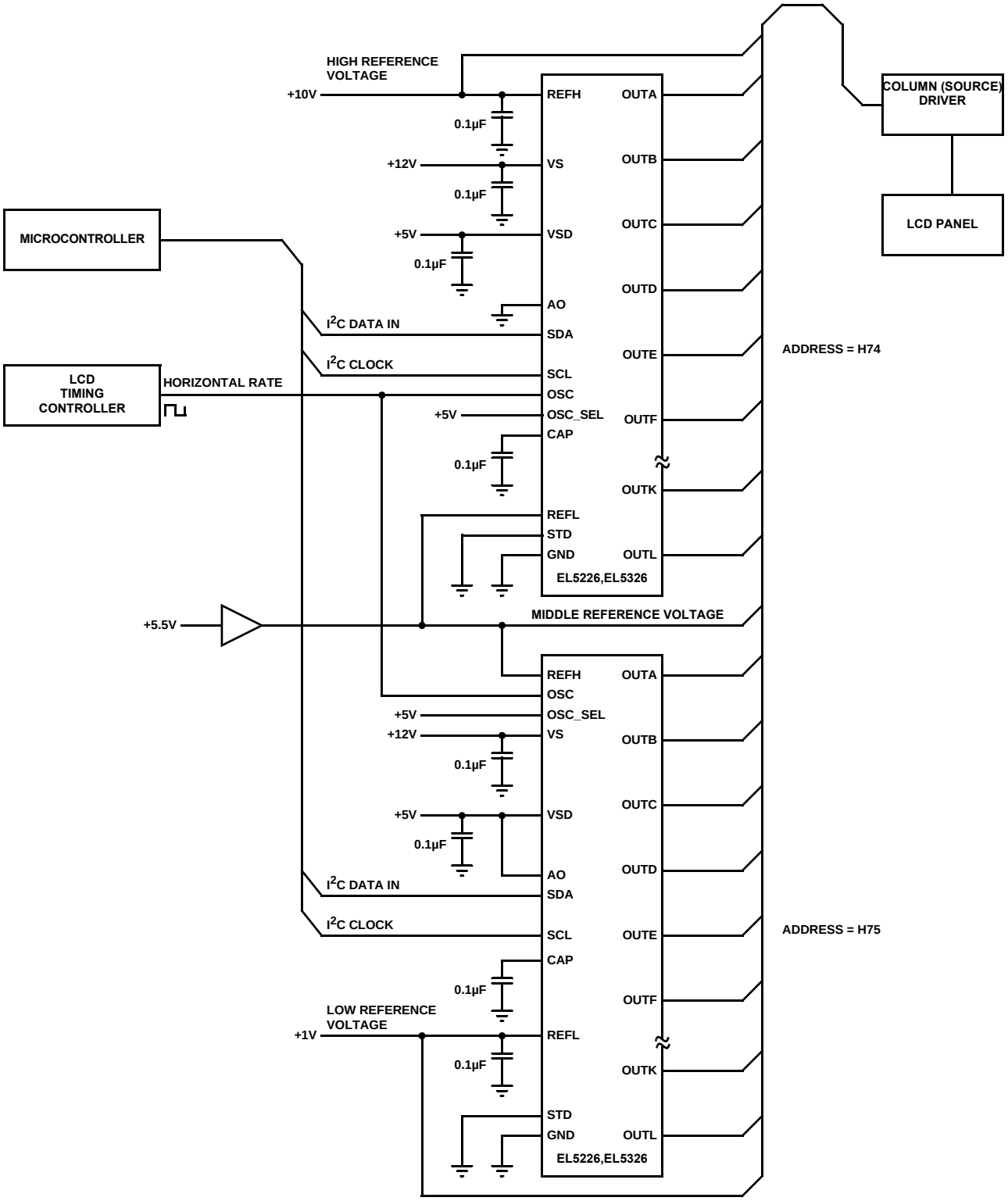
Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5226 and EL5326. The traces from the two ground pins to the ground plane must be very short. The thermal pad of the EL5226 and EL5326 should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1µF ceramic capacitor must be place very close to the V_S, V_{REFH}, V_{REFL}, and CAP pins. A 4.7µF local bypass tantalum capacitor should be placed to the V_S, V_{REFH}, and V_{REFL} pins.

APPLICATION USING THE EL5226 AND EL5326

In the first application drawing, the schematic shows the interconnect of a pair of EL5226 and EL5326 chips connected to give 8 gamma corrected voltages above the V_{COM} voltage, and 8 gamma corrected voltages below the V_{COM} voltage.

Downloaded from Elcodis.com electronic components distributor

Application Drawing



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Downloaded from Elcodis.com electronic components distributor