12MHz Rail-to-Rail Buffers + 100mA V_{COM} Amplifier

The EL5224, EL5324, and EL5424 feature 8, 10, and 12 low power buffers, respectively, and one high power output amplifier. They are designed primarily for buffering column driver reference voltages in TFT-LCD applications as well as generation of the V_{COM} supply. Each low power buffer features a -3dB bandwidth of 12MHz and features rail-to-rail input/output capability. The high power buffer can drive 100mA and swings to within 2V of each rail.

The 8-channel EL5224 is available in 24-pin QFN and 24-pin HTSSOP packages, the 10-channel EL5324 is available in 32-pin QFN and 28-pin HTSSOP packages, and the 12-channel EL5434 is available in the 32-pin QFNQFN package. They are specified for operation over the full -40°C to +85°C temperature range.

Features

- 8, 10, and 12 channel versions
- 12MHz -3dB buffer bandwidth
- 150mA V_{COM} buffer
- Operating supply voltage from 4.5V to 16.5V
- Low supply current - 6mA total (8-channel version)
- Rail-to-rail input/output swing (buffers only)
- QFN package - just 0.9mm high
- Pb-Free available (RoHS compliant)

Applications

- TFT-LCD column driver buffering and V_{COM} supply
- Electronics notebooks
- Computer monitors
- Electronics games
- Touch-screen displays
- Portable instrumentation

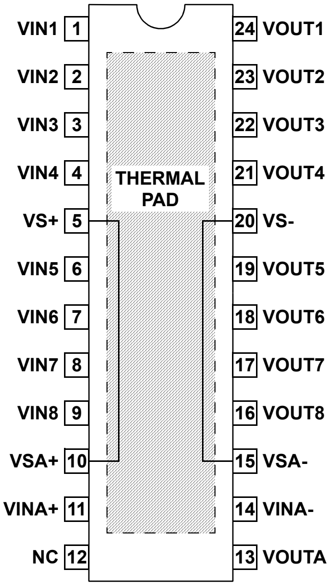
Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5224IL	24-Pin QFN		MDP0046
EL5224IL-T7	24-Pin QFN	7”	MDP0046
EL5224IL-T13	24-Pin QFN	13”	MDP0046
EL5224ILZ (See Note)	24-Pin QFN (Pb-free)		MDP0046
EL5224ILZ-T7 (See Note)	24-Pin QFN (Pb-free)	7”	MDP0046
EL5224ILZ-T13 (See Note)	24-Pin QFN (Pb-free)	13”	MDP0046
EL5224IRE	24-Pin HTSSOP	-	MDP0048
EL5224IRE-T7	24-Pin HTSSOP	7”	MDP0048
EL5224IRE-T13	24-Pin HTSSOP	13”	MDP0048
EL5224IREZ (See Note)	24-Pin HTSSOP (Pb-free)	-	MDP0048
EL5224IREZ-T7 (See Note)	24-Pin HTSSOP (Pb-free)	7”	MDP0048
EL5224IREZ-T13 (See Note)	24-Pin HTSSOP (Pb-free)	13”	MDP0048
EL5324IL	32-Pin QFN		MDP0046
EL5324IL-T7	32-Pin QFN	7”	MDP0046
EL5324IL-T13	32-Pin QFN	13”	MDP0046
EL5324ILZ (See Note)	32-Pin QFN (Pb-free)		MDP0046
EL5324ILZ-T7 (See Note)	32-Pin QFN (Pb-free)	7”	MDP0046
EL5324ILZ-T13 (See Note)	32-Pin QFN (Pb-free)	13”	MDP0046
EL5324IRE	28-Pin HTSSOP	-	MDP0048
EL5324IRE-T7	28-Pin HTSSOP	7”	MDP0048
EL5324IRE-T13	28-Pin HTSSOP	13”	MDP0048
EL5324IREZ (See Note)	28-Pin HTSSOP (Pb-free)	-	MDP0048
EL5324IREZ-T7 (See Note)	28-Pin HTSSOP (Pb-free)	7”	MDP0048
EL5324IREZ-T13 (See Note)	28-Pin HTSSOP (Pb-free)	13”	MDP0048
EL5424IL	32-Pin QFN		MDP0046
EL5424IL-T7	32-Pin QFN	7”	MDP0046
EL5424IL-T13	32-Pin QFN	13”	MDP0046
EL5424ILZ (See Note)	32-Pin QFN (Pb-free)		MDP0046
EL5424ILZ-T7 (See Note)	32-Pin QFN (Pb-free)	7”	MDP0046
EL5424ILZ-T13 (See Note)	32-Pin QFN (Pb-free)	13”	MDP0046

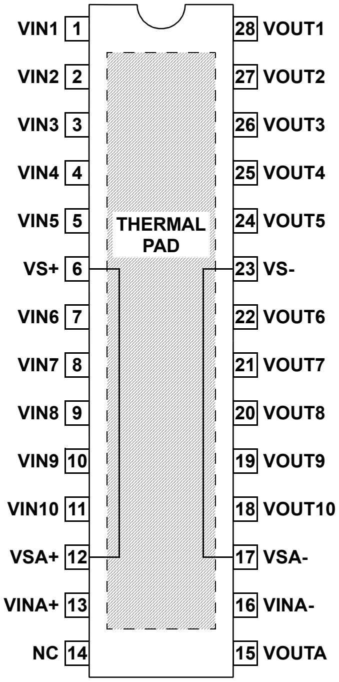
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

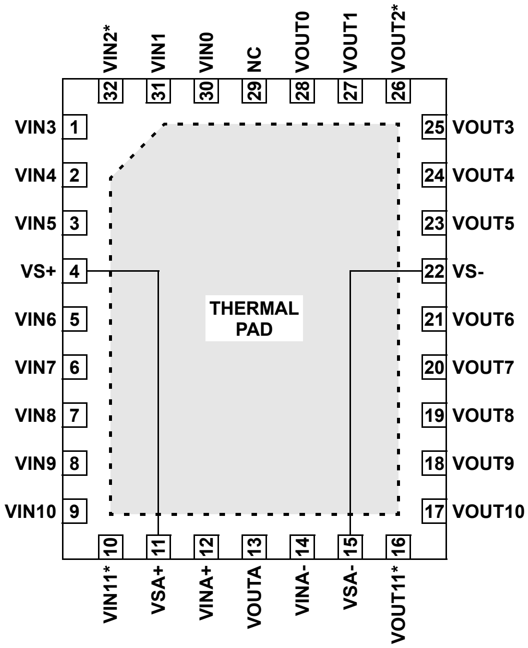
EL5224
(24-PIN HTSSOP)
TOP VIEW



EL5324
(28-PIN HTSSOP)
TOP VIEW

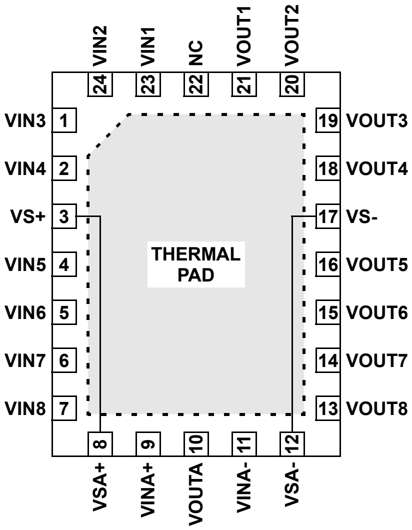


EL5324 & EL5424
(32-PIN QFN)
TOP VIEW



*Not available in EL5324

EL5224
(24-PIN QFN)
TOP VIEW



Absolute Maximum Ratings ($T_A = 25°C$)

Supply Voltage between V_S+ and V_S-	+18V	Power Dissipation	See Curves
Input Voltage	V_S- -0.5V, V_S+ +0.5V	Maximum Die Temperature	+125°C
Maximum Continuous Output Current (V_{OUT0-9})	30mA	Storage Temperature	-65°C to +150°C
Maximum Continuous Output Current (V_{OUTA})	150mA	Ambient Operating Temperature	-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +15V, V_S- = 0, R_L = 10kΩ, $R_F = R_G$ = 20kΩ, C_L = 10pF to 0V, Gain of V_{COM} = -1, and T_A = 25°C Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	14	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	$1V \le V_{OUT} \le 14V$	0.992		1.008	V/V
INPUT CHARACTERISTICS (V_{COM} BUFFER)						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		1	4	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		3		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	100	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
V_{REG}	Load Regulation	V_{COM} = 6V, -100mA < I_L < 100mA	-20		+20	mV
OUTPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OL}	Output Swing Low	I_L = 7.5mA		50	150	mV
V_{OH}	Output Swing High	I_L = 7.5mA	14.85	14.95		V
I_{SC}	Short Circuit Current		120	140		mA
OUTPUT CHARACTERISTICS (V_{COM} BUFFER)						
V_{OL}	Output Swing Low	50Ω to 7.5V		1	1.5	V
V_{OH}	Output Swing High	50Ω to 7.5V	13.5	14		V
I_{SC}	Short Circuit Current			160		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	Reference buffer V_S from 5V to 15V	55	80		dB
		V_{COM} buffer, V_S from 5V to 15V	60	100		dB
I_S	Total Supply Current	EL5224 (no load)	5	6.8	8	mA
		EL5324 (no load)	6	7.8	9.5	mA
		EL5424 (no load)	7	8.8	11	mA
DYNAMIC PERFORMANCE (BUFFER AMPLIFIERS)						
SR	Slew Rate (Note 2)	$-4V \le V_{OUT} \le 4V$, 20% to 80%	7	15		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		250		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz

Electrical Specifications

$V_S+ = +15V$, $V_S- = 0$, $R_L = 10k\Omega$, $R_F = R_G = 20k\Omega$, $C_L = 10pF$ to 0V, Gain of $V_{COM} = -1$, and $T_A = 25°C$ Unless Otherwise Specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GBWP	Gain-Bandwidth Product	$R_L = 10k\Omega$, $C_L = 10pF$		8		MHz
PM	Phase Margin	$R_L = 10k\Omega$, $C_L = 10pF$		50		°
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges

Pin Descriptions

24-PIN HTSSOP	24-PIN QFN	32-PIN QFN	28-PIN HTSSOP	PIN NAME	PIN FUNCTION
1	23	31	1	VIN1	Input
2	24	32 (Note 1)	2	VIN2	Input
3	1	1	3	VIN3	Input
4	2	2	4	VIN4	Input
5	3	4	6	VS+	Power
6	4	3	5	VIN5	Input
7	5	5	7	VIN6	Input
8	6	6	8	VIN7	Input
9	7	7	9	VIN8	Input
10	8	11	12	VSA+	Power
11	9	12	13	VINA+	Positive input of V_{COM}
12	22	29	14	NC	Not connected
13	10	13	15	VOUTA	Output of V_{COM}
14	11	14	16	VINA-	Negative input of V_{COM}
15	12	15	17	VSA-	Power
16	13	19	20	VOUT8	Output
17	14	20	21	VOUT7	Output
18	15	21	22	VOUT6	Output
19	16	23	24	VOUT5	Output
20	17	22	23	VS-	Power
21	18	24	25	VOUT4	Output
22	19	25	26	VOUT3	Output
23	20	26 (Note 1)	27	VOUT2	Output
24	21	27	28	VOUT1	Output
		8	10	VIN9	Input
		9	11	VIN10	Input
		10 (Note 1)		VIN11	Input
		16 (Note 1)		VOUT11	Output
		17	18	VOUT10	Output
		18	19	VOUT9	Output
		28		VOUT0	Output
		30		VIN0	Input

NOTE:

1. Not available in EL5324IL

Typical Performance Curves

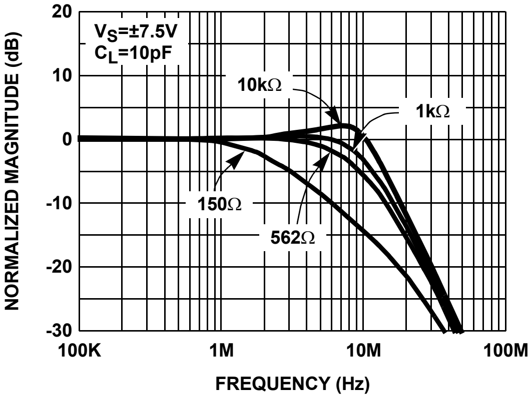


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS R_L (BUFFER)

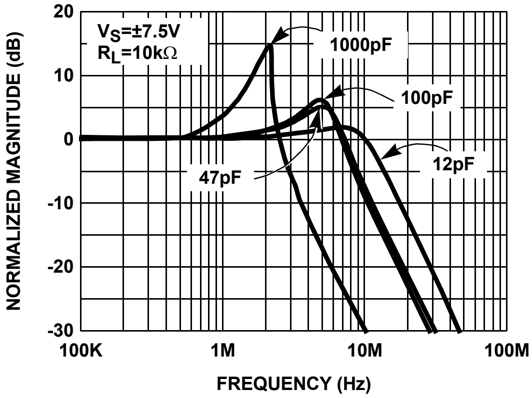


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS C_L (BUFFER)

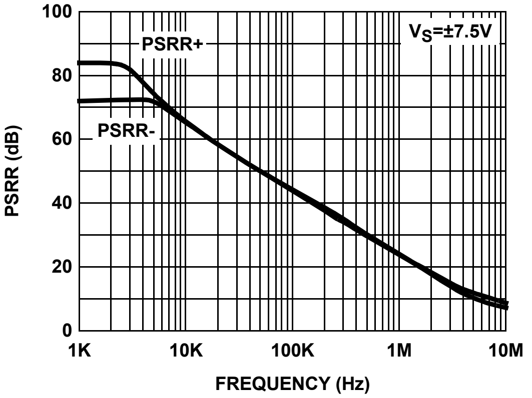


FIGURE 3. PSRR vs FREQUENCY (BUFFER)

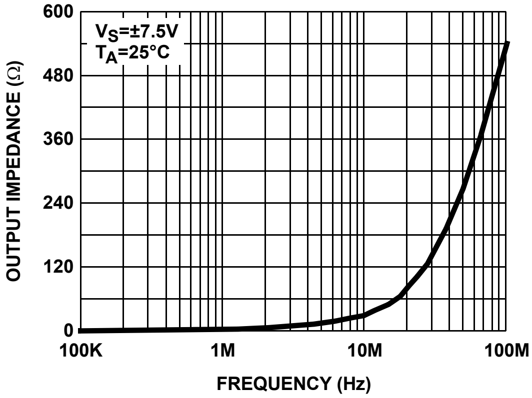


FIGURE 4. OUTPUT IMPEDANCE vs FREQUENCY (BUFFER)

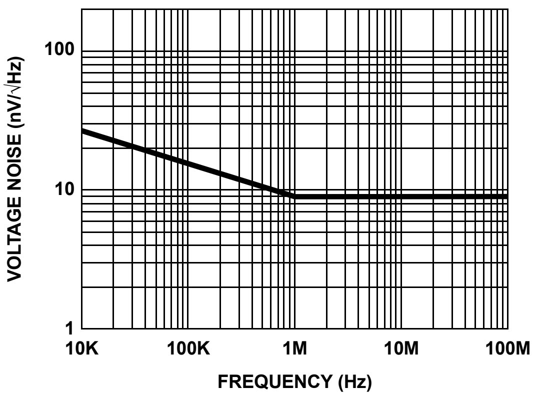


FIGURE 5. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (BUFFER)

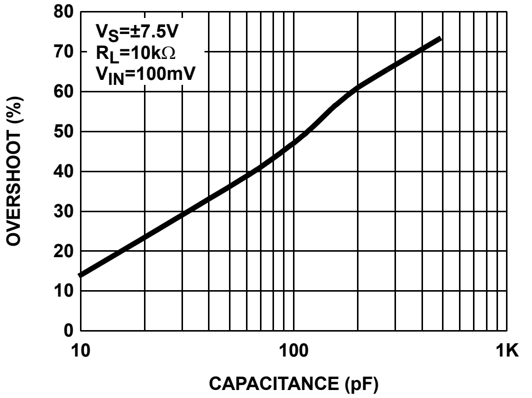


FIGURE 6. OVERSHOOT vs LOAD CAPACITANCE (BUFFER)

Typical Performance Curves (Continued)

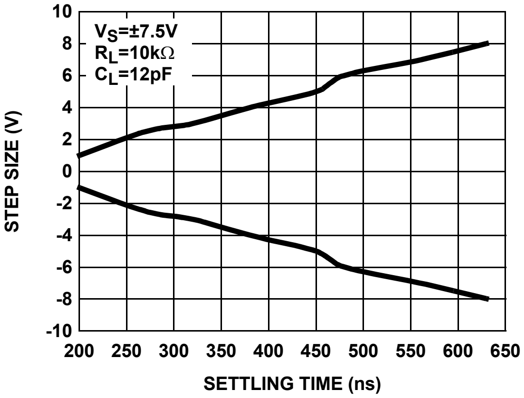


FIGURE 7. SETTLING TIME vs STEP SIZE (BUFFER)

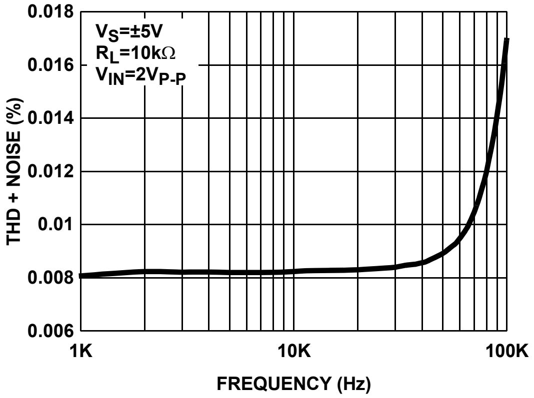


FIGURE 8. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY (BUFFER)

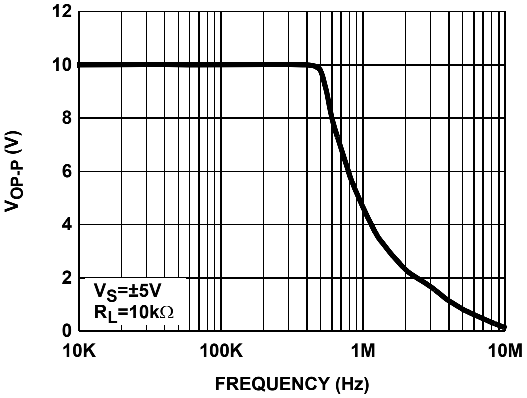


FIGURE 9. OUTPUT SWING vs FREQUENCY (BUFFER)

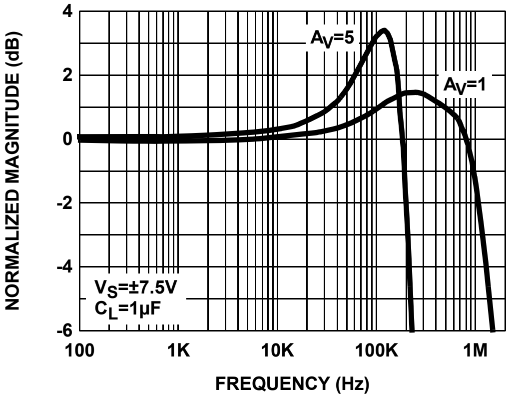


FIGURE 10. FREQUENCY RESPONSE (V_{COM})

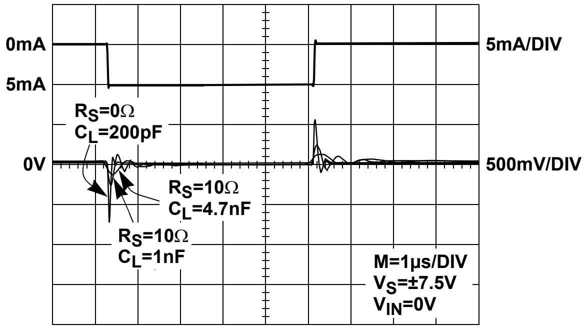


FIGURE 11. TRANSIENT LOAD REGULATION - SOURCING (BUFFER)

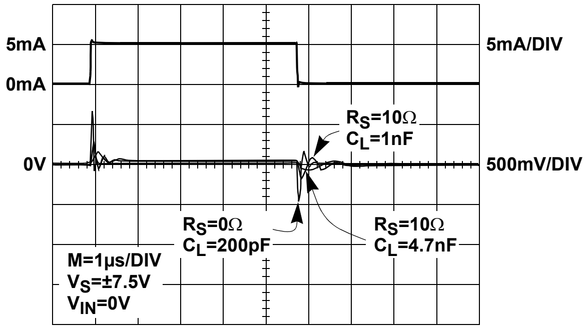


FIGURE 12. TRANSIENT LOAD REGULATION - SINKING (BUFFER)

Typical Performance Curves (Continued)

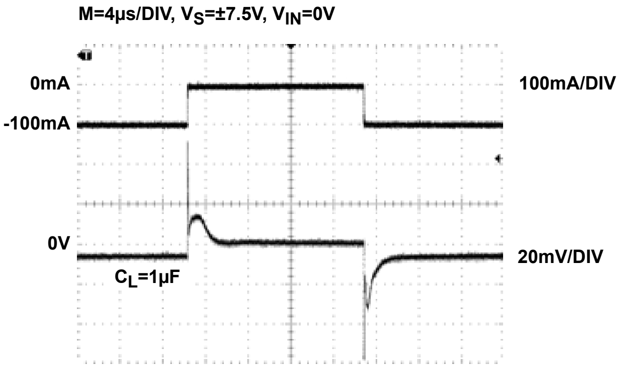


FIGURE 13. TRANSIENT LOAD REGULATION - SOURCING (V_{COM})

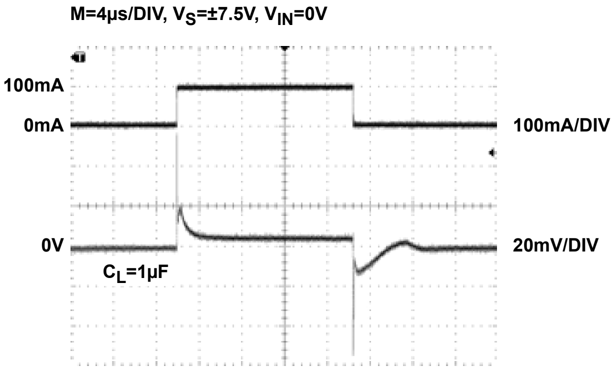


FIGURE 14. TRANSIENT LOAD REGULATION - SINKING (V_{COM})

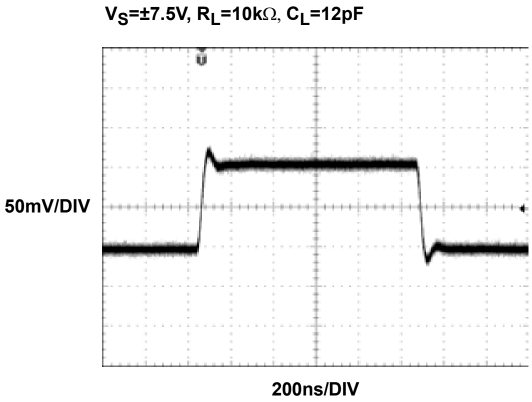


FIGURE 15. SMALL SIGNAL TRANSIENT RESPONSE (BUFFER)

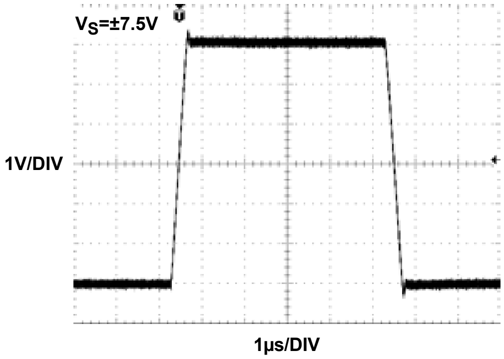


FIGURE 16. LARGE SIGNAL TRANSIENT RESPONSE (BUFFER)

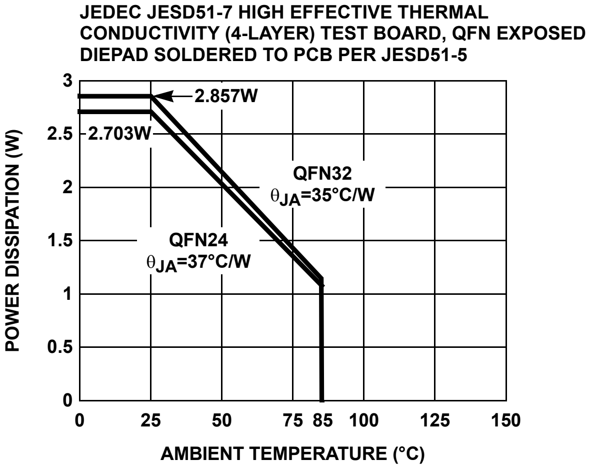


FIGURE 17. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

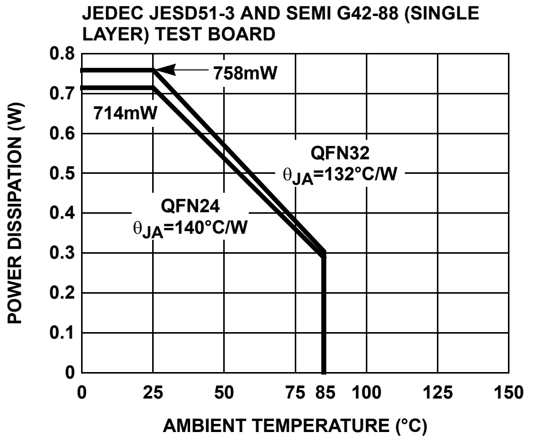


FIGURE 18. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

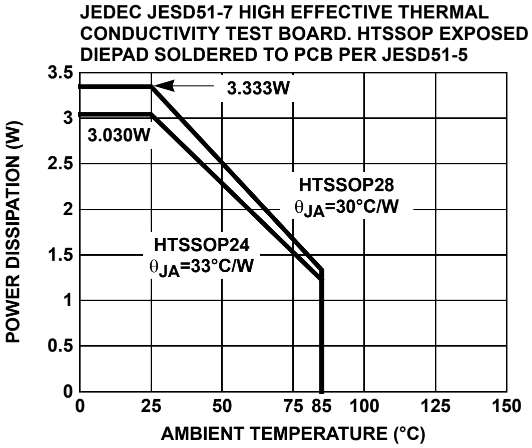


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

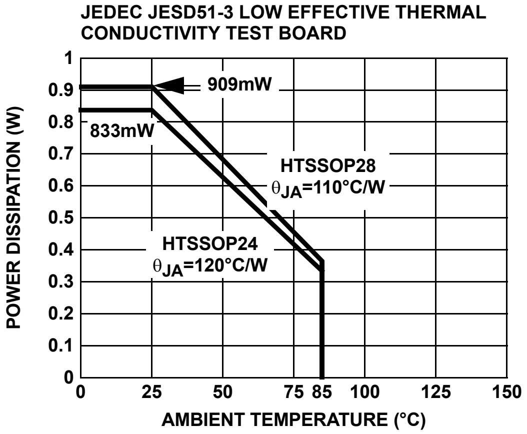


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL5224, EL5324, and EL5424 unity gain buffers and 100mA V_{COM} amplifier are fabricated using a high voltage CMOS process. The buffers exhibit rail-to-rail input and output capability and has low power consumption (600µA per buffer). When driving a load of 10kΩ and 12pF, the buffers have a -3dB bandwidth of 12MHz and exhibits 18V/µs slew rate. The V_{COM} amplifier exhibits rail-to-rail input. The output can be driving to within 2V of each supply rail. With a 1µF capacitance load, the GBWP is about 1MHz.

Correct operation is guaranteed for a supply range of 4.5V to 16.5V.

The Use of the Buffers

The output swings of the buffers typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 21 shows the input and output waveforms for the device. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.985V_{P-P}$.

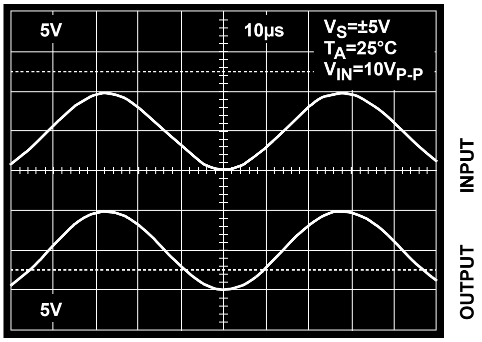


FIGURE 21. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

SHORT-CIRCUIT CURRENT LIMIT

The buffers will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

OUTPUT PHASE REVERSAL

The buffers are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 22 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

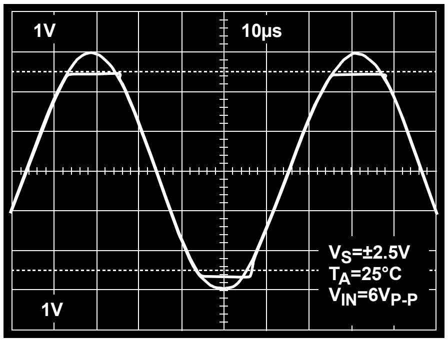


FIGURE 22. OPERATION WITH BEYOND-THE-RAILS INPUT

UNUSED BUFFERS

It is recommended that any unused buffers have their inputs tied to the ground plane.

DRIVING CAPACITIVE LOADS

The buffers can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The buffers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a snubber circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain.

The Use of V_{COM} Amplifier

The V_{COM} amplifier is designed to control the voltage on the back plate of an LCD display. This plate is capacitively coupled to the pixel drive voltage which alternately cycles positive and negative at the line rate for the display. Thus the amplifier must be capable of sourcing and sinking capacitive pulses of current, which can occasionally be quite large (a few 100mA for typical applications).

A simple use of the V_{COM} amplifier is as a voltage follower, as illustrated in Figure 23. Here, a voltage, corresponding to the mid-DAC potential, is generated by a resistive divider and buffered by the amplifier. The amplifier's stability is designed to be dominated by the load capacitance, thus for very short duration pulses (< 1µs) the output capacitor supplies the current. For longer pulses the V_{COM} amplifier supplies the current. By virtue of its high transconductance which progressively increases as more current is drawn, it can maintain regulation within 5mV as currents up to 100mA are drawn, while consuming only 2mA of quiescent current.

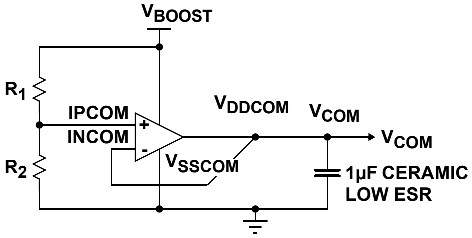


FIGURE 23. V_{COM} USED AS A VOLTAGE BUFFER

Alternatively, the back plate potential can be generated by a DAC and the V_{COM} amplifier used to buffer the DAC voltage, with gain if necessary. This is shown in Figure 24. In this case, the effective transconductance of the feedback is reduced, thus the amplifier will be more stable, but regulation will be degraded by the feedback factor.

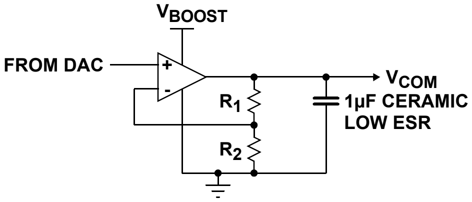


FIGURE 24. V_{COM} USED AS A BUFFER WITH GAIN

CHOICE OF OUTPUT CAPACITOR

A 1µF ceramic capacitor with low ESR is recommended for this amplifier. (For example, GRM42_ 6X7R105K16). This capacitor determines the stability of the amplifier. Reducing it will make the amplifier less stable, and should be avoided. With a 1µF capacitor, the unity gain bandwidth of the amplifier is close to 1MHz when reasonable currents are being drawn. (For lower load currents, the gain and hence bandwidth progressively decreases.) This means the active trans-conductance is:

$$2\pi \times 1\mu F \times 1MHz = 6.28S$$

This high transconductance indicates why it is important to have a low ESR capacitor.

If:

$$ESR \times 6.28 > 1$$

then the capacitor will not force the gain to roll off below unity, and subsequent poles can affect stability. The recommended capacitor has an ESR of 10mΩ, but to this must be added the resistance of the board trace between the capacitor and the sense connection - therefore this should be kept short, as illustrated in Figure 21, by the diagonal line to the capacitor. Also ground resistance between the capacitor and the base of R_2 must be kept to a minimum. These constraints should be considered when laying out the PCB.

If the capacitor is increased above 1µF, stability is generally improved and short pulses of current will cause a smaller "perturbation" on the V_{COM} voltage. The speed of response of the amplifier is however degraded as its bandwidth is decreased. At capacitor values around 10µF, a subtle interaction with internal DC gain boost circuitry will decrease the phase margin and may give rise to some overshoot in the response. The amplifier will remain stable though.

RESPONSE TO HIGH CURRENT SPIKES

The V_{COM} amplifier's output current is limited to 150mA. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. (In this case the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen on the µs time scale in practical systems and for pulses 2 or 3 times the current limit, the V_{COM} voltage will have settled again before the next line is processed.

Power Dissipation

With the high-output drive capability of the EL5224, EL5324, and EL5424 buffer, it is possible to exceed the 125°C "absolute-maximum junction temperature" under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i \times [V_S \times I_{SMAX} + (V_S+ - V_{OUT}i) \times I_{LOAD}i] + [V_{SA} \times I_{SAA} + (V_{SA}+ - V_{OUTA}) \times I_{LA}]$$

when sourcing, and:

$$P_{DMAX} = \Sigma i \times [V_S \times I_{SMAX} + (V_{OUT}i - V_S-) \times I_{LOAD}i] + [V_{SA} \times I_{SAA} + (V_{SA}+ - V_{OUTA}) \times I_{LA}]$$

when sinking.

where:

- i = 1 to total number of buffers
- V_S = Total supply voltage of buffer
- V_{SA} = Total supply voltage of V_{COM}
- I_{SMAX} = Maximum quiescent current per channel
- I_{SA} = Maximum quiescent current of V_{COM}
- $V_{OUT}i$ = Maximum output voltage of the application
- V_{OUTA} = Maximum output voltage of V_{COM}
- $I_{LOAD}i$ = Load current of buffer
- I_{LA} = Load current of V_{COM}

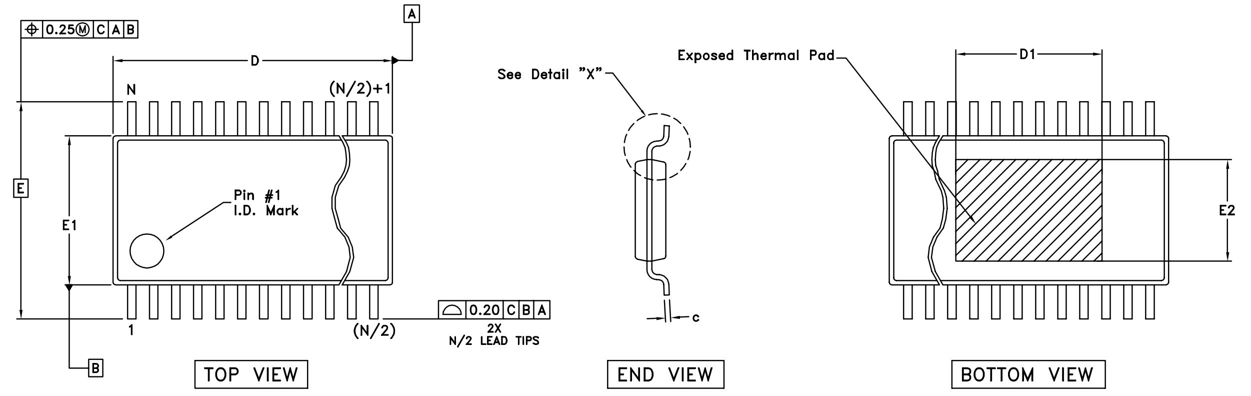
If we set the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

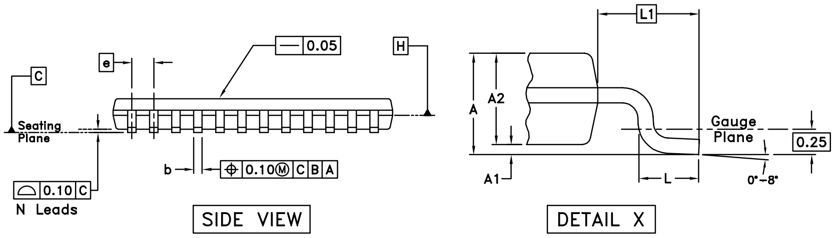
Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- and V_{SA}- pins are connected to ground, two 0.1µF ceramic capacitors should be placed from V_S+ and V_{SA}+ pins to ground. A 4.7µF tantalum capacitor should then be connected from V_S+ and V_{SA}+ pins to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. Internally, V_S+ and V_{SA}+ are shorted together and V_S- and V_{SA}- are shorted together. To avoid high current density, the V_S+ pin and V_{SA}+ pin must be shorted in the PCB layout. Also, the V_S- pin and V_{SA}- pin must be shorted in the PCB layout.

Important Note: The metal plane used for heat sinking of the device is electrically connected to the negative supply potential (V_S- and V_{SA}-). If V_S- and V_{SA}- are tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad must be isolated from any other power planes.

Package Outline Drawing (HTSSOP)





DIMENSION TABLE						
Symbol	14L	20L	24L	28L	38L	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.075	0.075	0.075	0.075	0.075	+/- 0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
D	5.00	6.50	7.80	9.70	9.70	+/- 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/- 0.10
L	0.60	0.60	0.60	0.60	0.60	+/- 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
e	0.65	0.65	0.65	0.65	0.50	Basic
D1	3.2	4.2	4.3	5.0	7.25	Reference
E2	3.0	3.0	3.0	3.0	3.0	Reference
N	14	20	24	28	38	Reference

Notes:

(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.

(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.

(3) Dimensions "D" and "E1" are measured at datum plane H.

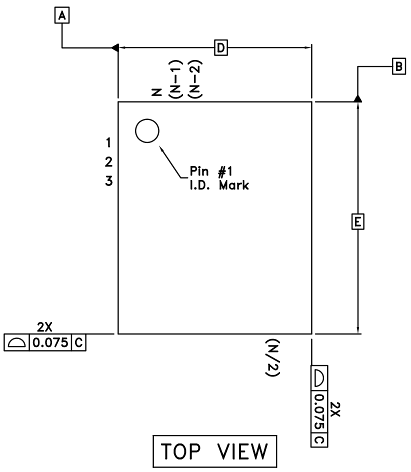
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

Drawing #: MDP0048
Rev: 2
Date: 12/4/03
Units: mm
JEDEC Reg: MO-153

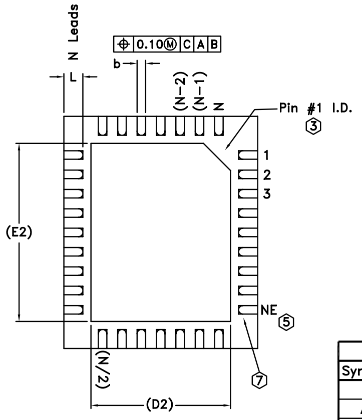
PACKAGE OUTLINE DRAWING
HTSSOP (Heat-Sink TSSOP) Family

SOLUTIONS IN SILICON

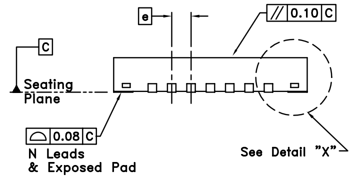
Package Outline Drawing (QFN)



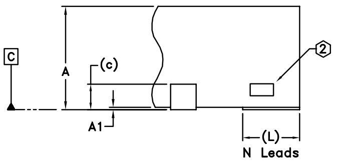
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/−0.02
D	7.00	5.00	8.00	5.00	Basic
D2 ⑧	5.10	3.80	5.80	3.60/2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 ⑧	5.10	5.80	5.80	4.60/3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N ④	44	38	32	32	Reference
ND ⑥	11	7	8	7	Reference
NE ⑤	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/−0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 ⑧	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 ⑧	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N ④	28	24	20	20	16	Reference
ND ⑥	6	5	5	5	4	Reference
NE ⑤	8	7	5	5	4	Reference

Notes:

1 Dimensioning and tolerancing per ASME Y14.5M−1994.

② Tiebar view shown is a non−functional feature.

③ Bottom−side pin #1 I.D. is a diepad chamfer as shown.

④ N is the total number of terminals on the device.

⑤ NE is the number of terminals on the "E" side of the package (or Y−direction).

⑥ ND is the number of terminals on the "D" side of the package (or X−direction). ND = (N/2)−NE.

⑦ Inward end of terminal may be square or circular in shape with radius (b/2) as shown.

⑧ If two values are listed, multiple exposed pad options are available. Refer to device−specific datasheet.

Drawing #: MDP0046
Rev: 10
Date: 12/1/04
Units: mm
JEDEC Reg: MO−220

PACKAGE OUTLINE DRAWING
QFN (QUAD FLAT NO−LEAD) PACKAGE FAMILY
(Formerly Known as LPP)

SOLUTIONS IN SILICON

NOTE: The package drawings shown here may not be the latest versions. For the latest revisions, please refer to the Intersil website at www.intersil.com/design/packages/elantec

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