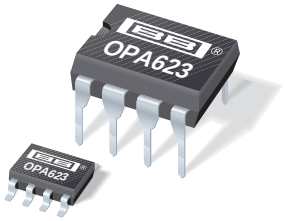
BURR - BROWN®



OPA623

Wide Bandwidth, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- BANDWIDTH: 350MHz, 2.8Vp-p
- HIGH OUTPUT CURRENT: ±70mA
- SLEW RATE: 2100V/µs, 5Vp-p
- DIFFERENTIAL GAIN/PHASE: 0.12%/0.05°
- LOW QUIESCENT CURRENT: ±4mA
- LOW INPUT BIAS CURRENT: 1.2µA
- RISE TIME: 1.9ns, 5Vp-p
- SETTLING TIME: 9ns, 0.1%

APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- HIGH-SPEED DIGITAL COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- LINE DRIVING (50Ω, 75Ω)
- DISTRIBUTION AMP
- CRT OUTPUT STAGE DRIVER
- ACTIVE FILTER

DESCRIPTION

The OPA623 is a current-feedback operational amplifier designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment.

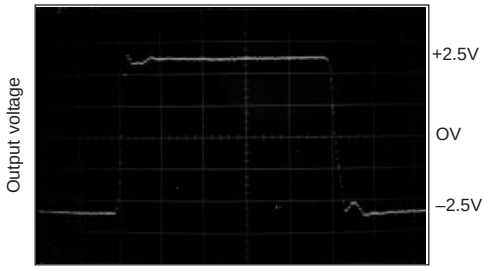
The new circuit design, together with the complementary bipolar process, achieves performance previously unattainable in monolithic integrated circuit technology.

The current-feedback op amp is optimized for wide bandwidth, excellent pulse response, gain flatness, low distortion, and operation at a low quiescent current of ±4mA.

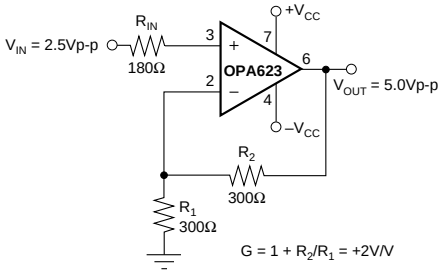
It provides a 350MHz large-signal bandwidth at 2.8Vp-p output voltage, as well as a 2100V/µs slew rate. The gain flatness of 0.05dB over a 30MHz bandwidth makes it suitable for HDTV designs. Another feature of the op amp is its high output current of ±70mA, enabling it to drive two back-terminated 75Ω cables when using the amplifier as a line driver in video routers, distribution amplifiers, and analog and digital communications equipment.

The OPA623 operates from a ±5V supply, is specified for the extended industrial temperature range (–40°C to +85°C), and is available in plastic SO-8 and 8-pin plastic DIP packages.

LARGE SIGNAL PULSE RESPONSE



Output Voltage - 5Vp-p, 5ns/DIV



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

DC-SPECIFICATION

At V_{CC} = ±5VDC, I_Q = ±4mA, R_L = 100Ω, R_{IN} = 210Ω, and T_{AMB} = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE					
Initial			–8	±25	mV
vs Temperature			125		µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	45	50		dB
vs Supply (non-tracking)	V_{CC} = +4.5V to +5.5V		47		dB
vs Supply (non-tracking)	V_{CC} = –4.5V to –5.5V		39		dB
+INPUT BIAS CURRENT					
Initial			–1.2	±4	µA
vs Temperature			7		nA/°C
–INPUT BIAS CURRENT					
Initial			+4.5	±20	µA
vs Temperature			340		nA/°C
INPUT IMPEDANCE					
+Input			2.74 || 1		MΩ || pF
INPUT NOISE	f = 100kHz to 100MHz				
Voltage Noise Density			10		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/(Vn • √5MHz)		89		dB
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±3	±3.2		V
Common-Mode Rejection		43	50		dB
RATED OUTPUT					
Voltage Output	R_L = 100Ω	±3	±3.1		V
Output Current			±70		mA
Closed-Loop Output Impedance	Gain = +2		0.12 || 1.5		Ω || pF
POWER SUPPLY					
Rated Voltage		±4.5		±5.5	VDC
Derated Performance		±4		±6	VDC
Quiescent Current	I_O = 0mA	±3.5	±4	±4.5	mA
Rejection Ratio		45	50		dB

ELECTRICAL (FULL TEMPERATURE RANGE, –40°C to +85°C)

At V_{CC} = ±5VDC, I_Q = ±4mA, R_L = 100Ω, and R_{IN} = 210Ω, unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU MIN	TYP	MAX	UNITS
INPUT OFFSET VOLTAGE				±30	mV
BIAS CURRENT +Input			–1.5	±5	µA
BIAS CURRENT –Input			27	±50	µA
RATED OUTPUT Voltage Output	R_L = 100Ω	±3	±3.1		V
POWER SUPPLY Quiescent Current	I_O = 0mA	±2	±4	±7	mA

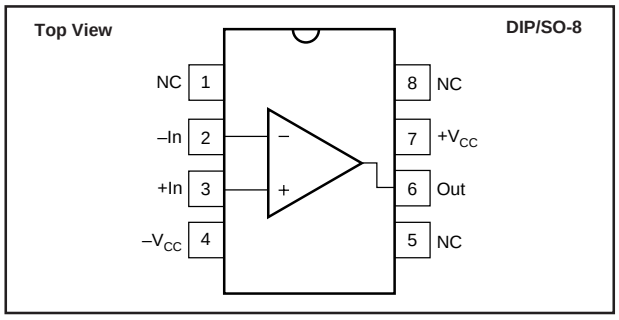
SPECIFICATIONS

AC-SPECIFICATION

At V_{CC} = ±5VDC, I_Q = ±4mA, R_L = 100Ω, R_{IN} = 210Ω, and T_{AMB} = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU MIN	TYP	MAX	UNITS
FREQUENCY DOMAIN					
Large Signal Closed-Loop Bandwidth (–3dB)	V_O = 2.8Vp-p, Gain = +1V/V		340		MHz
	V_O = 2.8Vp-p, Gain = +2V/V		350		MHz
	V_O = 2.8Vp-p, Gain = +5V/V		260		MHz
	V_O = 2.8Vp-p, Gain = +10V/V		210		MHz
	V_O = 2.8Vp-p, Gain = –1V/V		360		MHz
	V_O = 2.8Vp-p, Gain = –2V/V		330		MHz
	V_O = 5.0Vp-p, Gain = +2V/V		240		MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, Gain = +2V/V		290		MHz
GROUP DELAY TIME	Pin 3 to Pin 6, Gain = +2V/V		1.2		ns
DIFFERENTIAL GAIN	G = +2V/V, f = 4.43MHz, R_L = 150Ω V_O = +1.4V		0.12		%
DIFFERENTIAL PHASE	G = +2V/V, f = 4.43MHz, R_L = 150Ω V_O = +1.4V		0.05		Degrees
HARMONIC DISTORTION	Gain = +2V/V				
Second Harmonic	f = 10MHz, V_O = 2.0Vp-p		–56		dBc
Third Harmonic			–59		dBc
Second Harmonic	f = 30MHz, V_O = 2.0Vp-p		–30		dBc
Third Harmonic			–37		dBc
Second Harmonic	f = 50MHz, V_O = 2.0Vp-p		–30		dBc
Third Harmonic			–33		dBc
GAIN FLATNESS PEAKING	Gain = +2V/V				
	V_O = 2.0Vp-p, DC to 30MHz		0.05		dB
	V_O = 2.0Vp-p, DC to 100MHz		0.20		dB
TIME DOMAIN					
Rise Time	Gain = +2V/V, 10% to 90%				
	V_O = 2.0Vp-p		1.4		ns
	V_O = 5.0Vp-p		1.9		ns
Fall Time	Gain = +2V/V, 10% to 90%				
	V_O = 2.0Vp-p		1.4		ns
	V_O = 5.0Vp-p		2.6		ns
SLEW RATE	Gain = +2V/V, Rise Time = 1ns				
	V_O = 0.2Vp-p		140		V/µs
	V_O = 5.0Vp-p		2100		V/µs
SETTLING TIME	Gain = +2V/V, Rise Time = 2ns V_O = $2V_{p-p}$, 0.1%		9		ns

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage(1)	$\pm V_{CC}$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
OPA623AP	8-Pin Plastic DIP	006	–40°C to +85°C
OPA623AU	SO-8 Surface Mount	182	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

INPUT PROTECTION

The need for protection from static damage has long been recognized for MOSFET devices, but all semiconductor devices deserve protection form this potentially damaging source. The OPA623 incorporates on-chip ESD protection diodes as shown in Figure 1. These diodes eliminate the need for external protection diodes, which can add capacitance and degrade AC performance.

As shown, all input pins of the OPA623 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur when the amplifier loses its power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, the diode current should be limited externally to approximately 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using the Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the amplifier input characteristics without necessarily destroying the device. In precision amplifiers, such changes may degrade offset and drift noticeably. For this reason, static protection is strongly recommended when handling the OPA623.

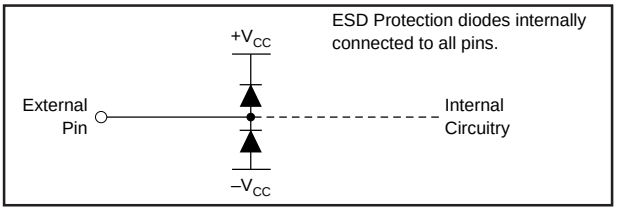
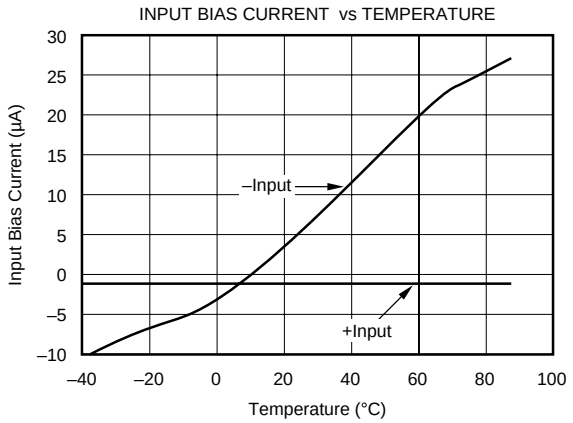
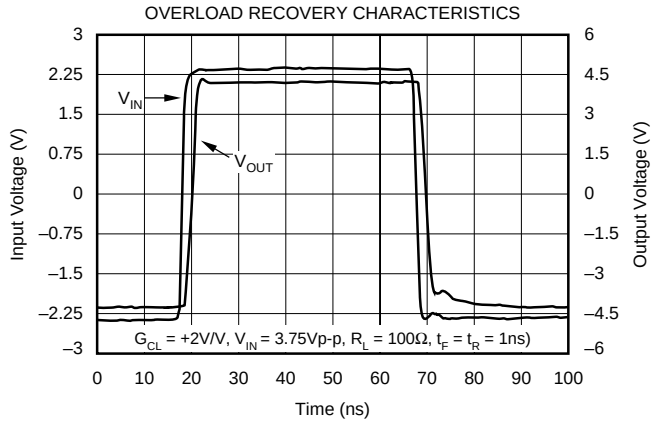


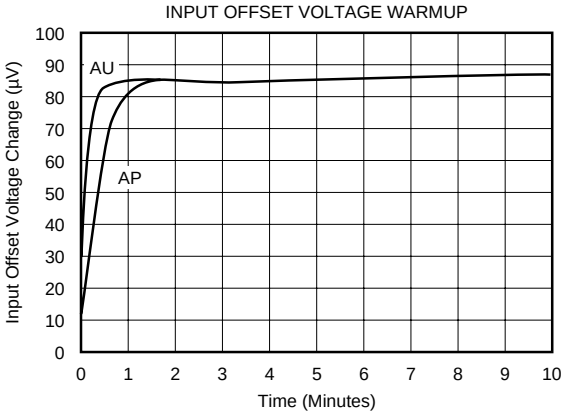
FIGURE 1. Internal ESD Protection.

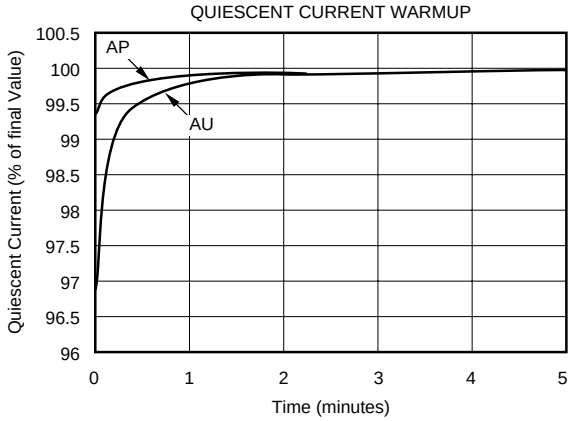
TYPICAL PERFORMANCE CURVES

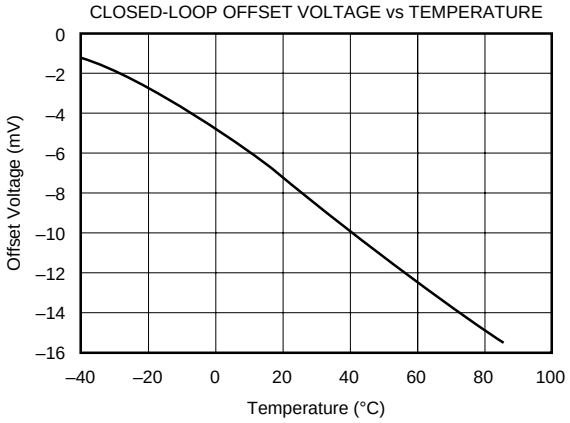
At V_{CC} = ±5VDC, R_L = 100Ω, I_Q = ±4mA, R_{IN} = 150Ω, and T_{AMB} = +25°C unless otherwise noted.

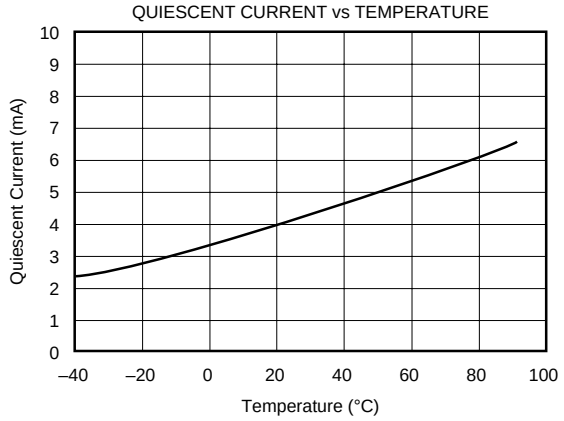








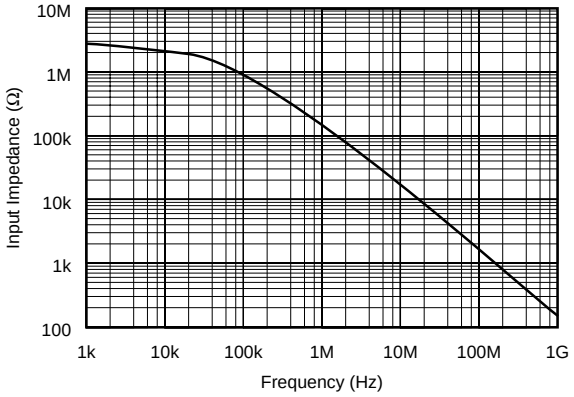




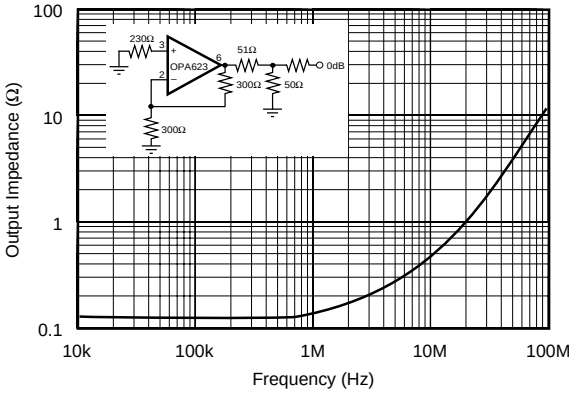
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, I_Q = ±4mA, R_{IN} = 150Ω, and T_{AMB} = +25°C unless otherwise noted.

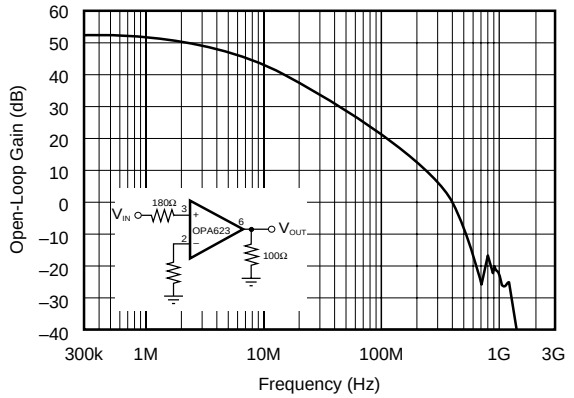
INPUT IMPEDANCE vs FREQUENCY



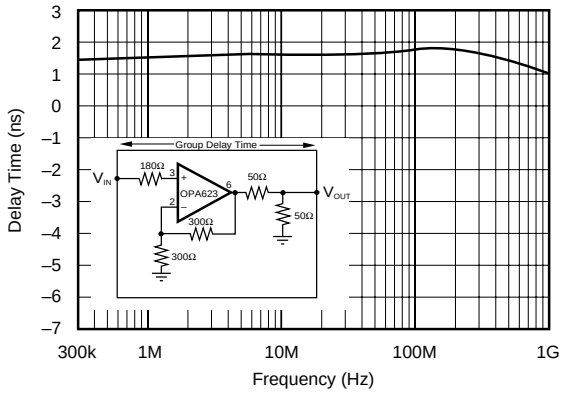
OUTPUT IMPEDANCE vs FREQUENCY



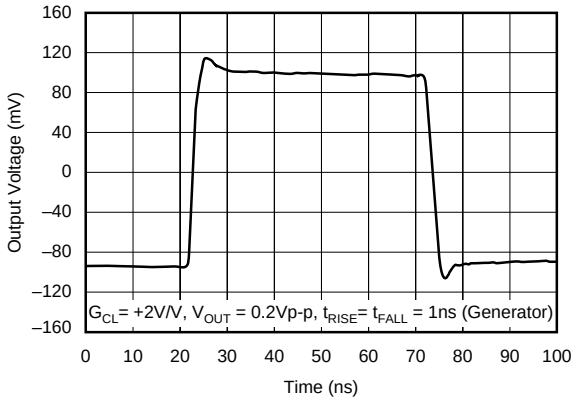
OPEN-LOOP GAIN vs FREQUENCY



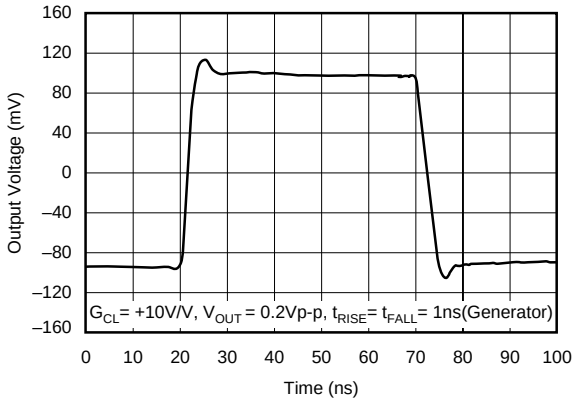
GROUP DELAY TIME



SMALL SIGNAL PULSE RESPONSE

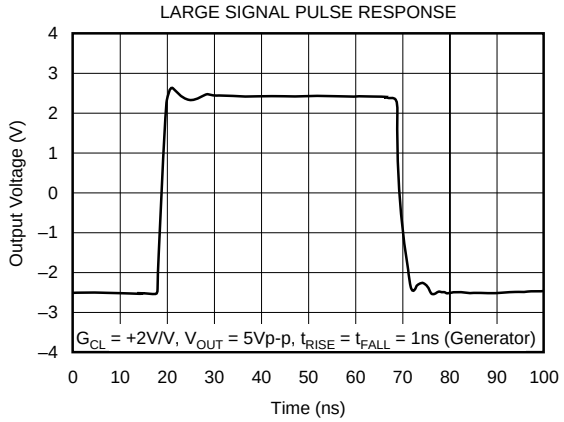


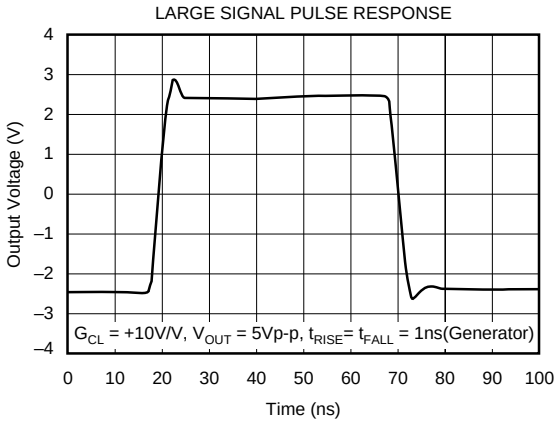
SMALL SIGNAL PULSE RESPONSE

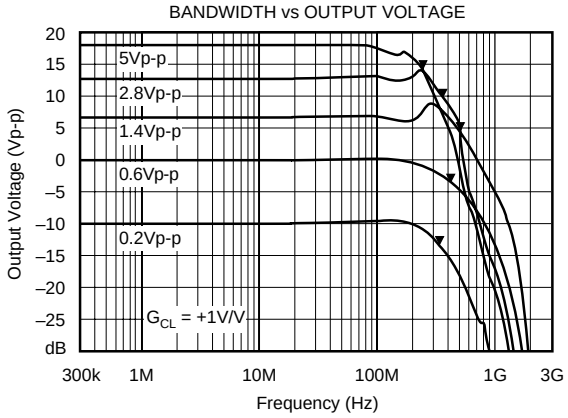


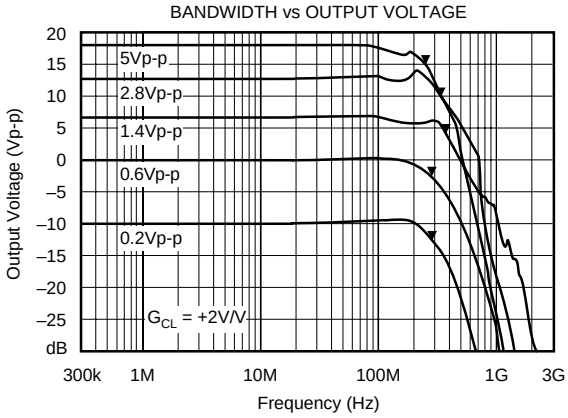
TYPICAL PERFORMANCE CURVES (CONT)

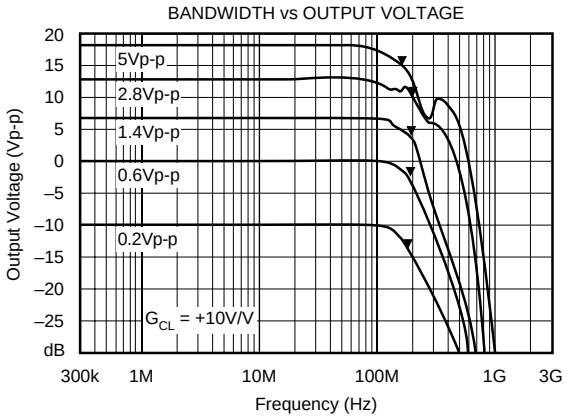
At V_{CC} = ±5VDC, R_L = 100Ω, I_Q = ±4mA, R_{IN} = 150Ω, and T_{AMB} = +25°C unless otherwise noted.

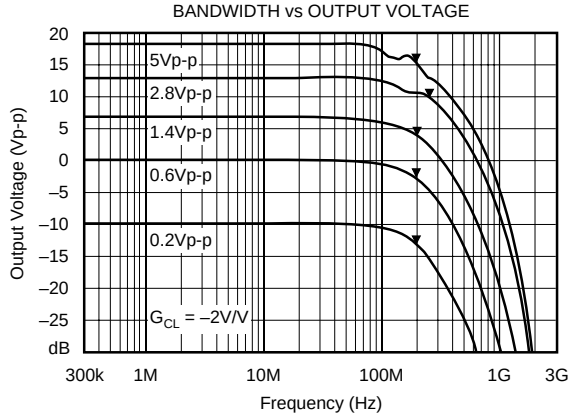








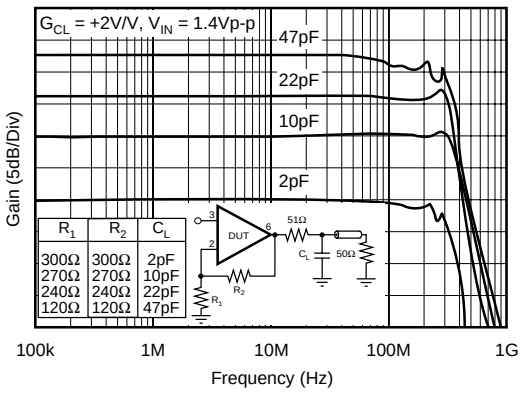




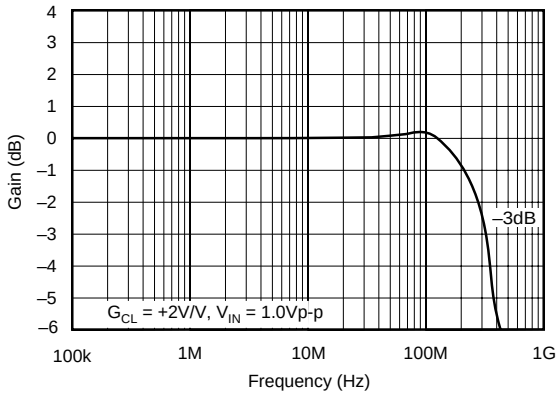
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω, I_Q = ±4mA, R_{IN} = 150Ω, and T_{AMB} = +25°C unless otherwise noted.

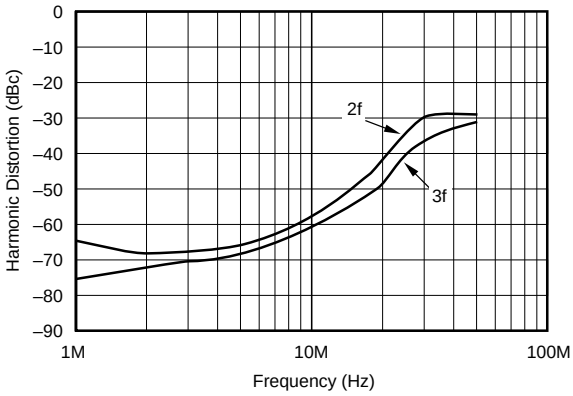
FREQUENCY RESPONSE vs C_{LOAD}



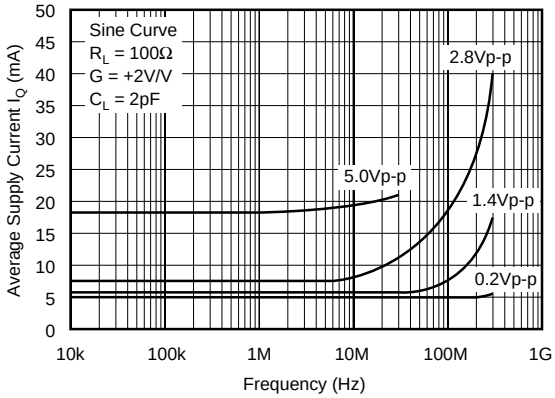
GAIN FLATNESS



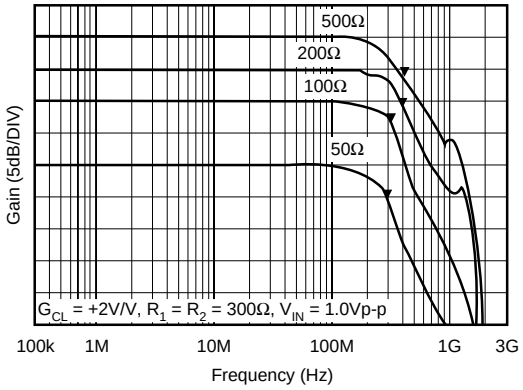
HARMONIC DISTORTION vs FREQUENCY



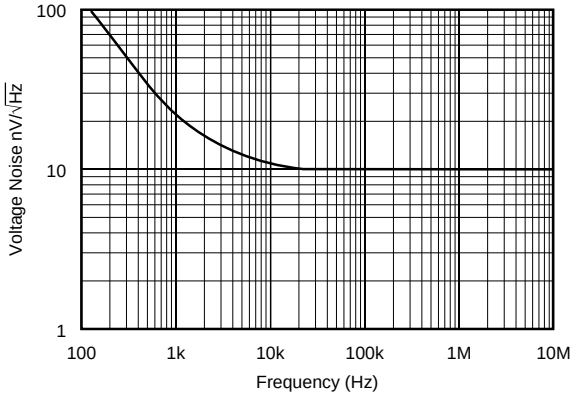
AVERAGE SUPPLY CURRENT vs FREQUENCY



FREQUENCY RESPONSE vs R_{LOAD}



SPECTRAL NOISE VOLTAGE DENSITY



DISCUSSION OF PERFORMANCE

Requiring very low quiescent power, the OPA623 achieves its exceptional AC performance by using the current-feedback topology. This wide-band monolithic operational amplifier is designed for gain applications of up to 20V/V, where power and cost are of primary concern.

Operating from a ±5V supply, the OPA623 consumes only 40mW, yet maintains a 350MHz large-signal bandwidth at V_{OUT} = 2.8Vp-p and a 2100V/µs slew rate. Benefiting from the current-feedback architecture, the OPA623 offers stable operation with no compensation capacitor, even at unity gain.

With its low differential gain and phase errors of typically 0.12% and 0.05° at 4.43MHz, the OPA623 meets the performance and cost requirements of high-volume broadcast and HDTV applications.

The OPA623's large-signal bandwidth, high slew rate, excellent pulse response, and high drive capabilities are features well-suited to wide-band RGB video applications, RF instruments, and even high-speed digital communication systems.

For most circuit configurations, the OPA623 current-feedback op amp can be treated like a conventional op amp. As with a voltage-feedback op amp, the feedback network connected to the inverting input controls the closed-loop gain. But with a current-feedback op amp, the impedance of the feedback network also controls the open-loop gain and frequency response. Feedback resistor values can be selected to provide nearly constant closed-loop bandwidth over a wide range of gains and flat gain adjustment vs frequency.

DESCRIPTION

A wide-band operational transconductance amplifier (OTA) and an output buffer are the main blocks of a current-feedback op amp. The simplified circuit diagram is illustrated in Figure 2. The OTA consists of a complementary unity-gain amplifier and a subsequent current mirror. The input buffer is connected across the inputs of the op amp. The voltage at the high-impedance +In terminal is transferred to the –In terminal at a low impedance. The current mirrors reflect any current flowing into or out of the +In terminal by a fixed ratio to the high-impedance OTA output, which is directly connected to the complementary output buffer. It is designed to drive low-impedance transmission

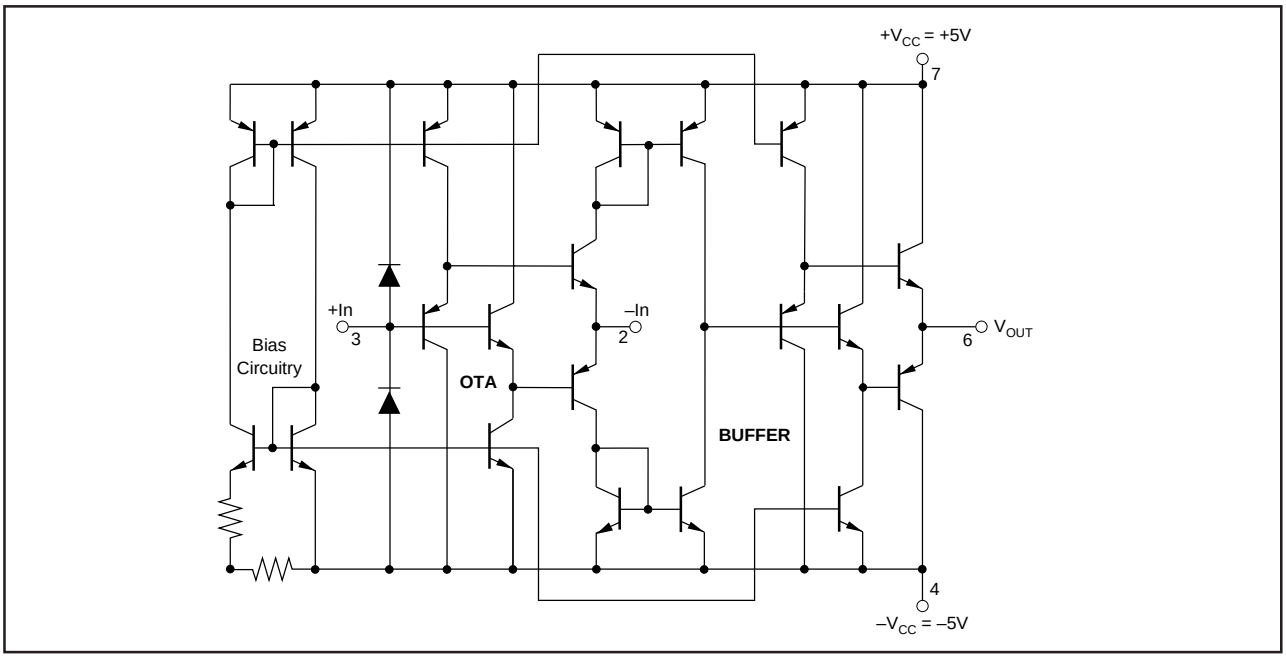


FIGURE 2. Simplified Circuit Diagram.

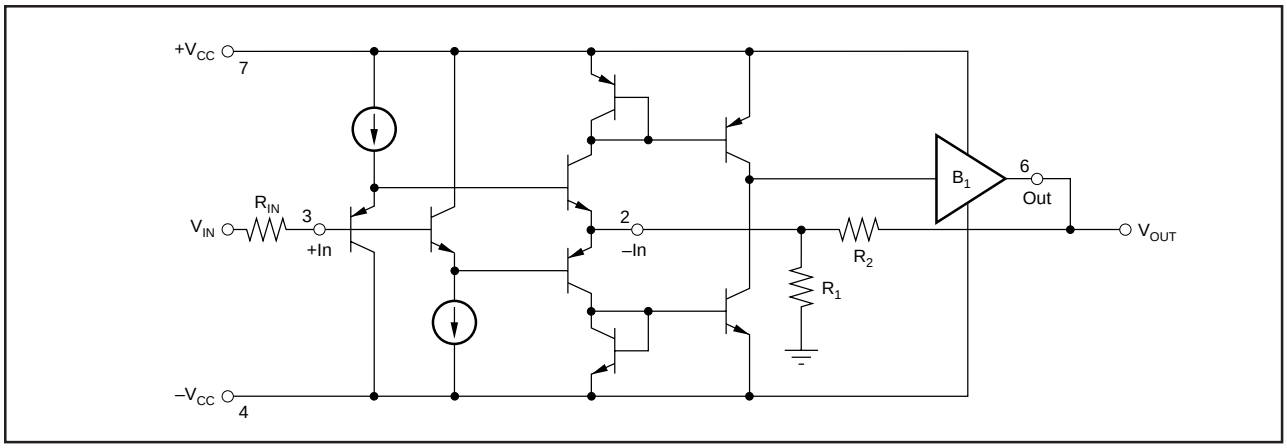


FIGURE 3. Non-Inverting Current-Feedback Op Amp Configuration.

lines or loads. The buffer output is not current-limited or protected.

As can be seen in Figure 3, the feedback in the form of a current is applied through R_2 to the low-impedance inverting input, and the size of $R_2 \parallel R_1$ determines the open-loop gain of the op amp.

The hybrid model shown in Figure 4 describes the AC behavior of a wide-band current-feedback op amp that is not internally compensated. The open-loop frequency response, which is illustrated in Figure 5 for various R_2 values, is determined by two time constants. The elements R and C between the current source output and the output buffer form the dominant open-loop pole T_C. The signal delay time T_D modelled in the output buffer combines several small phase-shifting time constants and delay times. They are distributed throughout the amplifiers and are also present in the feedback loop. As shown in Figure 5, increasing $R_2 \parallel R_1$ leads to a decreasing open-loop gain. The ratio of the two time constants T_C and T_D also determines the product $G_{OL} \bullet G_{CL}$ for optimal closed-loop frequency response:

$$G_{OL} = G_{CL} \bullet \frac{T_C}{2T_D}$$

The two time constants T_C and T_D, however, are fixed by the op amp design. But varying $R_2 \parallel R_1$ externally in the feedback loop allows for variation of the open-loop gain G_{OL} versus the closed-loop gain G_{CL}. This keeps the product $G_{OL} * G_{CL}$ constant, which is the theoretical condition for optimally flat frequency response.

This variation may be beneficial when driving high capacitive loads. Setting the open-loop gain externally also allows the circuit to be optimized to a wide range of capacitive loads, as shown in Figure 7 for a closed-loop gain of +2V/V and a capacitive load of up to 47pF.

It should be noted here that higher open-loop gain (resulting from lower feedback resistors) also yields lower distortion.

With external control of the open-loop characteristics of the op amp, dynamic behavior can be tailored to individual application requirements, and the open-loop gain selection

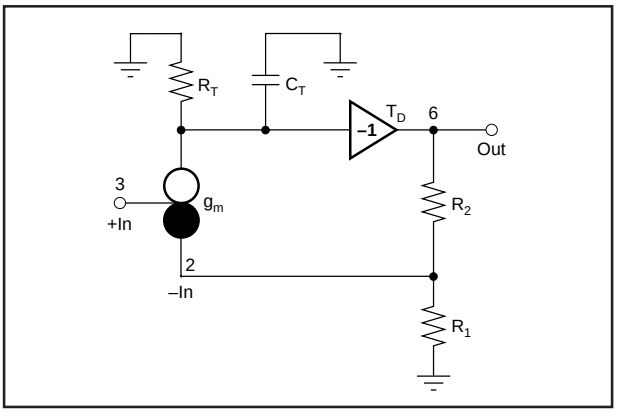


FIGURE 4. Hybrid Model OPA623.

provides a nearly constant closed-loop bandwidth, as shown in Figure 6 for various gains with an optimal flat frequency response. This behavior stands in contrast to op amps that are internally compensated for stable unity-gain operation, where the bandwidth is inversely proportional to the closed-loop gain, sharply limiting the bandwidth and slew rate at high output levels and gains.

In general, lower feedback resistors produce wider bandwidth, more frequency response peaking, and more pulse response overshooting. Higher feedback resistors results in an overdamped response with little or no peaking and overshooting.

Component pin and layout capacitances together with trace and wire board inductances from a resonant IC circuit can lead to oscillations of several hundreds of MHz. This very high frequency oscillation leads to an excessive increase in supply current which can destroy the device.

A resistor (100Ω to 250Ω) in series and close to the high-impedance, non-inverting input damps the LC circuit and generates a safe operation.

THERMAL CONSIDERATIONS

The OPA623 does not require a heat sink for operation in most environments. The use of a heat sink, however, will

reduce the internal thermal rise, resulting in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, (P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load). Although the P_{DQ} is very low (40mW at $V_{CC} = \pm 5V$), care should be taken when a signal is applied. For high-speed op amps, a more precise approach to determine power consumption is to measure the average total quiescent current for several typical load conditions. The power consumption of the OPA623 is influenced by the kind of signal, the applied signal frequency, the output voltage, load resistor, and the repetition rate of the signal transitions. Figure 8 shows the average supply current versus the frequency of an applied sine wave for various output voltages. Figure 9 illustrates the average supply current versus the repetition frequency of an applied square wave signal.

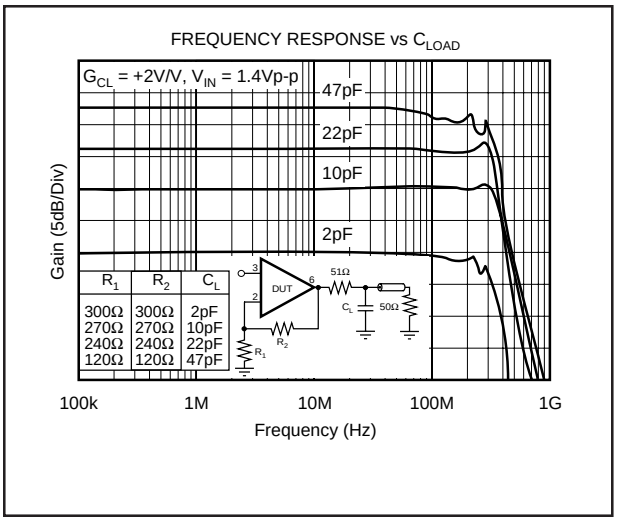


FIGURE 7. Frequency Response vs C_{LOAD}.

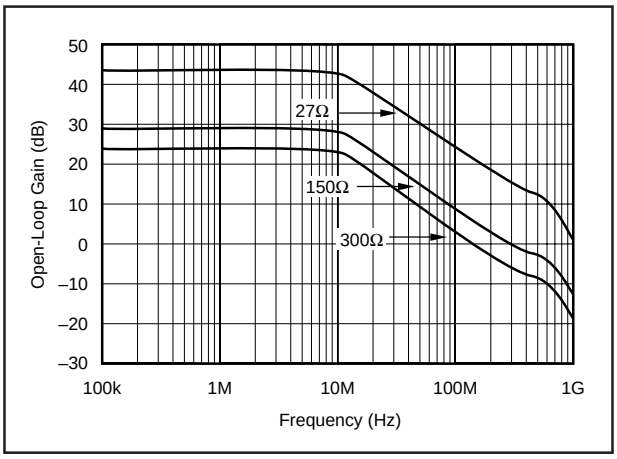


FIGURE 5. Open-Loop Gain vs $R_2 \parallel R_1$.

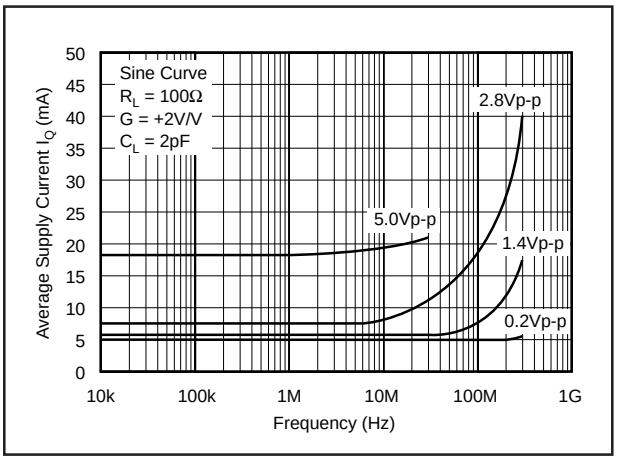


FIGURE 8. Average Supply Current vs Frequency (sinewave).

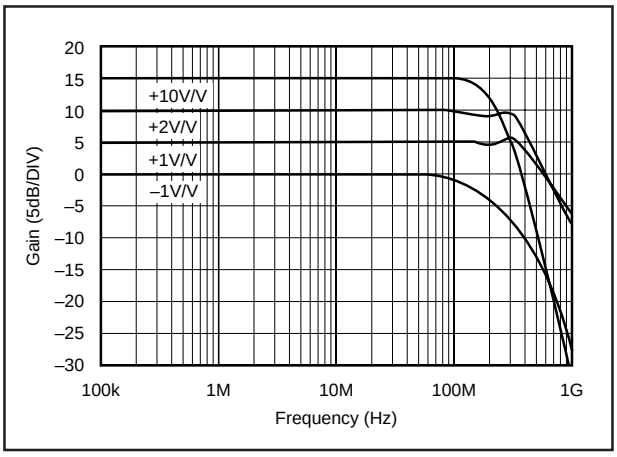


FIGURE 6. Optimum Frequency Response vs Closed-Loop Gain.

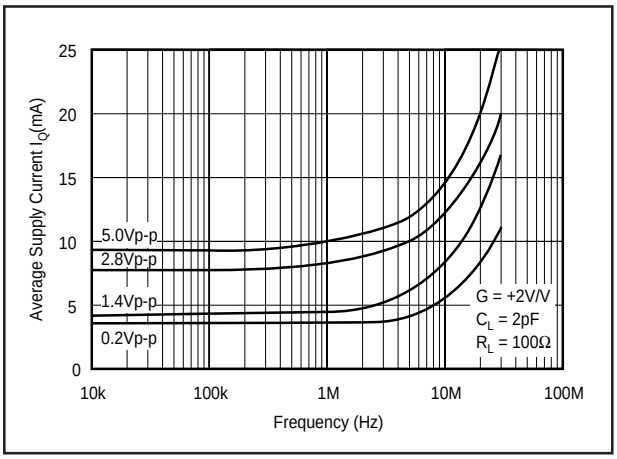


FIGURE 9. Average Supply Current vs Frequency (squarewave).

CIRCUIT LAYOUT

The high-frequency performance of the operational amplifier OPA623 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- A resistor (100Ω to 250Ω) in series and close to the high-impedance, noninverting input is necessary to reduce peaking; this resistor prevents any very high-frequency oscillations at the op amp input, which can lead to an excessive increase in quiescent current.
- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF) with a parallel 470pF ceramic chip capacitor. Surface-mount types are recommended because of their low lead inductance. Although the OPA623 operates at a low quiescent current, high charging and discharging currents flow during steep transitions.
- PC board traces for power lines should be wide to reduce impedance and inductance.
- Make short low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout, however, do not extend the ground plane under high-impedance nodes such as the amplifier's input terminals, which are sensitive to stray capacitances.
- Sockets are not recommended because they add significant inductance and parasitic capacitance.
- Use low-inductance, surface-mounted components. Circuits using all surface-mount components with the OPA623AU will offer the best AC performance.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Make the feedback trace as short as possible. The inverting input is sensitive to stray capacitances that lead to peaking in the frequency response. A stray capacitance at the inverting input increases the gain at high frequencies.

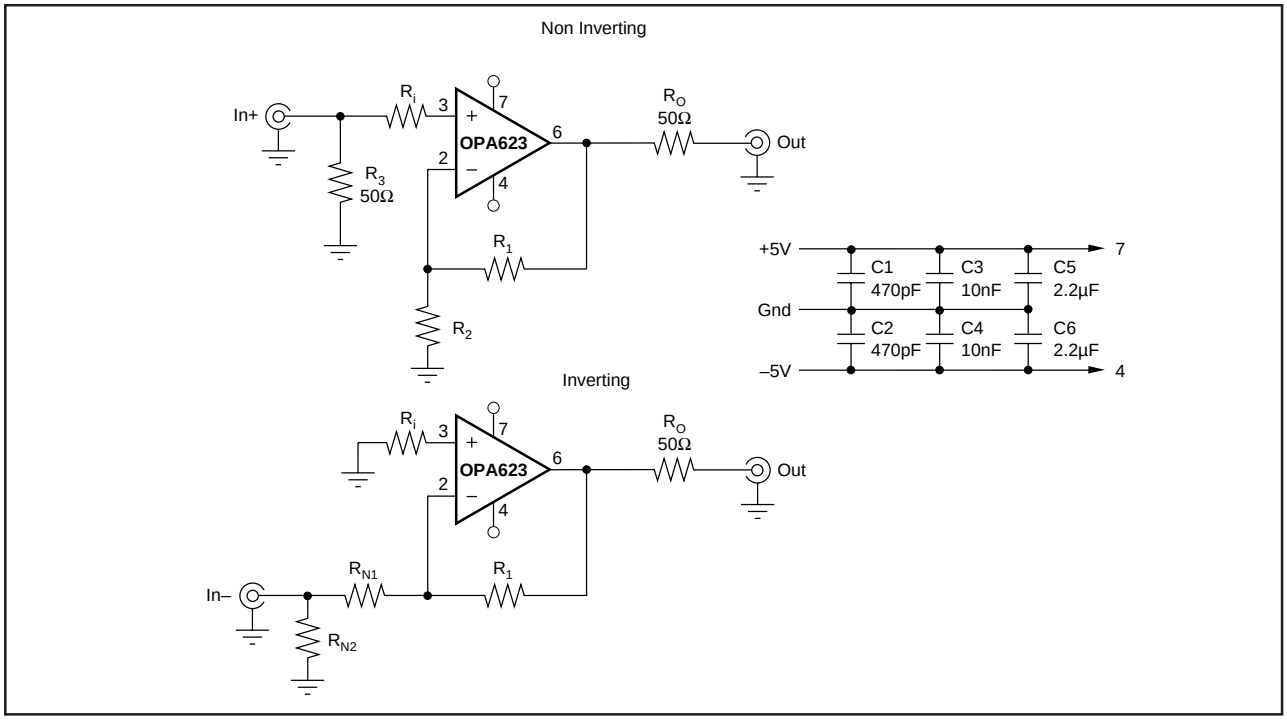


FIGURE 10. Circuit Schematic for Non-inverting and Inverting Configuration. Refer to Table I for Resistor Values.

	OPA623AP						OPA623AU					
	GAIN						GAIN					
COMPONENT	–2	–1	+1	+2	+5	+10	–2	–1	+1	+2	+5	+10
R_i	150Ω	150Ω	200Ω	180Ω	100Ω	100Ω	150Ω	150Ω	270Ω	180Ω	100Ω	100Ω
R_1	390Ω	390Ω	360Ω	300Ω	300Ω	130Ω	390Ω	390Ω	470Ω	300Ω	300Ω	160Ω
R_2	—	—	—	300Ω	75Ω	15Ω	—	—	—	300Ω	76Ω	18Ω
R_{N1}	200Ω	390Ω	—	—	—	—	200Ω	390Ω	—	—	—	—
R_{N2}	68Ω	56Ω	—	—	—	—	68Ω	56Ω	—	—	—	—
Typical Bandwidth (MHz)												
V_{OUT} = 0.2Vp-p	200	—	320	290	—	170	200	—	320	290	—	170
V_{OUT} = 2.8Vp-p	330	360	340	350	260	210	330	360	340	350	260	210

TABLE I. Recommended Component Values.

APPLICATIONS INFORMATION

The precise pulse response and high slew rate enables the OPA623 to be used in digital communication systems. Figure 12 shows the circuit schematic of an output amplifier with a gain of +2V/V, which can drive a 75Ω coaxial cable with a high-speed data stream of 140Mbit/s. Figure 13, for a binary 0, and Figure 14, for a binary 1, shows the pulse masks of the CCITT recommendation G.703 and the corresponding pulse responses of the OPA623. The signal code at the file rate of 139.264Mbit/s is CMI, the signal amplitude is 1Vp-p with ±11dB amplitude limits. Naturally, the OPA623 can also be used for HDB3 encoded 34Mbit/s,155Mbit/s, STM-1, and 155Mbit/s B-ISDN transmission systems.

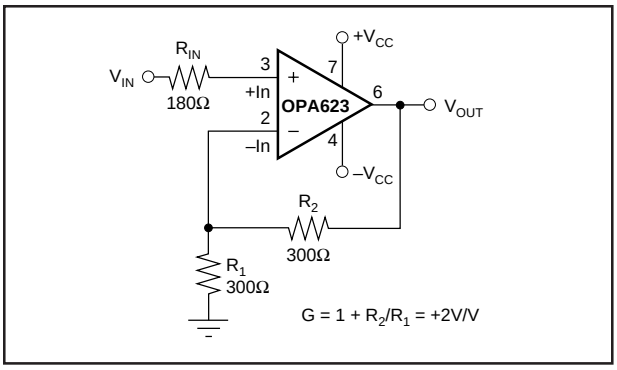
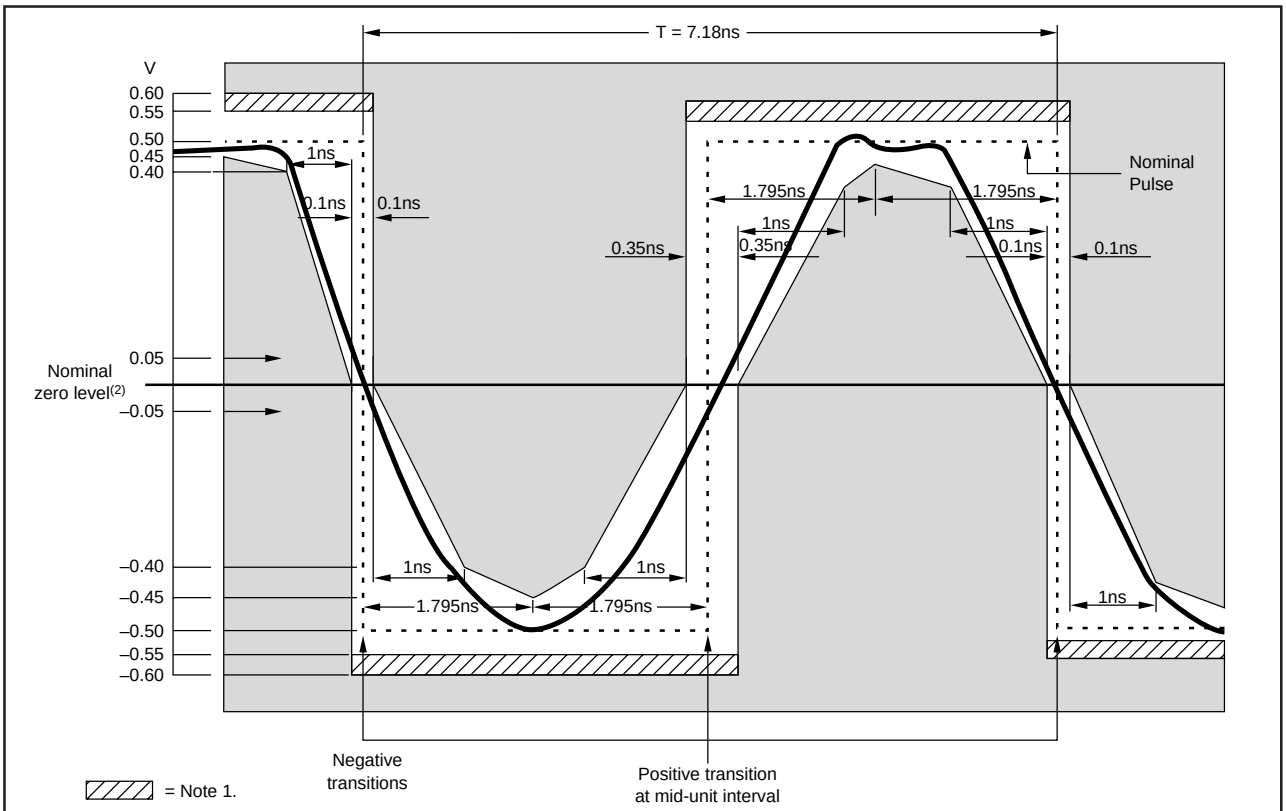


FIGURE 12. Driver Amplifier for a Digital 140Mbit/s Transmission system.



NOTE: (1) The maximum "steady state" amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

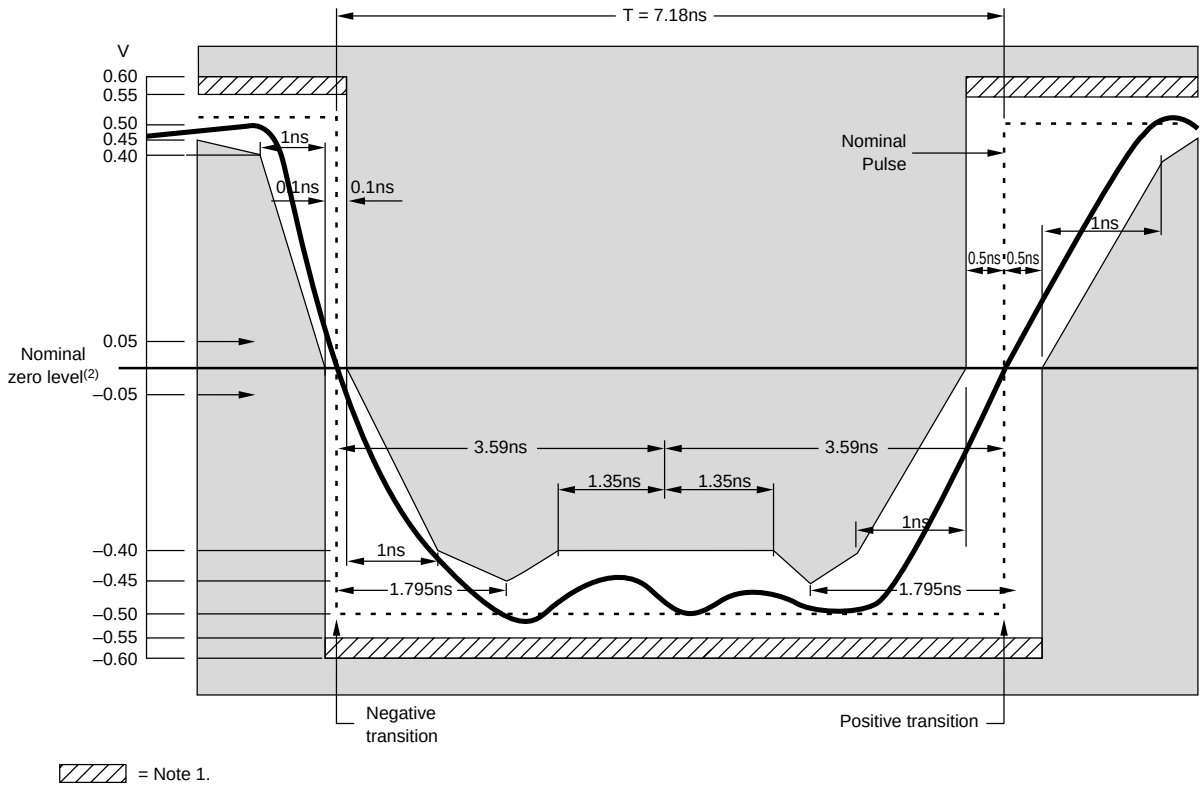
(2) For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05V of the nominal zero level of masks.

(3) Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a 139264kHz timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all-0s and all-1s signals, respectively. (In practice, the signal may contain frame alignment bits per Rec. G.751.)

(4) For the purpose of these masks, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

FIGURE 13. Mask of a Pulse Corresponding to a Binary 0 per CCITT Recommendation G.703.



NOTE: (1) The maximum "steady state" amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

(2) For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01µF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05V of the nominal zero level of masks.

(3) Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a 139264kHz timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all-0s and all-1s signals, respectively. (In practice, the signal may contain frame alignment bits per Rec. G.751.)

(4) For the purpose of these masks, the rise time and decay time should be measured between –0.4V and 0.4V, and should not exceed 2ns.

(5) The inverse pulse will have the same characteristics. Note that the timing tolerance at the zero level of the negative and positive transitions are ±0.1ns and ±0.5n, respectively.

FIGURE 14. Mask of a Pulse Corresponding to a Binary 1 per CCITT Recommendation G.703.

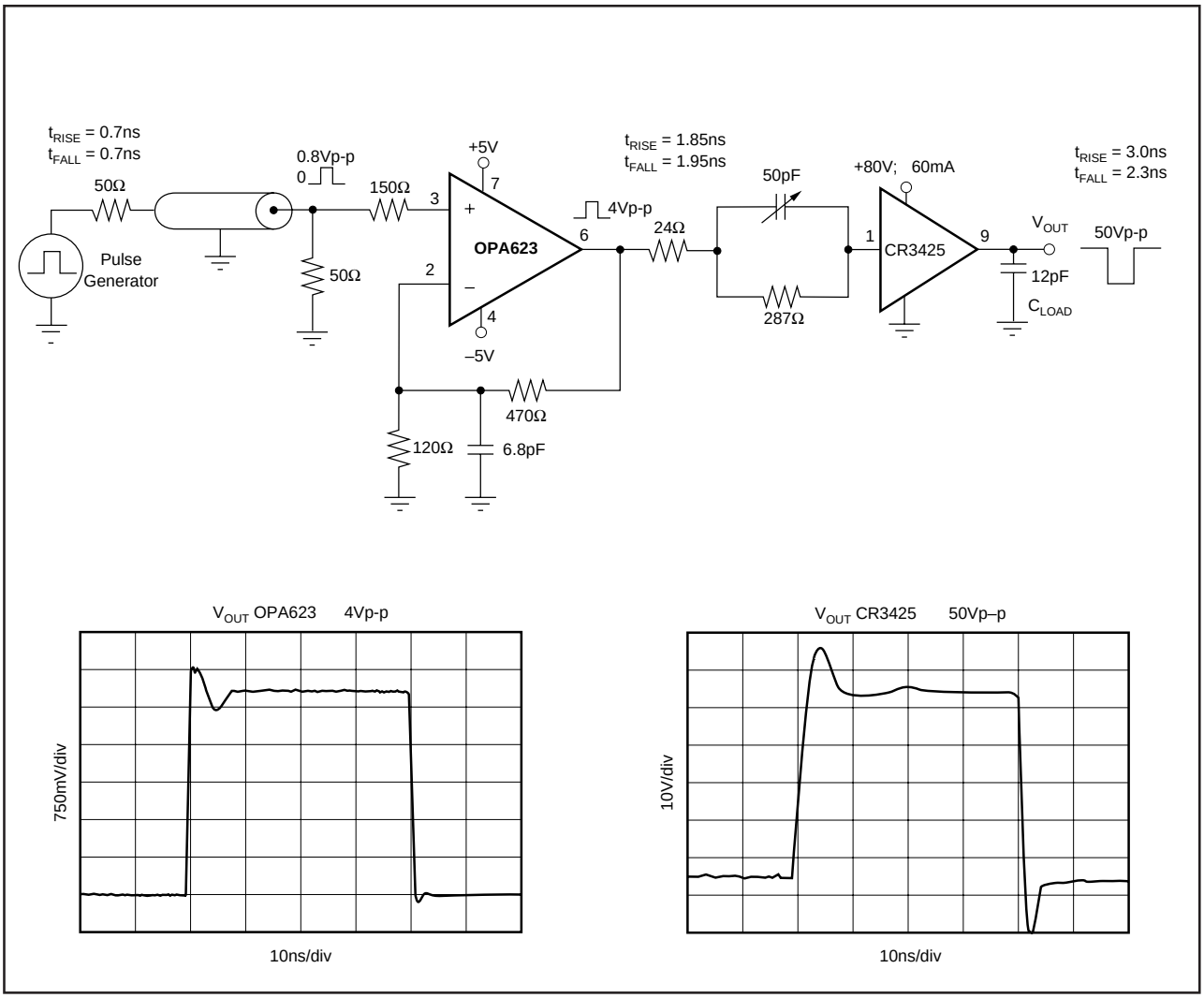


FIGURE 15. Video Amplifier for High Resolution Monitor (1600 x 1200 pixel).

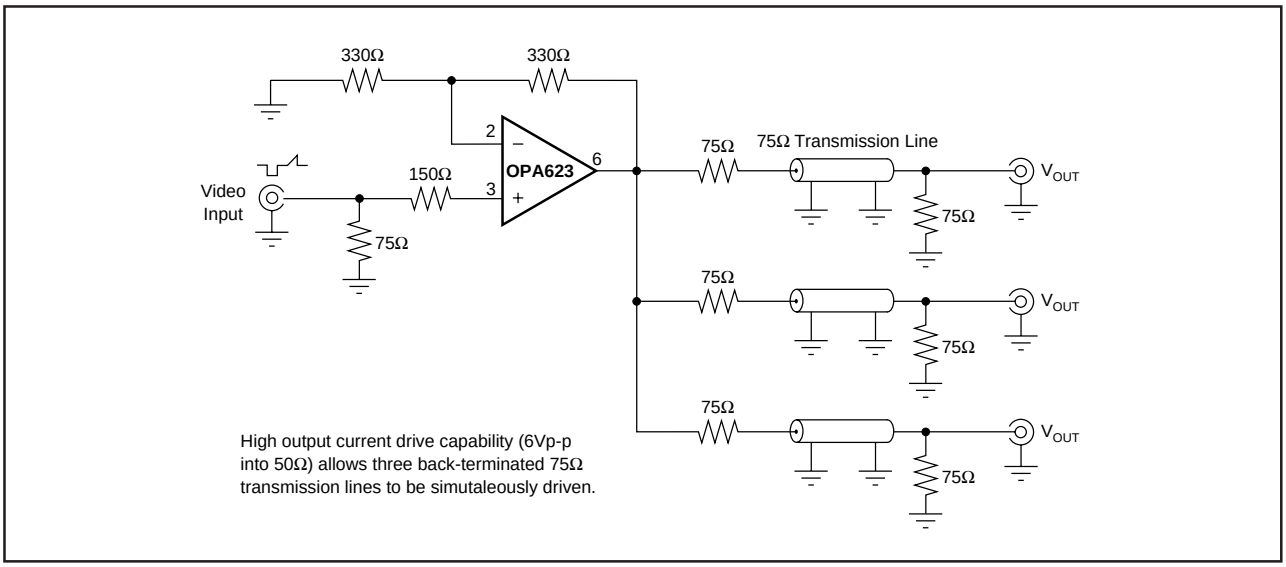


FIGURE 16. Video Distribution Amplifier.