Data Sheet September 1998 File Number 2859.3

700ns, Low Distortion, Precision Sample and Hold Amplifier

The HA-5340 combines the advantages of two sample/ hold architectures to create a new generation of monolithic sample/hold. High amplitude, high frequency signals can be sampled with very low distortion being introduced. The combination of exceptionally fast acquisition time and specified/characterized hold mode distortion is an industry first. Additionally, the AC performance is only minimally affected by additional hold capacitance.

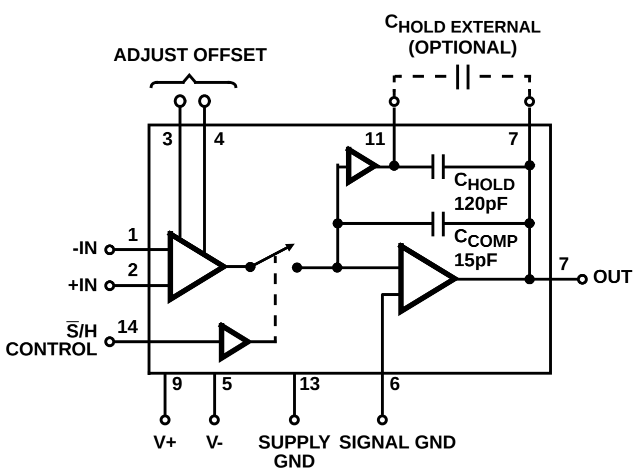
To achieve this level of performance, the benefits of an integrating output stage have been combined with the advantages of a buffered hold capacitor. To the user this translates to a front-end stage that has high bandwidth due to charging only a small capacitive load and an output stage with constant pedestal error which can be nulled out using the offset adjust pins. Since the performance penalty for additional hold capacitance is low, the designer can further minimize pedestal error and droop rate without sacrificing speed.

Low distortion, fast acquisition, and low droop rate are the result, making the HA-5340 the obvious choice for high speed, high accuracy sampling systems. For a Military temperature range version request the HA-5340/883 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA3-5340-5	0 to 75	14 Ld PDIP	E14.3
HA9P5340-5	0 to 75	16 Ld SOIC	M16.3

Functional Diagram



Features

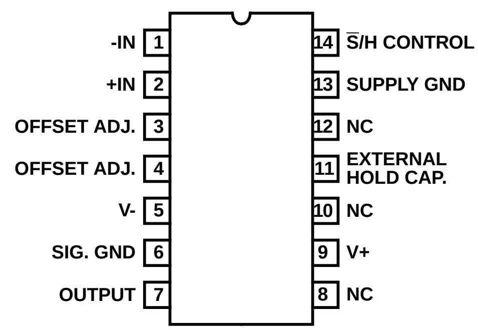
- Fast Acquisition Time (0.01%) 700ns
- Fast Hold Mode Settling Time (0.01%). 200n
- Low Distortion (Hold Mode) . . . . -72dBc (V_{IN} = 200kHz, f_S = 450kHz, $5V_{P-P}$)
- Bandwidth Minimally Affected By External C_H
- Fully Differential Analog Inputs
- Built-In 135pF Hold Capacitor
- Pin Compatible with HA-5320

Applications

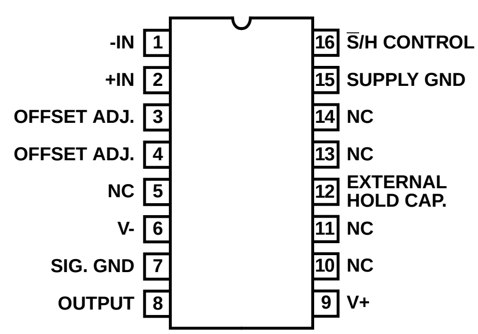
- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR
- RADAR

Pinouts

HA-5340 (PDIP)
TOP VIEW



HA-5340 (SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage 24V
Digital Input Voltage . . . . +8V, -6V
Output Current, Continuous . . . . ±20mA

Operating Conditions

Temperature Range
HA-5340-5 . . . . 0^oC to 75^oC
Supply Voltage Range (Typical) . . . . ±12V to ±18V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	90	N/A
SOIC Package	95	N/A

Maximum Junction Temperature (Plastic Package, Note 1) . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation must be designed to maintain the junction temperature below 150^oC for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-5340-5 MIN	HA-5340-5 TYP	HA-5340-5 MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-10	-	+10	V
Input Resistance (Note 3)		25	-	1	-	MΩ
Input Capacitance		25	-	-	3	pF
Input Offset Voltage		25	-	-	1.5	mV
		Full	-	-	3.0	mV
Offset Voltage Temperature Coefficient		Full	-	-	30	$\mu V/^oC$
Bias Current		25	-	±70	-	nA
		Full	-	-	±350	nA
Offset Current		25	-	±50	-	nA
		Full	-	-	±350	nA
Common Mode Range		Full	-10	-	+10	V
CMRR	±10V, Note 4	25	-	83	-	dB
		Full	72	-	-	dB
TRANSFER CHARACTERISTICS						
Gain	DC	25	110	140	-	dB
Gain Bandwidth Product	C_H External = 0pF	Full	-	10	-	MHz
	C_H External = 100pF	Full	-	9.6	-	MHz
	C_H External = 1000pF	Full	-	6.7	-	MHz
TRANSIENT RESPONSE						
Rise Time	200mV Step	25	-	20	30	ns
Overshoot	200mV Step	25	-	35	50	%
Slew Rate	10V Step	25	40	60	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage	V_{IH}	Full	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	V
Input Current	V_{IL} = 0V	Full	-	7	40	µA
	V_{IH} = 5V	Full	-	4	40	µA

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5340-5			UNITS
			MIN	TYP	MAX	
OUTPUT CHARACTERISTICS						
Output Voltage		Full	-10	-	+10	V
Output Current		Full	-10	-	+10	mA
Full Power Bandwidth (Note 5)		Full	0.6	0.9	-	MHz
Output Resistance	Hold Mode	25	-	0.05	0.1	Ω
		Full	-	0.07	0.15	Ω
Total Output Noise DC to 10MHz	Sample Mode	25	-	325	400	μV_{RMS}
	Hold Mode	25	-	325	400	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = 200kHz, $20V_{P-P}$	Full	-	115	-	dB
Total Harmonic Distortion	V_{IN} = 200kHz, $5V_{P-P}$	Full	-90	-100	-	dBc
	V_{IN} = 200kHz, $10V_{P-P}$	Full	-76	-82	-	dBc
	V_{IN} = 200kHz, $20V_{P-P}$	Full	-70	-74	-	dBc
	V_{IN} = 500kHz, $5V_{P-P}$	Full	-66	-75	-	dBc
Intermodulation Distortion	V_{IN} = $10V_{P-P}$, f_1 = 20kHz, f_2 = 21kHz	Full	-78	-83	-	dBc
HOLD MODE (50% Duty Cycle S/H)						
Signal to Noise Ratio (RMS Signal to RMS Noise) f_S = 450kHz	V_{IN} = 200kHz, $5V_{P-P}$	25	-	76	-	dB
	V_{IN} = 200kHz, $10V_{P-P}$	25	-	76	-	dB
Total Harmonic Distortion f_S = 450kHz	V_{IN} = 200kHz, $5V_{P-P}$	25	-	-72	-	dBc
	V_{IN} = 200kHz, $10V_{P-P}$	25	-	-66	-	dBc
	V_{IN} = 200kHz, $20V_{P-P}$	25	-	-56	-	dBc
f_S = 450kHz	V_{IN} = 100kHz, $5V_{P-P}$	25	-	-84	-	dBc
	V_{IN} = 100kHz, $10V_{P-P}$	25	-	-71	-	dBc
	V_{IN} = 100kHz, $20V_{P-P}$	25	-	-61	-	dBc
f_S = $2f_{IN}$(Nyquist)	V_{IN} = 20kHz, $5V_{P-P}$	25	-	-95	-	dBc
	V_{IN} = 50kHz, $5V_{P-P}$	25	-	-91	-	dBc
	V_{IN} = 100kHz, $5V_{P-P}$	25	-	-82	-	dBc
Intermodulation Distortion f_S = 450kHz	V_{IN} = $10V_{P-P}$ (f_1 = 20kHz, f_2 = 21kHz)	25	-	-79	-	dBc
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	10V Step to 0.01%	25	-	700	-	ns
		Full	-	-	900	ns
	10V Step to 0.1%	25	-	430	600	ns
Droop Rate	C_H = Internal	25	-	0.1	-	µV/µs
		Full	-	-	95	µV/µs
Hold Step Error	V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns	25	-	15	-	mV
Hold Mode Settling Time	To ±1mV	Full	-	200	300	ns
Hold Mode Feedthrough	$20V_{P-P}$, 200kHz, Sine	Full	-	-76	-	dB
EADT (Effective Aperture Delay Time)		25	-	-15	-	ns
Aperture Uncertainty		25	-	0.2	-	ns

Electrical Specifications V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2kΩ, C_L = 60pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5340-5 MIN	HA-5340-5 TYP	HA-5340-5 MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	19	25	mA
Negative Supply Current		Full	-	19	25	mA
PSRR	10% Delta	Full	75	82	-	dB

NOTES:

3. Derived from Computer Simulation only, not tested.
4. +CMRR is measured from 0V to +10V, -CMRR is measured from 0V to -10V.
5. Based on the calculation FPBW = Slew Rate/$2\pi V_{PEAK}$ (V_{PEAK} = 10V).

Test Circuits and Waveforms

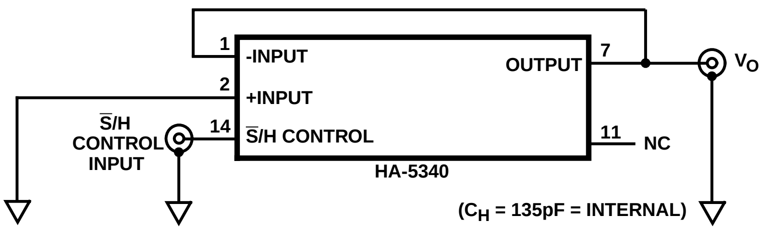
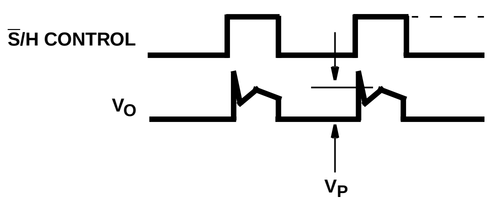


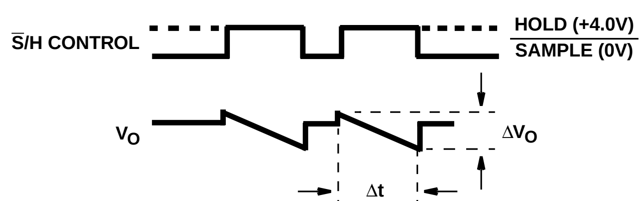
FIGURE 1. HOLD STEP ERROR AND DROOP RATE



NOTE:

6. Observe the "hold step" voltage V_P.

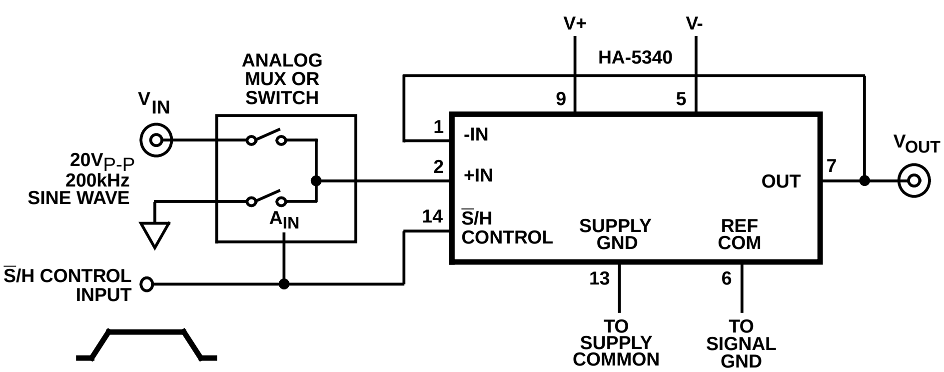
FIGURE 2. HOLD STEP ERROR



NOTES:

7. Observe the voltage "droop", $\Delta V_O/\Delta t$.
8. Measure the slope of the output during hold, $\Delta V_O/\Delta t$.
9. Droop can be positive or negative - usually to one rail or the other not to GND.

FIGURE 3. DROOP RATE TEST



NOTE:

10. Feedthrough in

$$dB = 20\log\frac{V_{OUT}}{V_{IN}} \quad \text{where:}$$

V_{OUT} = V_{P-P}, Hold Mode,
V_{IN} = V_{P-P}

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

Application Information

The HA-5340 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Intersil Application Note AN517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01μF to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. GND) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5340 includes a 135pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Teflon®, polystyrene and polypropylene dielectric capacitor types offer good performance over the specified operating temperature range.

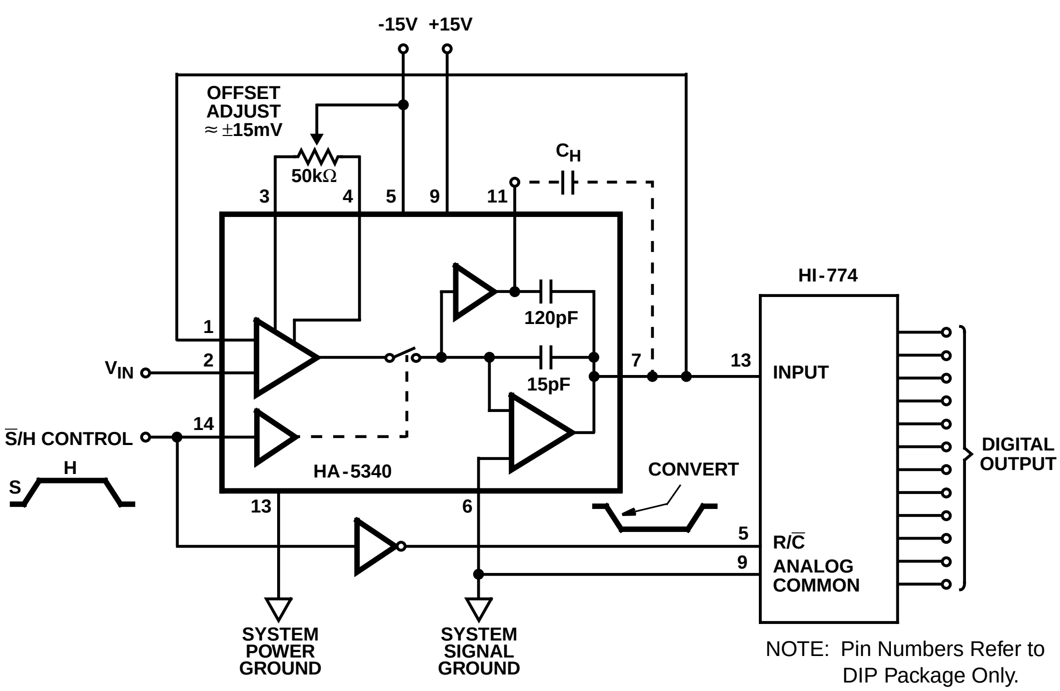
The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Typical Application

Figure 5 shows the HA-5340 connected as a unity gain noninverting amplifier - its most widely used configuration. As an input device for a fast successive - approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5340's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The HA-5340 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.



NOTE: Pin Numbers Refer to DIP Package Only.

FIGURE 5. TYPICAL HA-5340 CONNECTIONS; NONINVERTING UNITY GAIN MODE

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, Unless Otherwise Specified

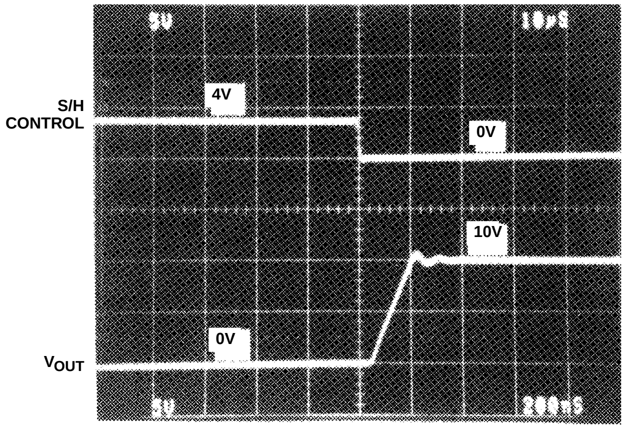


FIGURE 6. T_{ACQ} POS 0 TO +10 STEP

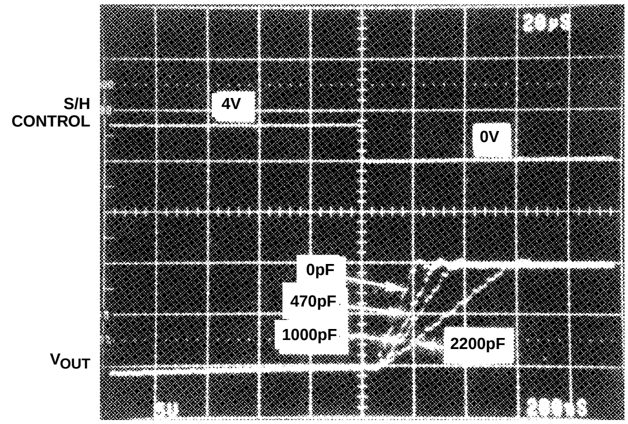


FIGURE 7. T_{ACQ} vs ADDITIONAL C_H

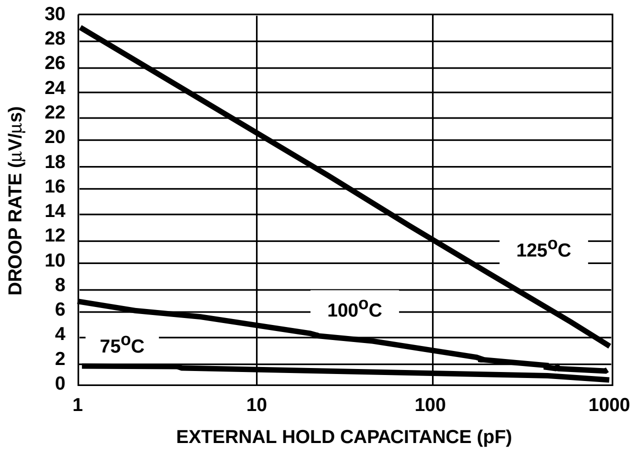


FIGURE 8. DROOP RATE vs HOLD CAPACITANCE

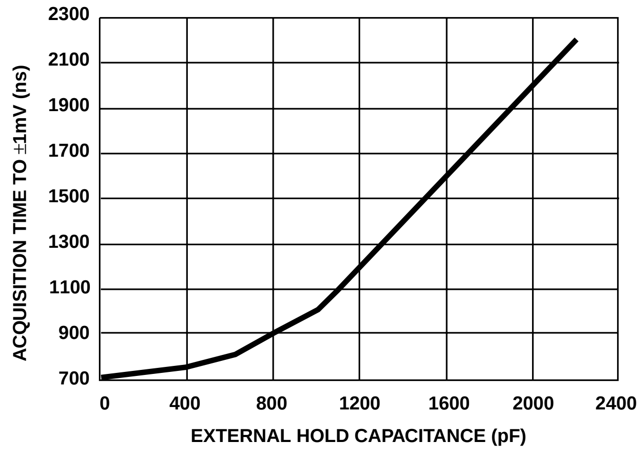


FIGURE 9. ACQUISITION TIME (0.01%) vs HOLD CAPACITANCE

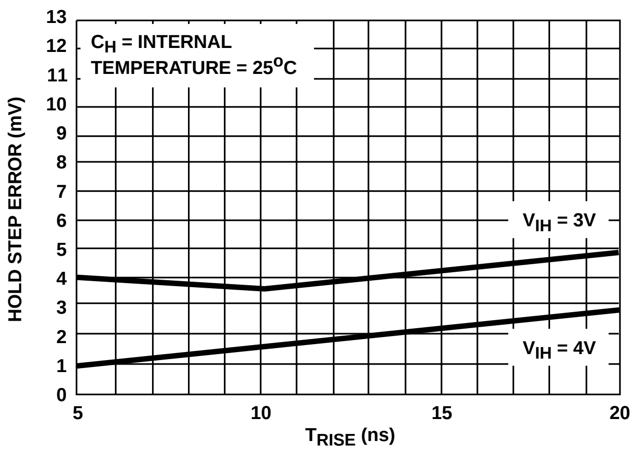


FIGURE 10. HOLD STEP ERROR vs T_{RISE}

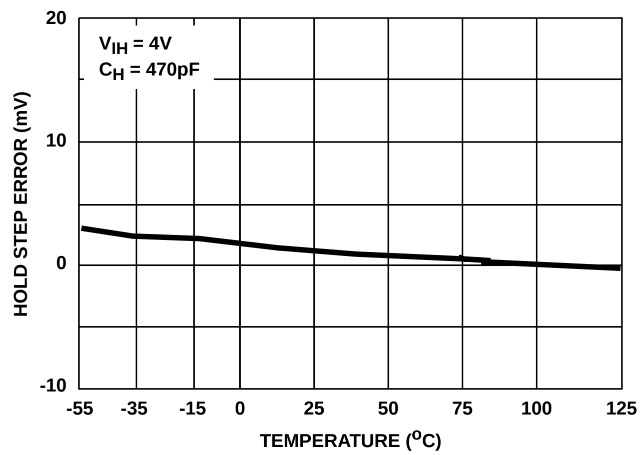


FIGURE 11. HOLD STEP ERROR vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, Unless Otherwise Specified **(Continued)**

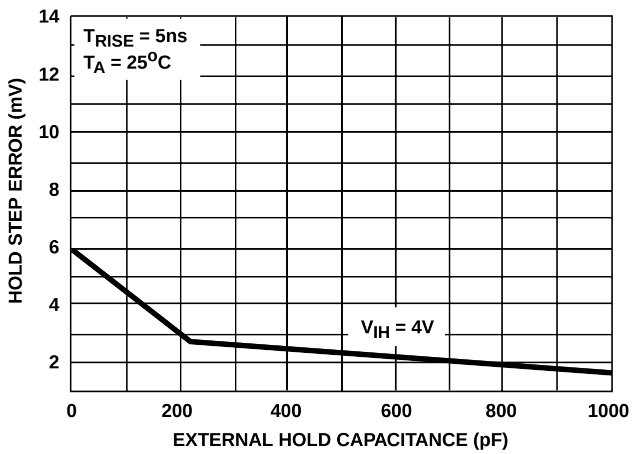


FIGURE 12. HOLD STEP ERROR vs HOLD CAPACITANCE

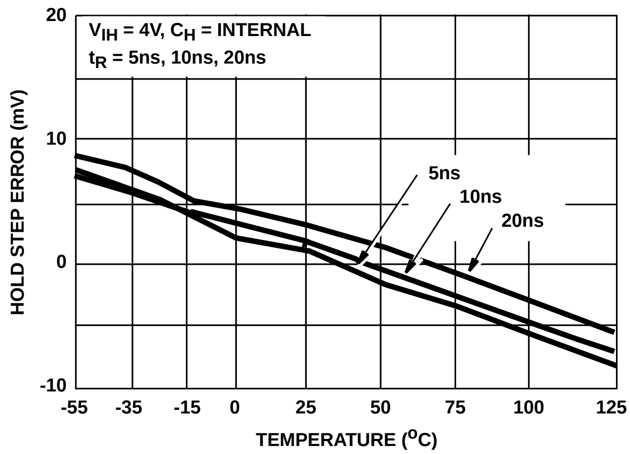
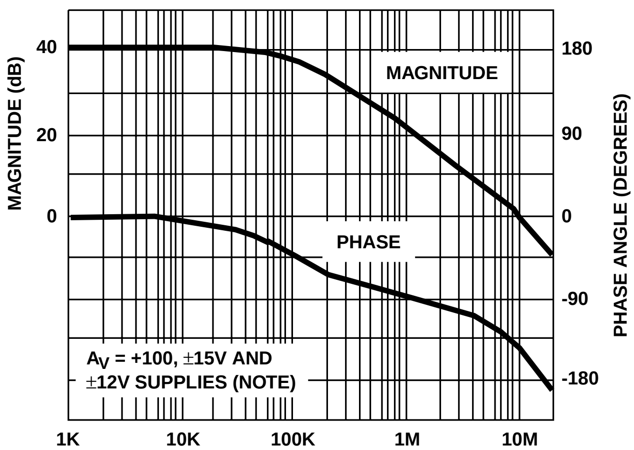


FIGURE 13. HOLD STEP ERROR vs TEMPERATURE



NOTE: ±15V and ±12V supplies trace the same line within the width of the line, therefore only one line is shown.

FIGURE 14. CLOSED LOOP PHASE/GAIN

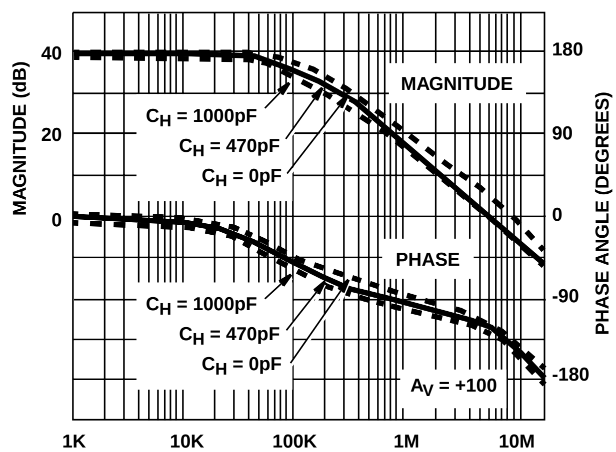


FIGURE 15. CLOSED LOOP PHASE/GAIN

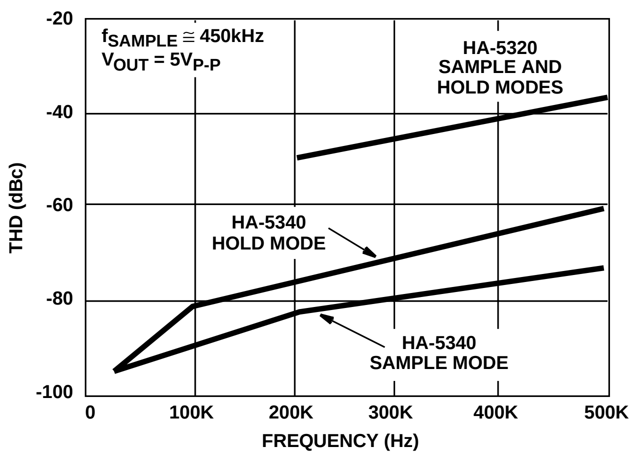


FIGURE 16. THD vs FREQUENCY

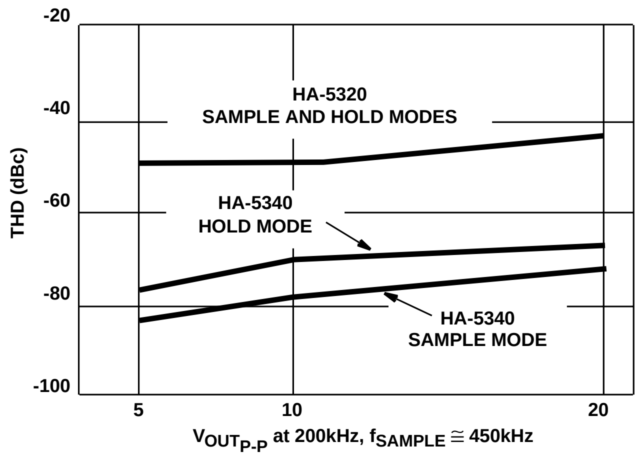


FIGURE 17. THD vs V_{OUT}

Die Characteristics

DIE DIMENSIONS:

84mils x 139mils x 19mils

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos)
Silox Thickness: 12kÅ ± 2.0kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

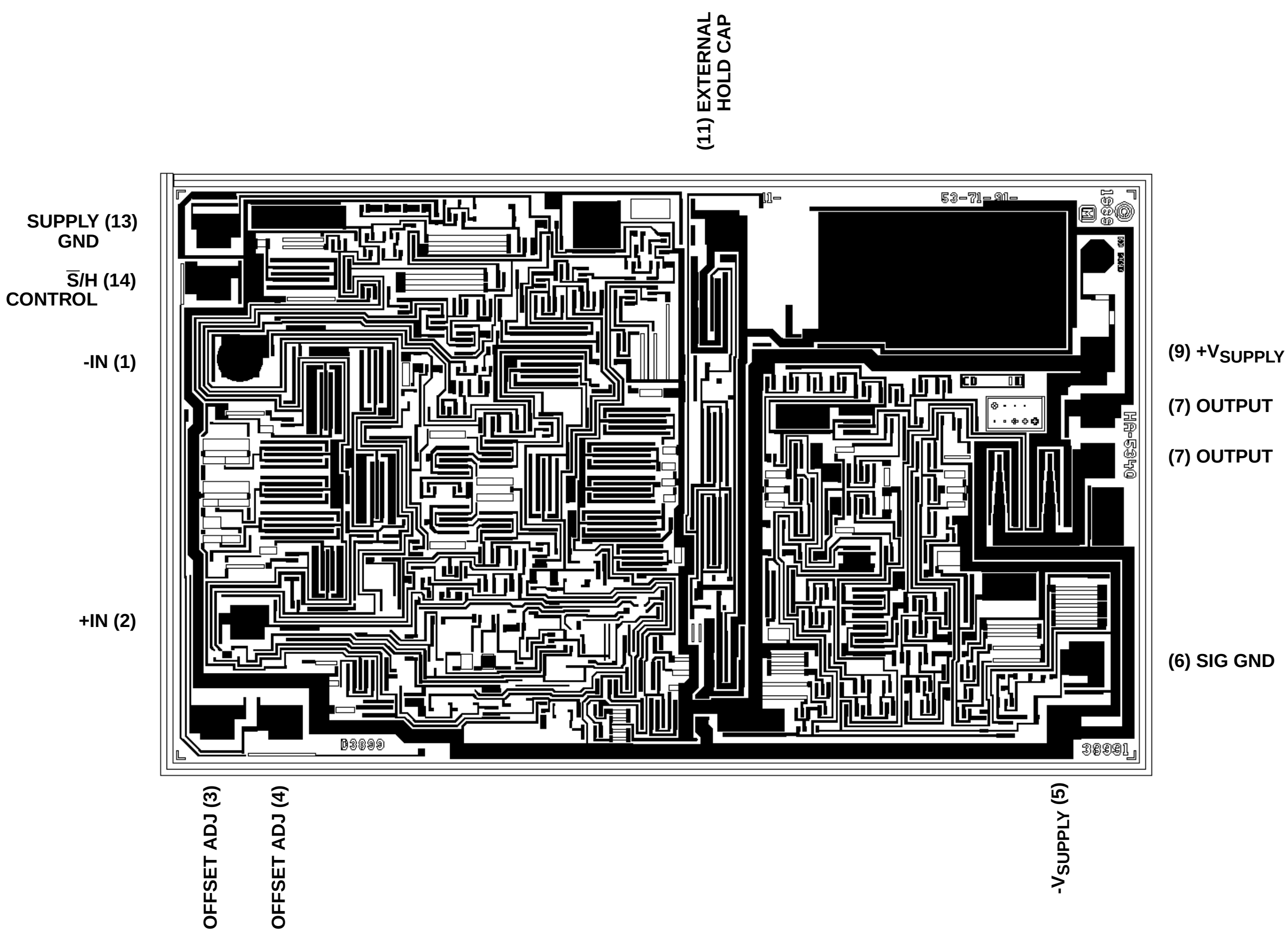
V-

TRANSISTOR COUNT:

196

Metallization Mask Layout

HA-5340



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