élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4331C

Triple 2:1 Mux-Amp AV = 1

Features

- 3 ns A-B switching
- 300 MHz bandwidth
- Power down mode
- TTL/CMOS compatible controls
- Fixed gain of 1
- 400V/µs slew rate

Applications

- RGB multiplexing
- Picture-in-picture
- Cable driving
- HDTV processing
- Switched gain amplifiers
- ADC input multiplexer

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4331CS	-45°C to +85°C	16-Lead SOIC	MDP0027

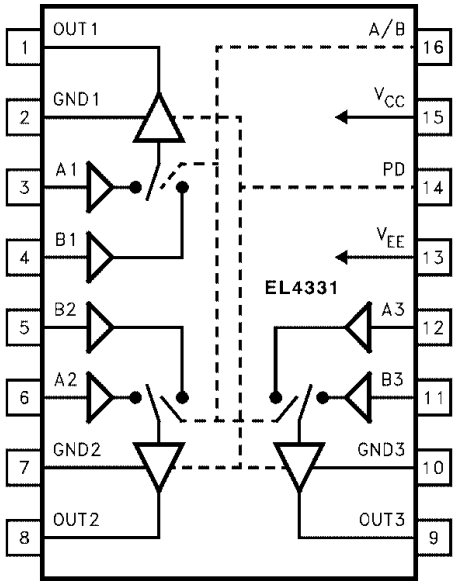
General Description

The EL4331C is a triple, very high speed, 2:1 Multiplexing Amplifier. It is intended primarily for component video multiplexing, and is especially suited for pixel switching. The amplifiers have their gain set to 1, internally. All three amplifiers are switched simultaneously from their A to B inputs by the TTL/CMOS compatible, common A/B control pin.

The EL4331C has a power down mode, in which the total supply current drops to less than 1 mA. In this mode, each output will appear as a high impedance.

The EL4331C runs from standard ±5V supplies, and is available in the narrow 16-pin small outline package.

Connection Diagrams



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EL4331C

Triple 2:1 Mux-Amp AV = 1

Absolute Maximum Ratings (T_A = 25 °C)

V_{CC} to V_{EE}	14V	Input Current, Any Input	5 mA
V_{CC} to Any GND	12V	Power Dissipation	See curves
V_{EE} to Any GND	12V	Operating Temperature	-45°C to +85°C
Continuous Output Current	45 mA	Leading Temperature during Soldering	300°C
Any Input (except P_D)	V_{EE}-0.3V to V_{CC}+0.3V	Junction Temperature	170°C
P_D Input	V_{CC}-7V to V_{CC}+0.3V	Storage Temperature	-60°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefor $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_{CC} = +5V, V_{EE} = -5V, Ambient Temperature =25°C, R_L = 500Ω, P_D = 5V

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Referred Offset Voltage		-12	30	II	mV
dV_{OS}	Input A to Input B Offset Voltage [1]		1	8	II	mV
I_B	Input Bias Current		-7	-30	II	µA
dI_B	Input A to Input B Bias Current [1]		0.5	4.0	II	µA
AV_{OL}	Open Loop Gain (from Gain Error Calculation)		54		V	dB
PSRR	Power Supply Rejection Ratio	60	70		II	dB
V_{OUT}_500	Output Voltage Swing into 500Ω Load	±2.7	±3.2		II	V
V_{OUT}_150	Output Voltage Swing into 150Ω Load		+3/-2.7		V	V
I_{OUT}	Current Output, Measured with 75Ω load [2]	30	40		II	mA
X_{TALK}	Crosstalk from Non-Selected Input (at DC)	-70	-85		II	dB
V_{IH}	Input Logic High Level (A/B and PD)	2.0			II	V
V_{IL}	Input Logic Low Level (A/B and PD)			0.8	II	V
I_{IL_AB}	Logic Low Input Current (V_{IN} = 0.8V), A/B Pin	-1	-20	-100	II	µA
I_{IH_AB}	Logic High Input Current (V_{IN} = 2.0V), A/B Pin	-5	0	5	II	µA
I_{IL_PD}	Logic Low Input Current (V_{IN} = 0.8V), PD Pin	-10	0	10	II	µA
I_{IH_PD}	Logic High Input Current (V_{IN} = 5.0V), PD Pin	0.5	1.0	1.6	II	mA
I_S	Total Supply Current	38	48	60	II	mA
$I_{S(PD)}$	Powered Down Supply Current		0.01	1.0	II	mA

1. Any channel's A-input to its B-input.
2. There is no short circuit protection on any output.

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AC Electrical Characteristics

V_{CC} = +5V, V_{EE} = -0.5V, Ambient Temperature = 25°C, R_L = 150Ω and C_L = 5 pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW	-3 dB Bandwidth		300		V	MHz
	-3 dB BW with 250Ω and 10 pF Load		400		V	MHz
SR	Slew Rate (4V Square Wave, Measured 25%–75%)		400		V	V/µs
T_S	Settling Time to 0.1% of Final Value		13		V	ns
T_{AB}	Time to Switch Inputs		3		V	ns
OS	Overshoot, V_{OUT} = $4V_{pk-pk}$		8		V	%
I_{SO-AB}-10M	Input to Input Isolation at 10 MHz		53		V	dB
I_{SO-AB}-100M	Input to Input Isolation at 100 MHz		33		V	dB
I_{SO-CH}-10M	Channel to Channel Isolation at 10 MHz		56		V	dB
$I_{SO-CH-CH}$-100M	Channel to Channel Isolation at 100 MHz		33		V	dB
Pkg	Peaking with Nominal Load		0		V	dB
T_{ON_PD}	Power Down Turn-On Time		150		V	ns
T_{OFF_PD}	Power Down Turn-Off Time		1		V	µs

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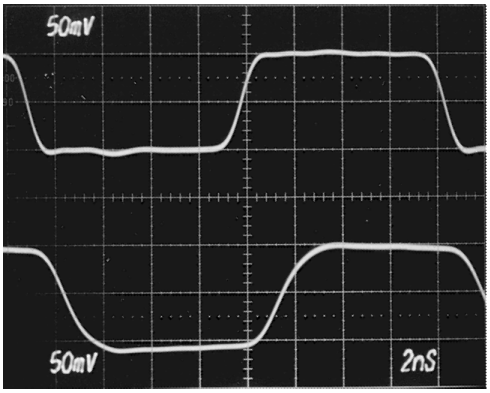
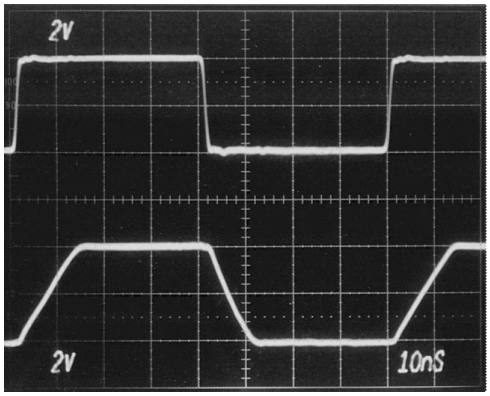
Triple 2:1 Mux-Amp AV = 1

Typical Performance Curves

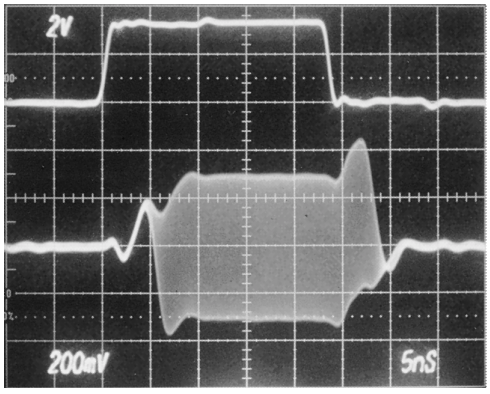
3 dB Bandwidth Small Signal Transmit Response



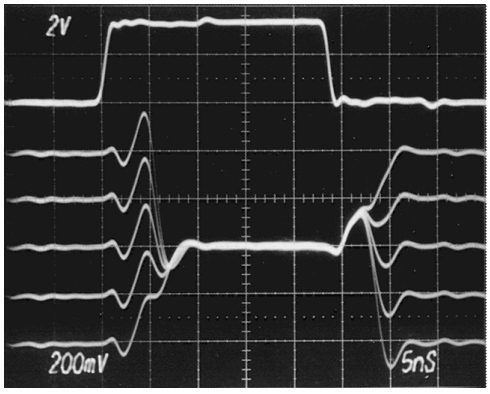
Large Signal Transient Response



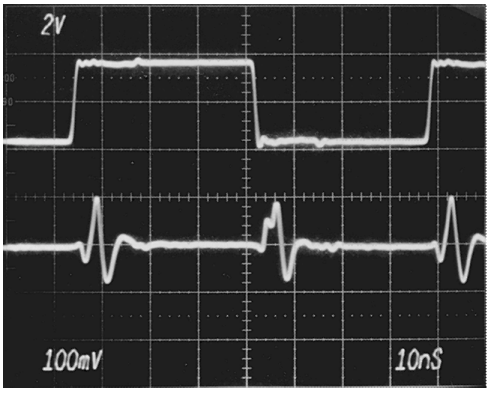
Switching from Ground to An Uncorrelated Sine Wave and Back



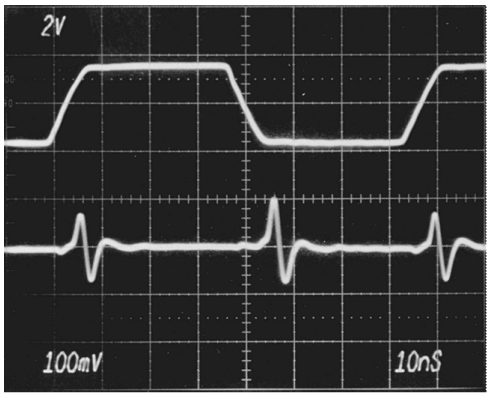
Switching a Family of DC Levels to Ground and Back



Switching Glitch, 0V to 0V with 2 ns AB edges



Switching Glitch, 0V to 0V with 10 ns AB Edges



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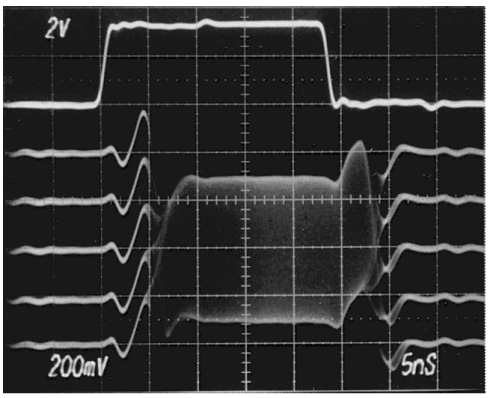
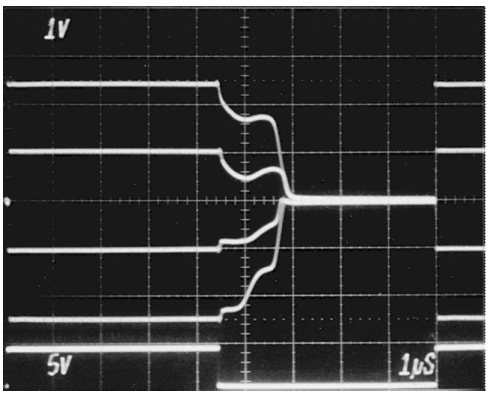
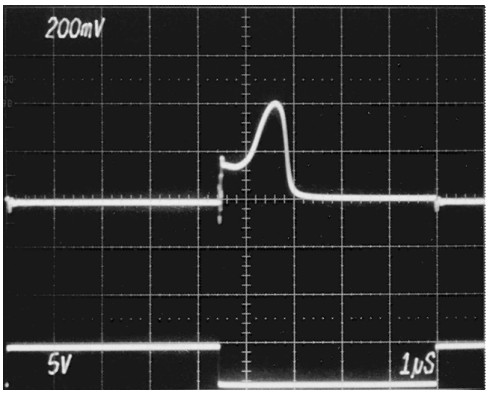
Switching a Family of DC Levels to a Sine Wave and BackV



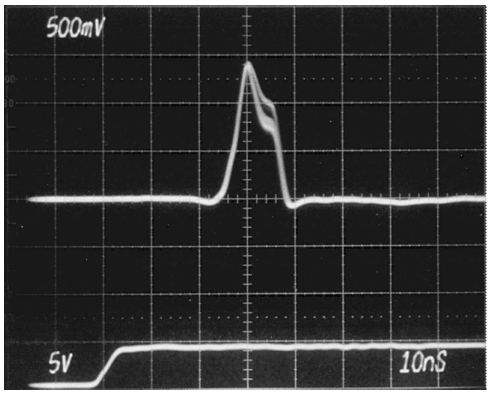
Output Response In and Out of Power Down with a Family of DC Inputs



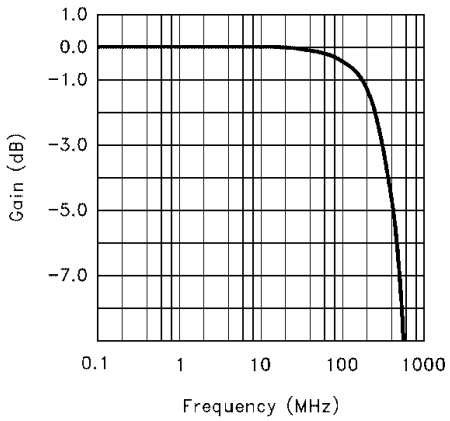
Output Power Down Turn-Off Response



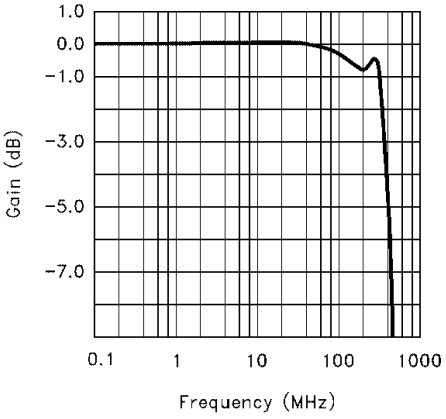
Output Power Down Turn-On Response



Frequency Response with 150Ω and 5 pF Load



Frequency Response with 240Ω and 5 pF Load



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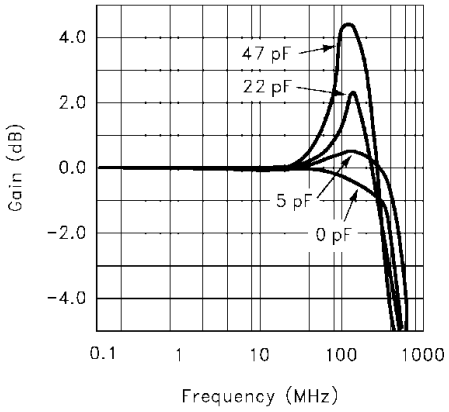
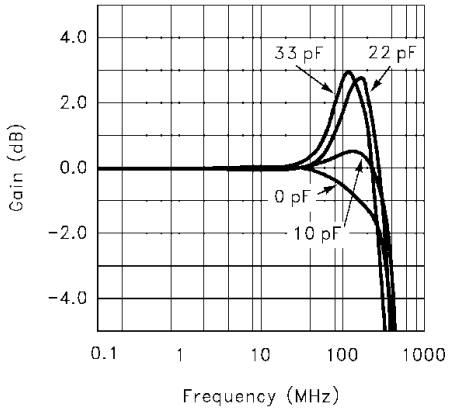
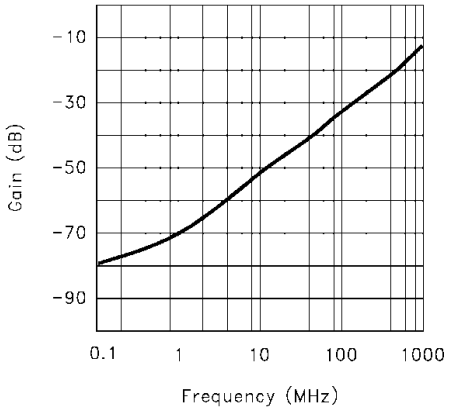
Frequency Response with 150Ω and Various Values of Capacitive Load



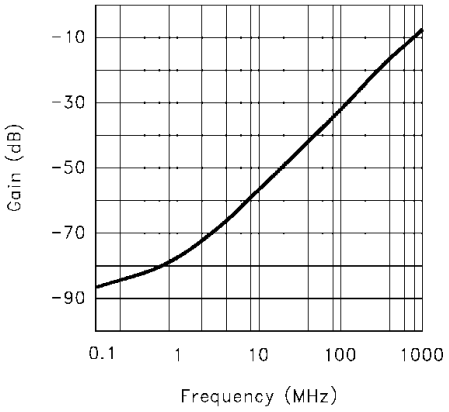
Frequency Response with 240Ω and Various Values of Capacitive Load



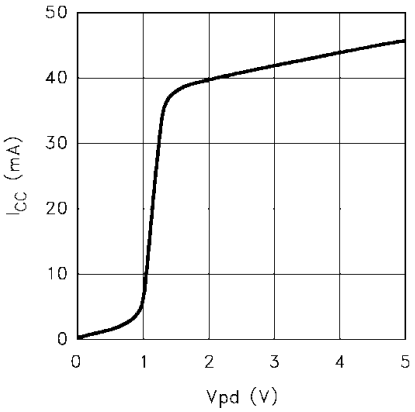
A-Input to B-Input Isolation



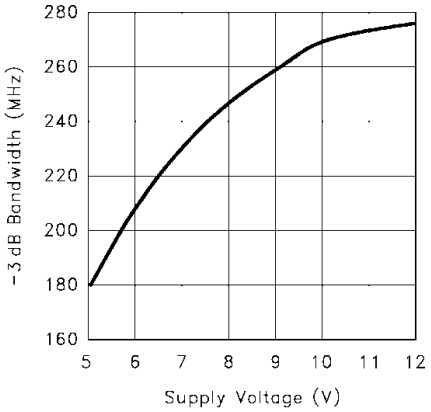
Channel to Channel Isolation



Supply Current vs Power Down Voltage



-3 dB BW vs Supply Voltage



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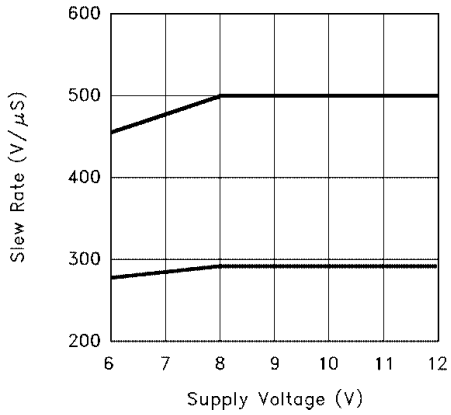
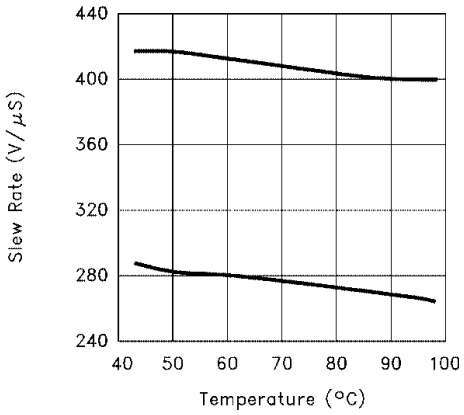
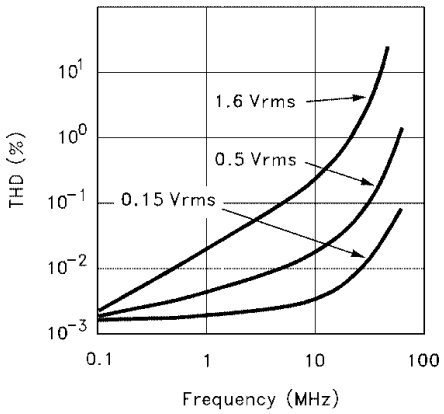
Slew Rate vs Supply Voltage



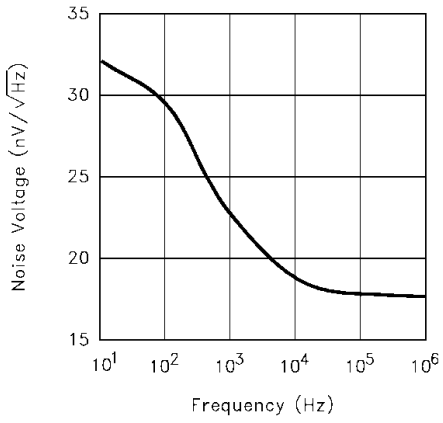
Slew Rate vs Temperature



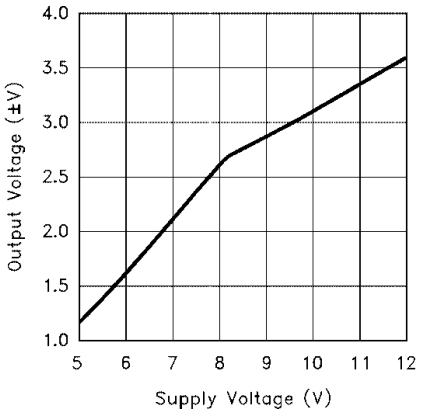
Total Harmonic Distortion



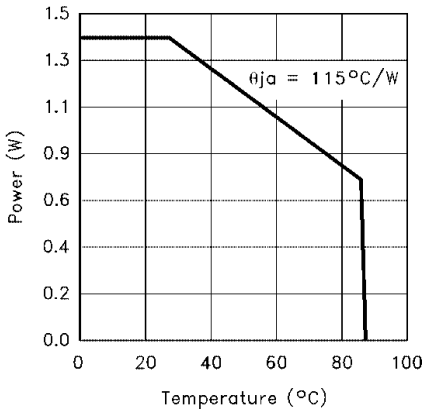
Voltage Noise Spectral Density



Output Voltage Swing vs Supply Voltage



Maximum Power Dissipation



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Applications Information

Pin Descriptions

A1, A2, A3	"A" inputs to amplifiers 1, 2 and 3 respectively
B1, B2, B3	"B" inputs to amplifiers 1, 2 and 3 respectively
GND1, GND2, GND3	These are the individual ground pins for each channel.
OUT1, OUT2, OUT3	Amplifier outputs. Note there is no short circuit protection.
V_{CC}	Positive power supply. Typically +5V.
V_{EE}	Negative power supply, typically -5V.
A/B	Common input select pin, a logic high selects the "A" inputs, logic low selects the "B" inputs. If left to float, this pin will float high and the "A" channels will be selected.
PD	A logic low puts the part into its power down mode. Note that when this pin is at a logic high (+5V), it will sink typically 1 mA. When pulled low, it will source a few µA, typically < 25 µA. This pin should not be left floating.

Circuit Operation

Each multiplexing amplifier has two input stages. The multiplexing amplifiers switch from their "A" inputs to their "B" inputs under control of the common **A/B** select pin. The switching has a make before break action. Each amplifier is internally connected for unity gain, allowing larger switching matrixes to be built up. Note however, that each amplifier likes to see a load of 250Ω or less; load resistances higher than this, can lead to excessive peaking. Load capacitance should be kept down below 40 pF, and 40 pF requires a load resistance of ð 150Ω to keep the output from excessive peaking. Higher capacitive loads can best be driven using a series resistor to isolate the amplifier from the reactive load.

The ground pins are used as a reference for the logic controls. Both **A/B** and **PD** are referenced to ground. The supplies do not have to be symmetrical around ground, but the logic inputs are referred to the ground pins, and the logic swing must not exceed the +V supply. Due to the fact that all three channels share common control pins, the three grounds **have** to be at the same potential. One third of the 1 mA that **PD** will sink (at 5V) will be seen at each ground pin. Also, the individual grounds are internally connected to their channel compensation capacitor in an effort to keep crosstalk low.

A/B Switching

Referring to the photographs showing the 0V–0V switching glitches, it will be noted that slower edges on the A/B control pin result in switching glitches of somewhat less total energy. The switching action is a make-before-break, so the two inputs essentially get mixed at the output for a few nanoseconds. Note that the two inputs are buffered, so there is no component of one input injected into the other input. The input impedance does not depend on whether an input has been selected.

Power Down

Referring to the photographs of the power down function and Figure 4, it will be noted that there is a considerable glitch in the output as the part powers down. It will also be noted that the power down time is considerably longer than power up, 1 µs compared to 150 ns. In power down mode, the whole amplifier, its reference and bias lines are all powered down. At the same time, the output stage has been configured so that the powered down output appears as a high impedance. This allows circuits such as the multiplexer shown in application #4 to be realized, although the price is the

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significant output disturbance as one part turns on before the other has fully turned off.

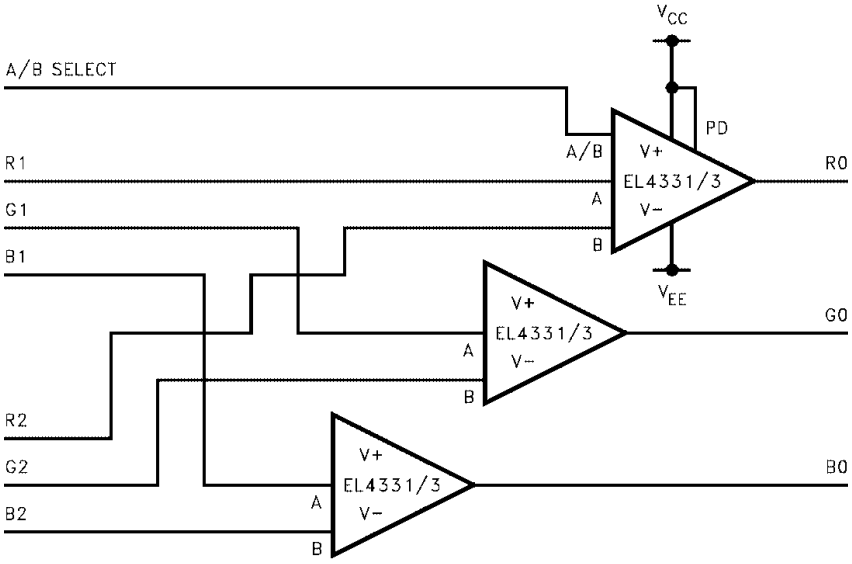

Figure 1. Two RGB Sources Multiplexed to One RGB Output

Single Supply Operation

Due to the fact that video signals often have negative sync levels and invariably require ground to be within the signal swing, running the EL4331 on a single supply rail compromises many aspects of its performance. It is difficult to generate a solid, clean, pseudo ground a few volts away from ground without using more power, and components than simply providing a negative power rail. A signal ground has to be capable of handling all the return currents from all the inputs, as well as the outputs, from DC to frequencies in excess of 400 MHz. While this is by no means impossible, a negative rail can be generated from a standard +5V rail for a couple of dollars and a square inch, or less, of board space. However, a pseudo ground can be derived with for example an LM336, to give an “AC ground” 2.5V above 0V. The logic inputs will need some form of level shifting to ensure that the logic “1” and “0” specifications can be met. The pseudo ground must be well bypassed to the real ground; note that the pseudo ground will have to sink/source all the current that flows in the internal compensation capacitors during slewing. This can easily be several milliamps in a few nanoseconds. If the pseudo ground “moves” because one channel is forcing current into the derived ground, cross-talk into the other two channels will become very significant.

Application Circuit #1

Figure 1 shows a very high speed RGB (or YUV) multiplexer. Two video sources can be displayed on one monitor with the only stipulation that the video sources have to be synchronous. An example is a picture-in-picture, or “window” is generated with one video source (e.g. RGB TV) in a window, and a computer application around it. Multiplexing synchronous RGB signals has the advantage that the video signals do not have to be digitized, and an image stored in RAM prior to being displayed.

When the monitor is switched off, or goes into its power-saving blanked mode, the EL4331 can be powered down to further save power. The input impedance does not change appreciably between powered up and down modes, although the bias current does drop to near zero.

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A demonstration board with this circuit on it is available from Elantec.

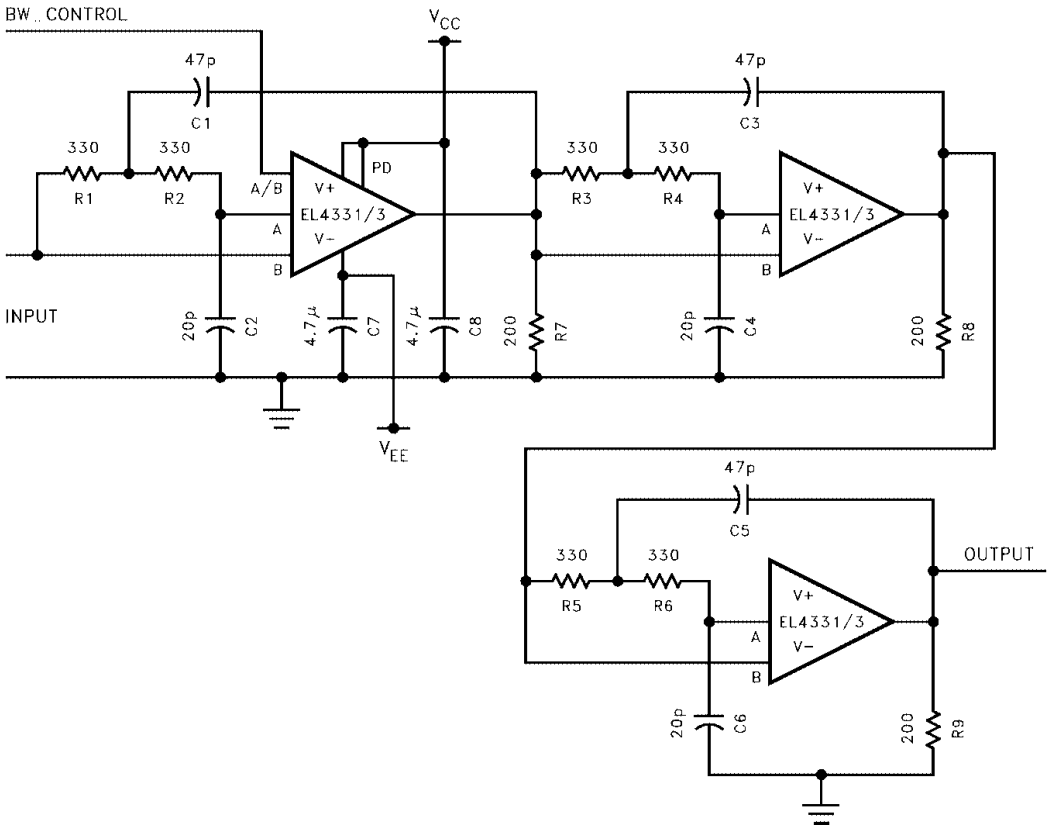

Figure 2. A Bandwidth-Selectable Filter

Application Circuit #2

Figure 2 shows a circuit that has either a very wide bandwidth, or an 11 MHz low pass response. The EL4331's "A" inputs are connected to the one frequency determining set of components, while the "B" inputs are connected directly. The A/B select pin therefore selects the desired bandwidth. This would allow appropriate filtering to clean up noisy low bandwidth video signals when displaying them on a high quality wide bandwidth monitor.

Application Circuit #3

Figure 3 shows one of the three channels of a component video, 8:1 multiplexer. The A/B select pins naturally allow binary coded addressing—allowing simple microprocessor or state machine control. Note that each amplifier output is loaded, to keep the amplifier outputs damped.

Photograph A1 shows a staircase generated by having all the inputs (sig0 through sig7) connected to a resistive divider chain, and the select bits were driven by a binary counter. Photograph A2 shows the glitch between steps 4 and 5; this is the worst glitch since all three banks of EL4331s are switching together. The magnitude of this glitch is affected by the timing skew of the select lines, the physical length of the traces, and the difference in amplitude of the two signals. This particular circuit was bread-boarded using EL4331s on their adapter boards (available from Elantec for those who can not bread-board with SOICs), and the binary counter was an 'LS163.

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Applications Information

High Speed 8-to-1 Multiplexer

Note: No supply bypass capacitors shown and only one of three channels shown.

Channel Selection Table

BIT2BIT1BIT0OUTPUT

000SIG0

001SIG1

010SIG2

011SIG3

100SIG4

101SIG5

110SIG6

111SIG7

Figure 3. A High Speed, 8:1 Component Video Multiplexer

Photograph A3 shows the same circuit, with the counter running at 25 MHz. This turns out to be close to the limit of the TTL counter used in the breadboard, rather than the limit of the EL4331. Here the different glitches are easily recognizable—a small glitch for one of the 4 input

EL4331s A/B switching, somewhat larger glitches when two banks switch together, and the biggest glitch when all three banks switch. Photograph A4 shows the big glitch in detail. A good PCB and equal length and matched traces would clean up these glitches.

433129

A1

433130

A2

433131

A3

433132

A4

8-to-1 Multiplexer using Power Down

Note: No supply bypass capacitors shown. Only one of three channels shown.

Channel Selection Table

BIT2BIT1BIT0OUTPUT

000SIG0

001SIG1

010SIG2

011SIG3

100SIG4

101SIG5

110SIG6

111SIG7

Figure 4. A Simple 8:1 Component Video Multiplexer

Figure 4 shows one of the three channels of a component video, 8:1 multiplexer. In this example, the power down capability is used to save on EL4331s, but as can be seen, the control part does become more complicated. Using the power down mode for multiplexing does, of course, slow down the speed with which one can select a given input channel. However, if input channel selection can be done during a blanking period, the couple of microseconds that it takes to power down one

chip may be no problem. Note that some external logic is needed in this application, both to select the appropriate amplifier, and also to force a break-before-make action by pulling the T_OFF line low. All this logic would best be incorporated inside a PAL or gate array, and is shown in gate form just to illustrate the idea. Note that the BIT0 line would have the 3 ns response time, since it is switching the muxamps directly.

Photograph B1 shows a staircase generated by having all the inputs (sig0 through sig7) connected to a resistive divider chain, and then the select bits and the PD pins were driven by a binary counter and a 2-line to 1 of 4 decoder. Photograph B2 shows the glitch between steps 4 and 5; this glitch is caused by the fact that the amplifier that has just been powered up momentarily fights the amplifier that has been powered down, but is not yet off. As seen in the photograph, this causes a glitch of about 200 ns duration. However, when the A/B select pin changes inputs, the glitches are much smaller, as shown in photograph B3. Photograph B4 shows the +2.5V to

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-2.5V transition. This is another PD caused glitch, similar to the step 4 to step 5 glitch, but with a much increased magnitude—which causes significantly more fighting between the output stages.

Despite the glitches, if the PD switching can be done during signal blanking, and only A/B switching is used during the picture, this simple multiplexer has significant parts savings and power savings when compared to the high performance multiplexer in the previous application note.

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EL4331C

Triple 2:1 Mux-Amp AV = 1

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