

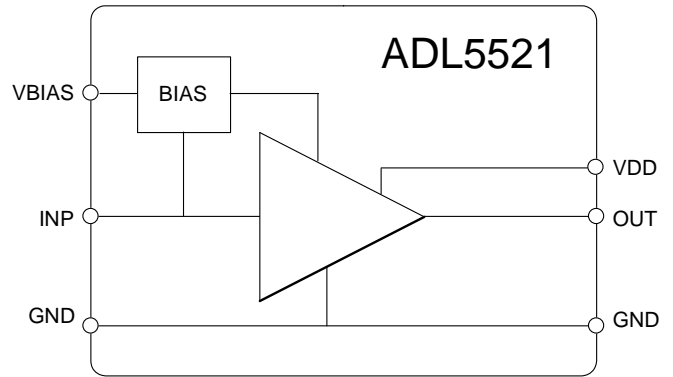
FEATURES

Gain of 15.3dB at 1950MHz
Matched 50-Ω input and output
Noise Figure of 0.8dB at 1950MHz
OIP3 of 35.3dBm typ at 1950MHz
Single 5V Supply Operation
Operating current of 65ma at +5V
LFCSP 3x3 mm Package

GENERAL DESCRIPTION

The ADL5521 is a high performance GaAs pHEMT low-noise amplifier. It provides high gain and low noise figure for single down-conversion IF sampling receiver architectures as well as direct down conversion receivers.

The ADL5521 amplifier comes in a compact, thermally enhanced 3x3mm LFCSP package and operates over the temperature range of -40°C to $+85^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAM*Figure 1.***Rev. PrA**

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703 © 2003 Analog Devices, Inc. All rights reserved.

SPECIFICATIONS

$V_s = 5\text{ V}$, $T = 25^\circ\text{C}$, $f_c = 1950\text{MHz}$

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
Input return loss	External match		12		dB
Output return loss	External match		20.7		dB
Gain			15.3		dB
Gain Flatness	In the [1920 – 1980] frequency band		0.015		dB/MHz
Gain vs. Temperature	In the [1920 – 1980] frequency band		0.018		dB/degC
Noise Figure			0.8		dB
Output IP3			35.3		dBm
Output 1 dB Compression Point			22.5		dBm
S12 Isolation			21.4		dB
POWER-INTERFACE					
Supply Voltage		4.5	5	5.5	V
Current Consumption			65	TBD	mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
Max RF Input Level	TBD
Internal Power Dissipation	TBD mW
θ_{JA} (Exposed paddle soldered down)	TBD mW
θ_{JA} (Exposed paddle not soldered down)	TBD°C/W
θ_{JC} (At exposed paddle)	TBD°C/W
Maximum Junction Temperature	TBD°C/W
Operating Temperature Range	TBD°C
Storage Temperature Range	-40°C to +85°C
Lead Temperature Range (Soldering 60 sec)	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

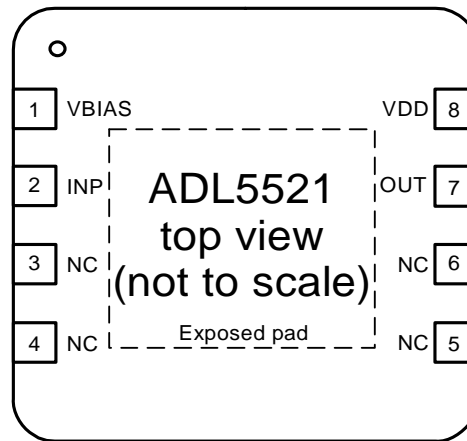


Figure 2. 8-Lead LFCSP

Table 3. Pin Function Descriptions- 8Lead CSP

Pin No.	Mnemonic	Description
1	VBIAS	Bias: Internal DC bias
2	INP	RF Input: Must be AC-coupled.
3,4,5,6	NC	NC: No internal connection
7	OUT	RF Output: Must be AC-coupled.
8	VDD	Supply: VDD bias needs to be bypassed to ground using low-inductance capacitors.
Exposed pad	EP	Exposed Paddle: Connect to a low impedance ground plane

TYPICAL PERFORMANCE CHARACTERISTICS

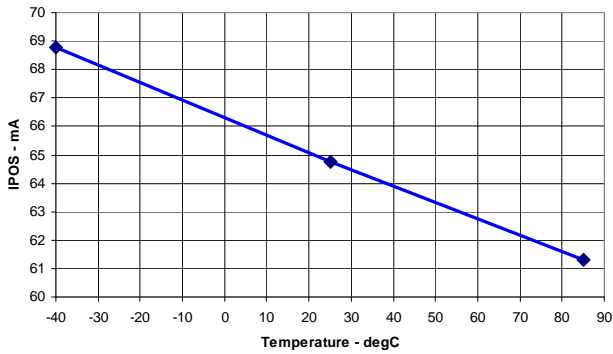


Figure 3. ADL5521 Current vs. Temperature

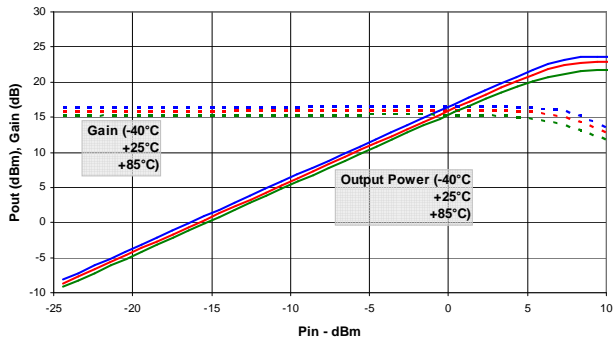


Figure 4. Output Power and Gain vs. Temperature

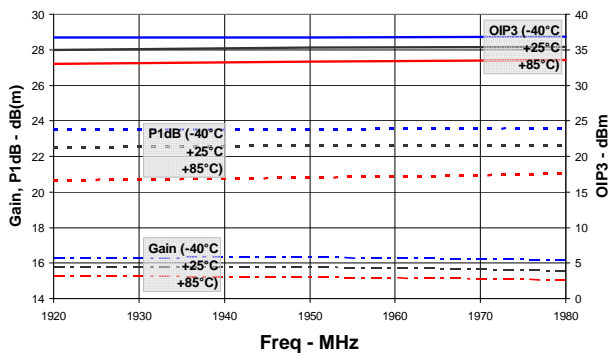


Figure 5 Gain, P1dB, OIP3 vs. Frequency

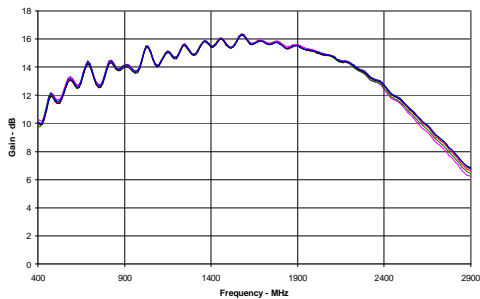


Figure 6. Gain vs. Frequency, Complete Frequency Range, 5 Parts

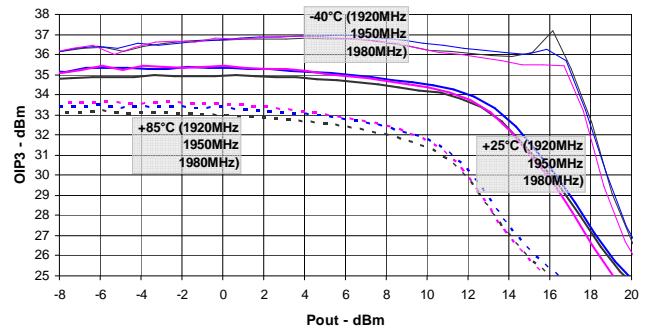


Figure 7. OIP3 vs. Output Power, Temperature and Frequency

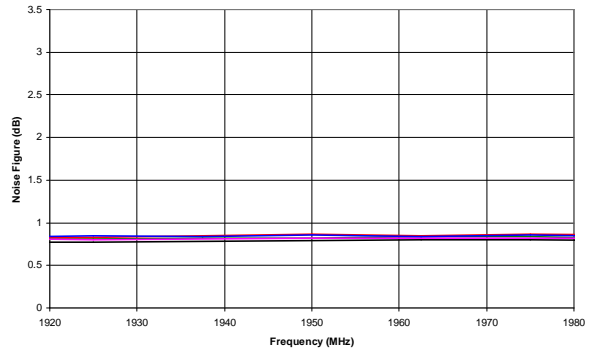


Figure 8. Distribution of Noise Figure for Five Parts, 1920 to 1980 MHz

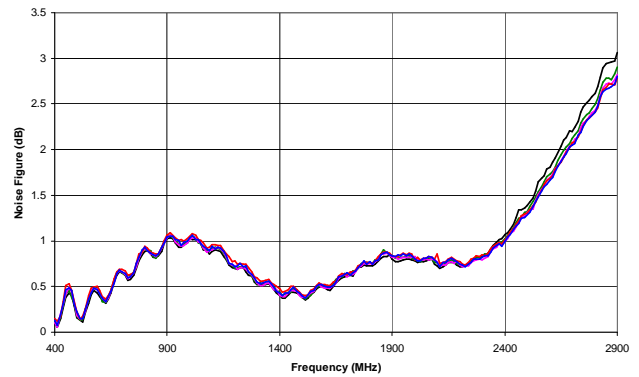


Figure 9. Distribution of Noise Figure for Five Parts, Complete Frequency Range

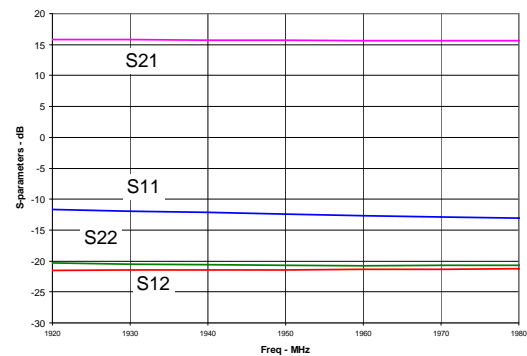


Figure 10. Typical S Parameters, 1920 to 1980 MHz

OUTLINE DIMENSIONS

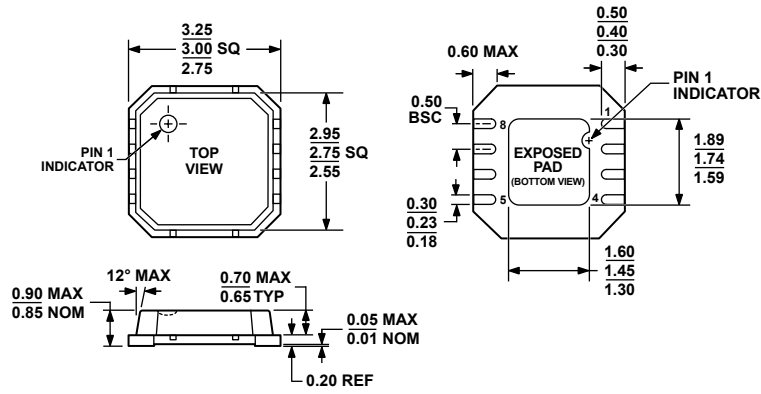


Figure 11. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
 3mm × 3 mm Body, Very Thin, Dual Lead
 CP-8-2
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADL5521ACPZ-R7 ¹	-40°C to +85°C	7" Tape and Reel	CP-8-2
ADL5521ACPZ-WP ¹	-40°C to +85°C	Waffle Pack	CP-8-2
ADL5521-EVALZ		Evaluation Board	

¹ Z = Pb free part