

# SIEMENS

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**SAT-IF-Demodulator**

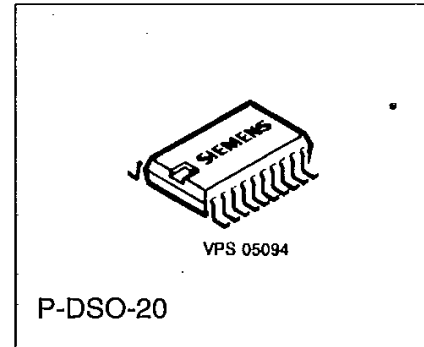
**TDA 6142X**

**Preliminary Data**

**Bipolar IC**

**Features**

- Good C/N response through high input sensitivity
- Reduced noise bandwidth of prescaler at 480MHz through LC circuit
- Limiting of internal bandwidth of prescaler at 960 MHz
- Improved stability against oscillation through LC circuit
- High frequencies are damped and interference is reduced by LC circuit
- Enhanced AFC circuit with good thermal stability
- Integrated input selector for dual SAW filter



Type	Ordering Code	Package
TDA 6142X	Q6700-A5046	P-DSO-20 (SMD)

Amplifier and IF demodulator for satellite applications, consisting of: four-stage limiter amplifier with selectivity circuit and selector switch for two IF-inputs, each with a base stage; divider by 4; video amplifier; automatic gain control; AFC-output with adjustable rate of rise; polarity switchover of video signal.

**Application**

In satellite receiving systems.

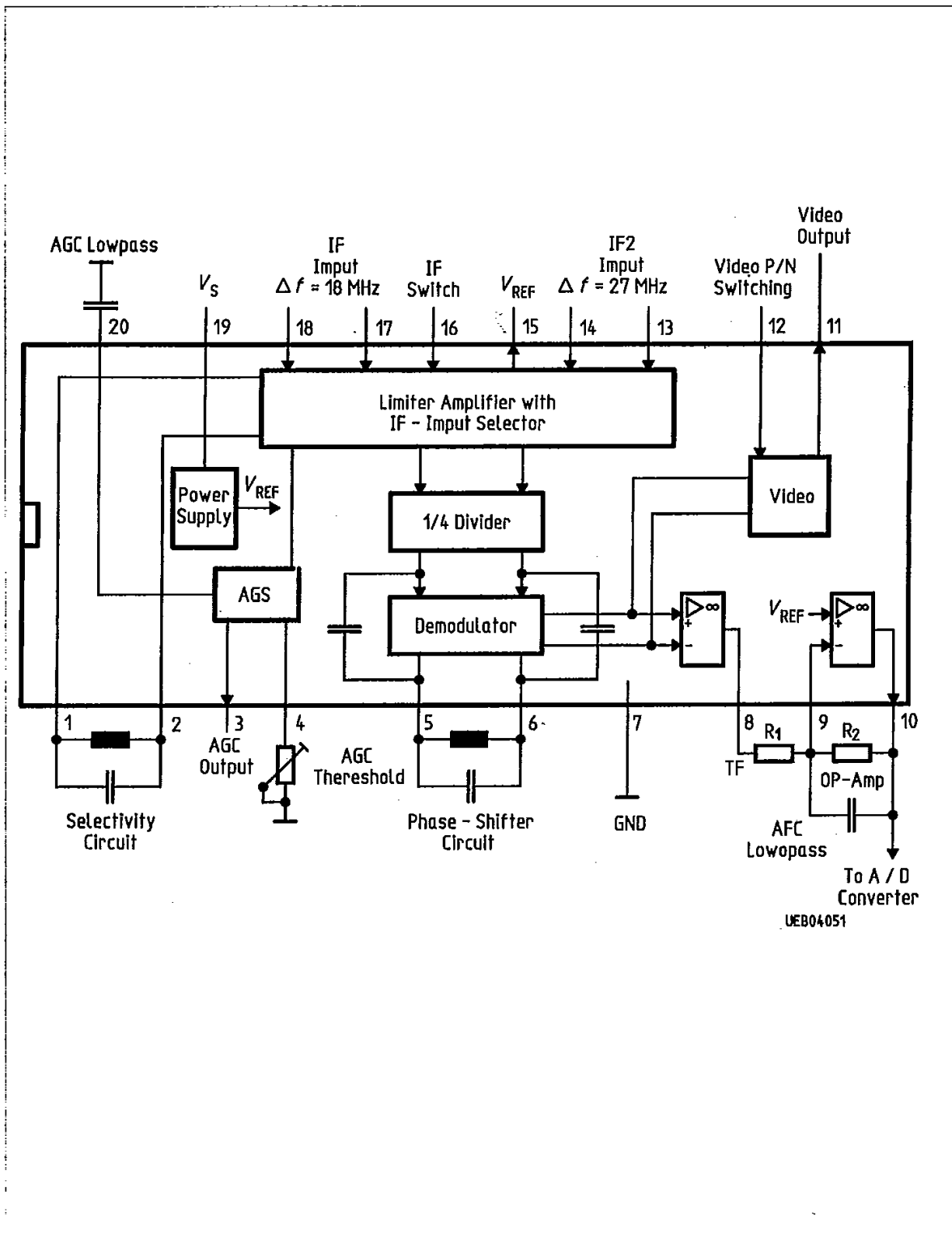
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**Pin Definitions and Functions**

Pin No.	Function
1	Connection of parallel-resonant circuit
2	Connection of parallel-resonant circuit
3	AGC-voltage output
4	Setting of AGC threshold
5	Connection of resonant circuit for demodulator
6	Connection of resonant circuit for demodulator
7	Ground
8	AFC-preamplifier output
9	AFC-lowpass filter and feedback point for AFC-sensitivity setting
10	AFC-output to A/D-converter and AFC-lowpass filter
11	Video output
12	Video polarity switching, positive/negative
13	IF-reference input 2
14	IF-input 2, eg $\Delta f = 27$ MHz
15	Reference voltage output
16	IF-input selector for IF-input 1 or 2
17	IF-reference input 1
18	IF-input 1, eg $\Delta f = 18$ MHz
19	Supply voltage 5 V
20	AGC-lowpass filter



UEB04051

Block Diagram

**Circuit Description**

The frequency-modulated satellite IF-signal is applied by way of a SAW-filter - with two balanced outputs and different bandwidth - to the two low-impedance, balanced inputs of the limiter amplifier. One IF-input at a time can be through-connected by applying an external DC-voltage to the IF-input selector. Unbalanced operation is also possible by appropriate RF blocking of the balanced inputs, but this entails higher noise levels. An external selectivity circuit in the penultimate amplifier stage produces good selectivity in the limiter amplifier and consequently better harmonics suppression.

The output signal from this amplifier is fed to a divider, which divides the frequency by 4. Following this the signal is applied once direct and once with phase shift - produced by an external phase-shifter circuit - to a quadrature demodulator.

The demodulated video signal is amplified and appears at the video output. The polarity of this demodulated video signal can be inverted by applying an external DC-voltage to the polarity-switching input.

Parallel to this, the demodulated video signal is used for automatic frequency control (AFC). Here it is fed via a preamplifier to an inverting operational amplifier with an internal reference voltage. Any frequency offset that is present will show itself in the form of a changing DC voltage, which can be applied to an external A/D-converter. The rate of rise of the AFC and thus the gain of the operational amplifier can be set externally by a resistor network.

The information for the field strength of the frequency-modulated satellite IF-signal appears both as a DC-voltage at the AGC-output and on the AGC-lowpass filter. The AGC-threshold can be varied with a potentiometer. The IF stage of the satellite tuner (TUA 2008X) or an input stage can be controlled in gain by way of the AGC-output.

## Absolute Maximum Ratings

 $T_A = 0$  to  $70\text{ }^\circ\text{C}$ 

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	0	6	V	
Selectivity circuit	$V_{1,2}$	0	6	V	
AGC-output voltage	$V_3$	1	13	V	Open collector
AGC-threshold input	$V_4$	0.3	2	V	
Resonant-circuit inputs	$V_{5,6}$	-0.3	3	V	
Video P/N-switching	$V_6$	-0.3	6	V	
AFC-amplifier	$V_8$	0	6	V	
AFC-lowpass filter	$V_9$	0	5	V	
AFC-output	$V_{10}$	0	5	V	
Video output	$V_{11}$	1	5	V	
Video P/N-switching	$V_{12}$	-0.3	6	V	
IF-inputs	$V_{13, 14, 17, 18}$	0.3	3	V	
Reference voltage	$V_{15}$	0.3	5	V	
IF-input selector	$V_{16}$	0.3	5	V	
AGC-lowpass filter	$V_{20}$	-0.3	5	V	
Junction temperature	$T_J$		150	$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-40	125	$^\circ\text{C}$	
Thermal resistance system-air	$R_{thSA}$		125	K/W	
Surge strength for all pins <sup>1)</sup>	$V_{ESD}$	-2000	2000	V	<sup>2)</sup>

## Operating Range

Supply voltage	$V_S$	4.5	5.5	V
Input frequency range	$f_{15}$	300	700	MHz
Ambient temperature	$T_A$	0	70	$^\circ\text{C}$

1) Single discharge of 100-pF capacitor across series resistor of 1.5 k $\Omega$  in turn on each pin (MIL-STD)

2) Float pins not required; pin 7 always ground

**Characteristics**

$T_A = 25\text{ }^\circ\text{C}; V_S = 5\text{ V} \pm 10\%$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current drain	$I_S$	40	50	60	mA	

**Input Sensitivity**

IF input	$a_{IFin}$	-65		3	dBm	$f_{13, 14 \& 17, 18} = 480\text{ MHz}$
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**IF-Input Switching**

IF-input 1	$V_{16}$	3.2		5	V	
IF-input 2	$V_{16}$	0		2.8	V	

**Video Output**

Video voltage ( $\Delta f = 13.5\text{ MHz}$ )	$V_{11}$	400		800	mV	
Distortion factor	$THD$		< 1		%	
Signal/noise ratio	$S/N$		70		dB	

**Video P/N-Switching**

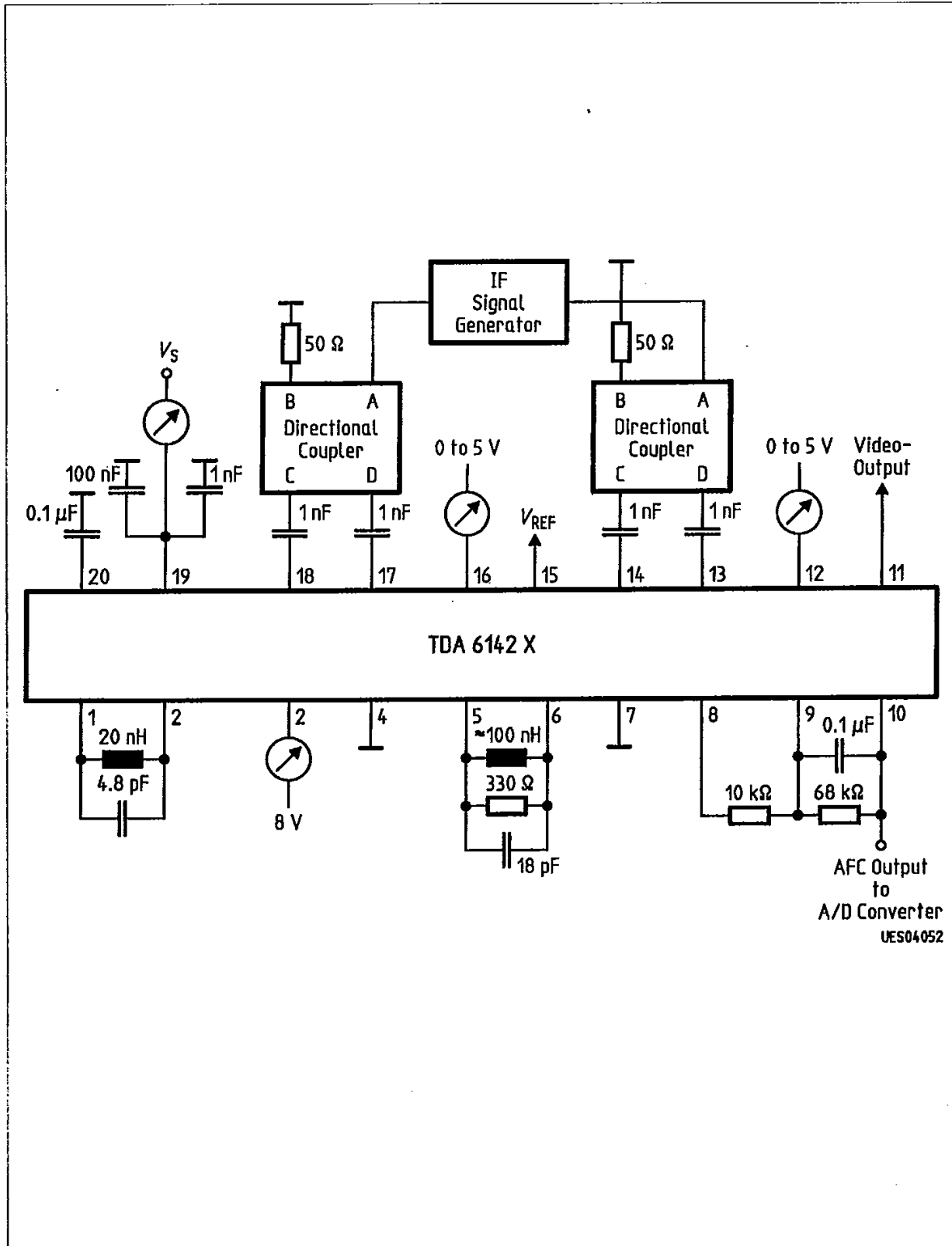
Positive polarity	$V_{12}$	3.5			V	
Input current	$I_{12H}$			50	$\mu\text{A}$	
Negative polarity	$V_{12}$			1	V	
Input current	$I_{12L}$			-50	$\mu\text{A}$	

**AGC-Current (Open-collector current limited)**

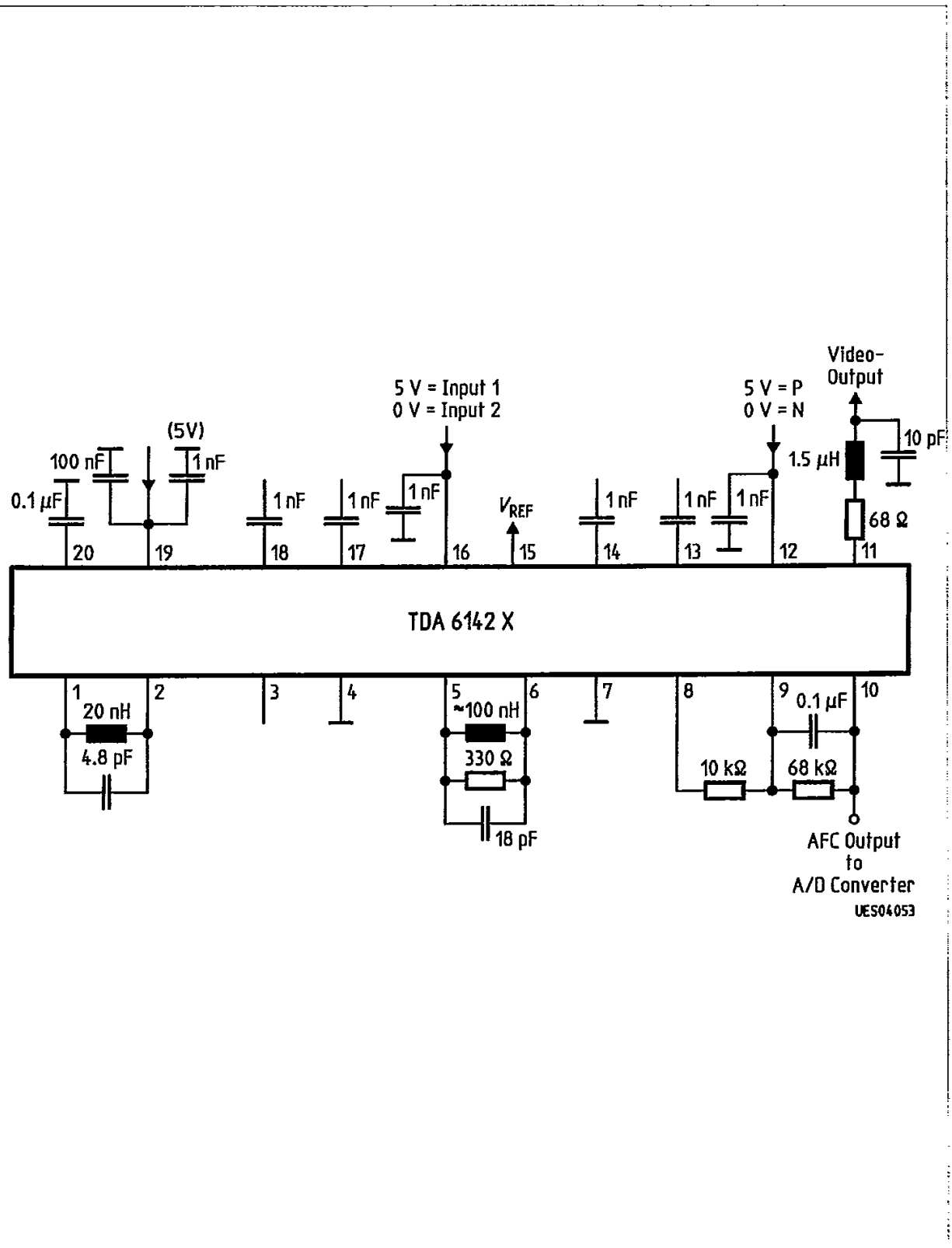
$a_{IFin} = +3\text{ dBm}$	$I_3$		500		$\mu\text{A}$	$V_3 = 8\text{ V}; R_{AGC} = 0$
$a_{IFin} = -3\text{ dBm}$	$I_3$		10		$\mu\text{A}$	$V_3 = 8\text{ V}; R_{AGC} = 0$
$a_{IFin} = -24\text{ dBm}$	$I_3$		500		$\mu\text{A}$	$V_3 = 8\text{ V}; R_{AGC} = \infty$
$a_{IFin} = -30\text{ dBm}$	$I_3$		10		$\mu\text{A}$	$V_3 = 8\text{ V}; R_{AGC} = \infty$

**AFC-Voltage (Open-collector current limited)**

$f_{IFin} = 380\text{ MHz}$	$V_{10}$	$V_S$			V	$R_2/R_1 = 7$
$f_{IFin} = 580\text{ MHz}$	$V_{10}$	-0.5		0.5	V	$R_2/R_1 = 7$



Test Circuit 1



**Application Circuit**



Diagram 1

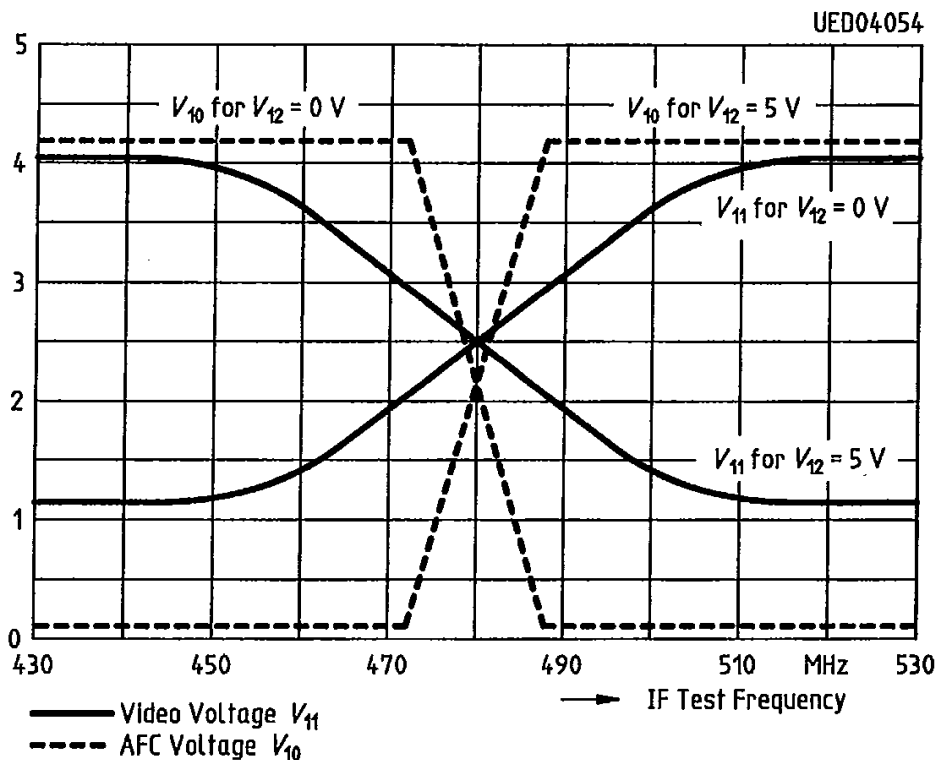


Diagram 2

