Ultra-Low Distortion Differential ADC Driver

Preliminary Technical Data

ADA4938-1

FEATURES

Extremely low harmonic distortion
- −108 dBc HD2 @ 10 MHz
- −79 dBc HD2 @ 70 MHz
- −125 dBc HD3 @ 10 MHz
- −87 dBc HD3 @ 70 MHz

Low input voltage noise: 2.2 nV/√Hz

High speed
- −3 dB bandwidth of 1.5 GHz, G = 1
- Slew rate: 4700 V/μs
- 0.1 dB gain flatness to 125 MHz
- Fast settling to 0.01% in 8.5 ns
- Fast overdrive recovery of 4 ns

1 mV typical offset voltage

Externally adjustable gain

Differential to differential or single-ended to differential operation

Adjustable output common-mode voltage

Wide Supply Voltage Range: +5 V & ± 5 V

Pb-free 3 mm x 3 mm LFCSP package

FUNCTIONAL BLOCK DIAGRAM

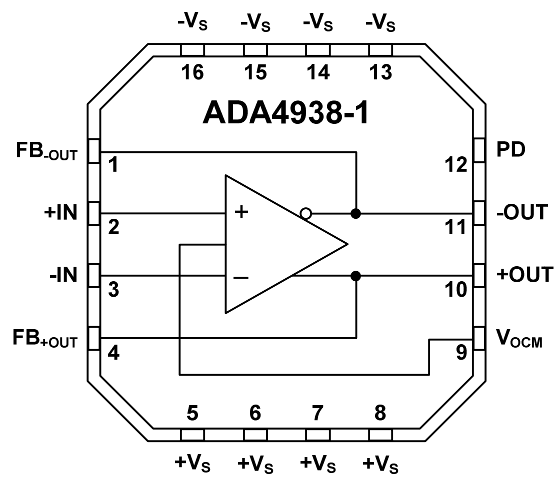

Figure 1.

APPLICATIONS

ADC drivers
Single-ended-to-differential converters
IF and baseband gain blocks
Differential buffers
Line drivers

GENERAL DESCRIPTION

The ADA4938-1 is a low noise, ultra-low distortion, high speed differential amplifier. It is an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 70 MHz. The output common mode voltage is adjustable over a wide range, allowing the ADA4938-1 to match the input of the ADC. The internal common mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

Full differential and single-ended to differential gain configurations are easily realized with the ADA4938-1. A simple external feedback network of four resistors determines the amplifier's closed-loop gain.

The ADA4938-1 is fabricated using ADI's proprietary third generation high-voltage XFCB process, enabling it to achieve very low levels of distortion with input voltage noise of only 2.2 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4938-1 make it well suited for a wide variety of data acquisition and signal processing and applications.

The ADA4938-1 is available in a Pb-free, 3 mm x 3mm lead frame chip scale package (LFCSP). It is specified to operate over the extended industrial temperature range of −40°C to +85°C.

Rev. PrA

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REVISION HISTORY

12/06—Revision PrA: Initial Version

SPECIFICATIONS

DUAL SUPPLY OPERATION

At 25 °C, $+V_S$ = 5 V, $-V_S$ = −5 V, V_{OCM} = 0 V, $R_G = R_F$ = 200 Ω, G = +1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} TO ±OUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, Differential Input		1500		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, Differential Input		125		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, Differential Input		1300		MHz
	V_{OUT} = 4 V p-p, Differential Input		800		MHz
Slew Rate	V_{OUT} = 2 V p-p		4700		V/µs
Settling Time	0.01%, V_{OUT} = 2 Vp-p		8.5		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE[1]					
Second Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−108		dBc
	V_{OUT} = 2 V p-p, 70 MHz		−79		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−125		dBc
	V_{OUT} = 2 V p-p, 70 MHz		−87		dBc
IMD	70 MHz				dBc
IP3	70 MHz				dBm
Voltage Noise (RTI)			2.2		nV/√Hz
Noise Figure	G = +2		12		dB
Input Current Noise			2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-}$ = 0 V		1		mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current			3.5		µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−4.7 to 3.4		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V		−77		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output	1		4	V
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V; 10 MHz		−66		dB
V_{OCM} to ±OUT PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			400		MHz
Slew Rate			1700		V/µs
INPUT VOLTAGE NOISE (RTI)			7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		−3.8		3.8	V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-}$ = 0 V		1	3.5	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		1		V/V
POWER SUPPLY					

Parameter	Conditions	Min	Typ	Max	Unit
Operating Range		4.5		12	V
Quiescent Current			40		mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
	Powered down		< 1		mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; $\Delta V_S = \pm 1$ V		−90		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤ 1		V
	Enabled		≥ 2		V
Turn-Off Time			1		µs
Turn-On Time			200		ns
$\overline{PD}$ Bias Current					
Enabled	$\overline{PD}$ = 5 V		40		µA
Disabled	$\overline{PD}$ = 0 V		200		µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

SINGLE SUPPLY OPERATION

At 25 °C, $+V_S$ = 5 V, $-V_S$ = 0 V, V_{OCM} = 2.5 V, R_G = R_F = 200 Ω, G = +1, R_L, dm = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential output, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} TO ±OUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, Differential Input		1500		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p, Differential Input		125		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, Differential Input		1100		MHz
Slew Rate	V_{OUT} = 2 V p-p		3900		V/µs
Settling Time	0.01%, V_{OUT} = 2 V p-p		8.1		ns
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−115		dBc
	V_{OUT} = 2 V p-p, 70 MHz		−87		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−110		dBc
	V_{OUT} = 2 V p-p, 70 MHz		−79		dBc
IMD	70 MHz				dBc
IP3	70 MHz				dBm
Voltage Noise (RTI)			2.2		nV/√Hz
Noise Figure	G = +2		12		dB
Input Current Noise			2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		1		mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current			3.5		µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			0.3 to 3.4		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V		−77		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output	1.1		3.9	V
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−66		dB
V_{OCM} TO ±OUT PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			400		MHz
Slew Rate	V = 0.5 V		1700		V/µs
INPUT VOLTAGE NOISE (RTI)					nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		1.2		3.8	V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS, cm}$ = $V_{OUT, cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		1		mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		1		V/V
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current			36		mA
	T_{MIN} to T_{MAX} variation		40		µA/°C

Parameter	Conditions	Min	Typ	Max	Unit
	Powered down		< 1		mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; $\Delta V_S = \pm 1$ V		−90		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤ 1		V
	Enabled		≥ 2		V
Turn-Off Time			1		μs
Turn-On Time			200		ns
PD Bias Current					
Enabled	$\overline{PD}$ = 5 V		20		μA
Disabled	$\overline{PD}$ = 0 V		−120		μA
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	TBD
Power Dissipation	See Figure 2
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for a device (including exposed pad) soldered to the circuit board.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	TBD	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4938-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4938-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through-holes, ground, and power planes reduces the θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP (TBD °C/W) on a JEDEC standard 4-layer board.

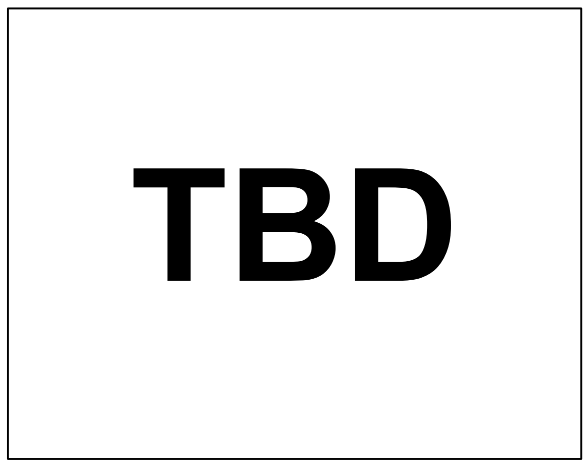
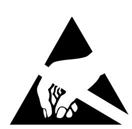


Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

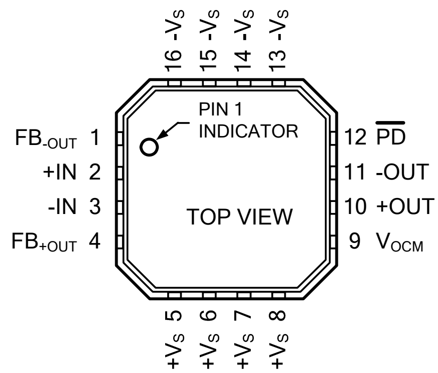
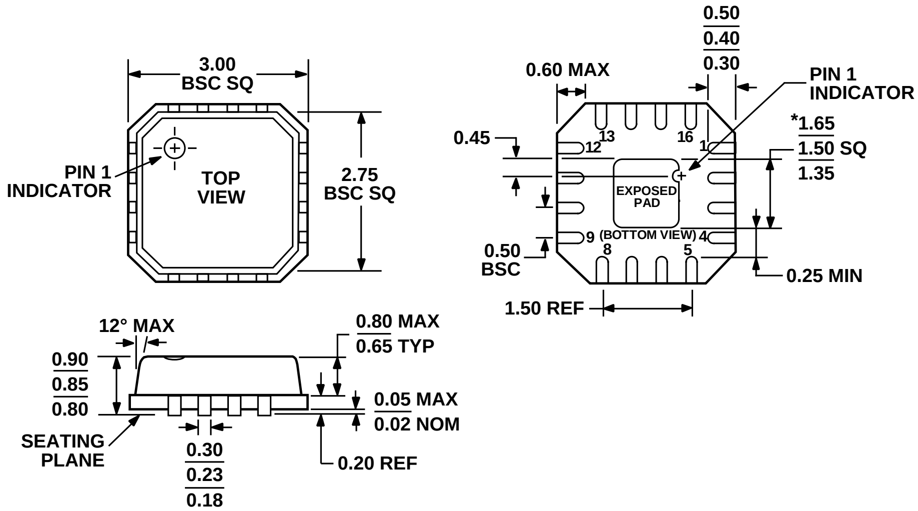


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB_{-OUT}	Negative output feedback pin
2	+IN	Positive input summing node
3	−IN	Negative input summing node
4	FB_{+OUT}	Positive output feedback pin
5 to 8	$+V_S$	Positive supply voltage
9	V_{OCM}	Output common mode voltage
10	+OUT	Positive output
11	−OUT	Negative output
12	$\overline{PD}$	Power-down pin
13 to 16	$-V_S$	Negative supply voltage

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 4. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Ordering Quantity	Temperature Range	Package Description	Package Option	Branding
ADA4938-1YCPZ-R2	5,000	−40°C to +85°C	16-Lead 3 mm × 3 mm LFCSP	CP-16 -3	
ADA4938-1YCPZ-RL	1,500	−40°C to +85°C	16-Lead 3 mm × 3 mm LFCSP	CP-16 -3	
ADA4938-1YCPZ-R7	250	−40°C to +85°C	16-Lead 3 mm × 3 mm LFCSP	CP-16 -3	

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