1 nV/√Hz, Low Power, Rail-to-Rail Output Amplifiers

ADA4896-2/ADA4897-1

FEATURES

- **Low wideband noise**
  - **1 nV/√Hz**
  - **2.8 pA/√Hz**
- **Low 1/f noise**
  - **2.4 nV/√Hz @ 10 Hz**
- **Low distortion: −115 dBc @ 100 kHz, V_{OUT} = 2 V p-p**
- **Low power: 3 mA/amp**
- **Low input offset voltage: 0.5 mV maximum**
- **High speed**
  - **230 MHz, −3 dB bandwidth (G = +1)**
  - **120 V/µs slew rate**
  - **45 ns settling time to 0.1%**
- **Rail-to-rail output**
- **Wide supply range: 3 V to 10 V**
- **Disable feature (ADA4897-1)**

APPLICATIONS

- **Low noise preamplifier**
- **Ultrasound amplifiers**
- **PLL loop filters**
- **High performance ADC drivers**
- **DAC buffers**

GENERAL DESCRIPTION

The ADA4896-2/ADA4897-1 are unity gain stable, low noise, rail-to-rail output, high speed voltage feedback amplifiers that have a quiescent current of 3 mA. With the 1/f noise of 2.4 nV/√Hz at 10 Hz and a spurious-free dynamic range of −80 dBc at 2 MHz, the ADA4896-2/ADA4897-1 are an ideal solution in a variety of applications, including ultrasound, low noise preamplifiers, and drivers of high performance ADCs. The Analog Devices, Inc., proprietary next generation SiGe bipolar process and innovative architecture enable such high performance amplifiers.

TheADA4896-2/ADA4897-1 have 230 MHz bandwidth, 120 V/µs slew rate, and settle to 0.1% in 45 ns. With a wide supply voltage range (3 V to 10 V), the ADA4896-2/ADA4897-1 are ideal candidates for systems that require high dynamic range, precision, and high speed.

The ADA4896-2 is available in 8-lead LFCSP and 8-lead MSOP packages. The ADA4897-1 is available in 8-lead SOIC and 6-lead SOT-23 packages. Both the ADA4896-2 and ADA4897-1 work over the extended industrial temperature range of −40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

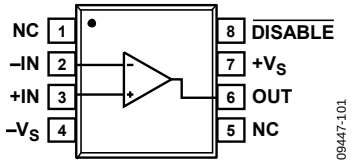

Figure 1. 8-Lead SOIC (ADA4897-1)

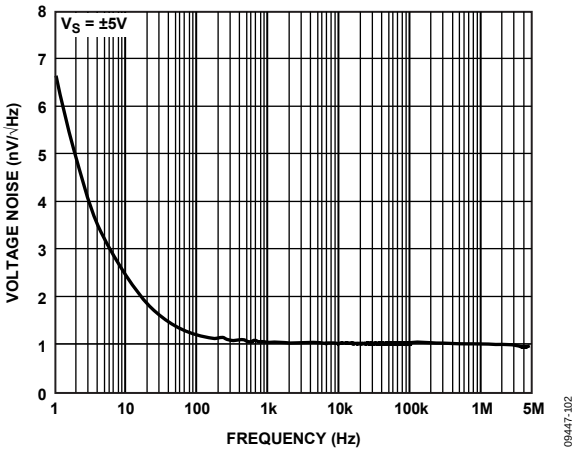

Figure 2. Voltage Noise vs. Frequency

Table 1. Other Low Noise Amplifiers

Part Number	V_N (nV/√Hz) @ 1 kHz	V_N (nV/√Hz) @ 100 kHz	BW (MHz)	Supply Voltage (V)
AD797	0.9	0.9	8	10 to 30
AD8021	5	2.1	490	5 to 24
AD8099	7	0.95	510	5 to 12
AD8045	6	3	1000	3.3 to 12
ADA4899-1	1.4	1	600	5 to 12
ADA4898-1/ ADA4898-2	0.9	0.9	65	10 to 32

Table 2. Complementary ADCs

Part Number	Bits	Speed (MSPS)	Power (mW)
AD7944	14	2.5	15.5
AD7985	16	2.5	15.5
AD7986	18	2	15

Rev. 0

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REVISION HISTORY

7/11—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, G = +1, R_L = 1 kΩ to ground, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		230		MHz
	G = +1, V_{OUT} = 2 V p-p		30		MHz
	G = +2, V_{OUT} = 0.02 V p-p		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 100 Ω		7		MHz
Slew Rate	G = +2, V_{OUT} = 6 V step		120		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		45		ns
Settling Time to 0.01%	G = +2, V_{OUT} = 2 V step		90		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (dBc) SFDR	f_C = 100 kHz, V_{OUT} = 2 V p-p		–115		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		–93		dBc
	f_C = 2 MHz, V_{OUT} = 2 V p-p		–80		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		–61		dBc
Input Voltage Noise	f = 10 Hz		2.4		nV/√Hz
	f = 100 kHz		1		nV/√Hz
Input Current Noise	f = 10 Hz		31		pA/√Hz
	f = 100 kHz		2.8		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		–500	–28	+500	µV
Input Offset Voltage Drift			0.2		µV/°C
Input Bias Current		–17	–11	–4	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current		–0.6	–0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = –4 V to +4 V	100	110		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode/differential		10 M/10 k		Ω
Input Capacitance	Common mode/differential		3/11		pF
Input Common-Mode Voltage Range			–4.9 to +4.1		V
Common-Mode Rejection	V_{CM} = –2 V to +2 V	–92	–120		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±5 V, G = +2		81		ns
+Output Voltage Swing	R_L = 1 kΩ	4.85	4.96		V
–Output Voltage Swing	R_L = 1 kΩ	–4.85	–4.97		V
+Output Voltage Swing	R_L = 100 Ω	4.5	4.73		V
–Output Voltage Swing	R_L = 100 Ω	–4.5	–4.84		V
Output Current	45 dBc SFDR		80		mA
Short-Circuit Current	Sinking/sourcing		135		mA
Capacitive Load Drive	30% overshoot, G = +2		39		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.8	3.0	3.2	mA
	$\overline{\text{DISABLE}}$ = –5 V		0.25		mA
Positive Power Supply Rejection	$+V_S$ = 4 V to 6 V, $-V_S$ = –5 V	–96	–125		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $-V_S$ = –4 V to –6 V	–96	–121		dB

Parameter	Conditions	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$ PIN (ADA4897-1)					
$\overline{\text{DISABLE}}$ Voltage	Enabled		>+V_S − 0.5		V
	Disabled		<+V_S − 2		V
Input Current					
Enabled	$\overline{\text{DISABLE}}$ = +5 V		−2.5		μA
Disabled	$\overline{\text{DISABLE}}$ = −5 V		−80		μA
Switching Speed					
Enabled			0.25		μs
Disabled			12		μs

+5 V SUPPLY

T_A = 25°C, G = +1, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		230		MHz
	G = +1, V_{OUT} = 2 V p-p		30		MHz
	G = +2, V_{OUT} = 0.02 V p-p		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 100 Ω		7		MHz
Slew Rate	G = +2, V_{OUT} = 3 V step		100		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		45		ns
Settling Time to 0.01%	G = +2, V_{OUT} = 2 V step		95		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (dBc) SFDR	f_C = 100 kHz, V_{OUT} = 2 V p-p		−115		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−93		dBc
	f_C = 2 MHz, V_{OUT} = 2 V p-p		−80		dBc
	f_C = 5 MHz, V_{OUT} = 2 V p-p		−61		dBc
Input Voltage Noise	f = 10 Hz		2.4		nV/√Hz
	f = 100 kHz		1		nV/√Hz
Input Current Noise	f = 10 Hz		31		pA/√Hz
	f = 100 kHz		2.8		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−500	−30	+500	µV
Input Offset Voltage Drift			0.2		µV/°C
Input Bias Current		−17	−11	−4	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = 0.5 V to 4.5 V	97	110		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode/differential		10 M/10 k		Ω
Input Capacitance	Common mode/differential		3/11		pF
Input Common-Mode Voltage Range			0.1 to 4.1		V
Common-Mode Rejection	V_{CM} = +1 V to +4 V	−91	−118		dB
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time	V_{IN} = 0 V to 5 V, G = +2		96		ns
+Output Voltage Swing	R_L = 1 kΩ	4.85	4.98		V
−Output Voltage Swing	R_L = 1 kΩ	0.15	0.014		V
+Output Voltage Swing	R_L = 100 Ω	4.8	4.88		V
−Output Voltage Swing	R_L = 100 Ω	0.2	0.08		
Output Current	45 dBc SFDR		70		mA
Short-Circuit Current	Sinking/sourcing		125		mA
Capacitive Load Drive	30% overshoot, G = +2		39		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.6	2.8	2.9	mA
	$\overline{\text{DISABLE}}$ = 0 V		0.18		
Positive Power Supply Rejection	$+V_S$ = 4.5 V to 5.5 V, $-V_S$ = 0 V	−96	−123		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V	−96	−121		dB

Parameter	Conditions	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$ PIN (ADA4897-1)					
$\overline{\text{DISABLE}}$ Voltage	Enabled		>+V_S − 0.5		V
	Disabled		<+V_S − 2		V
Input Current					
Enabled	$\overline{\text{DISABLE}}$ = +5 V		−2.5		µA
Disabled	$\overline{\text{DISABLE}}$ = 0 V		−50		µA
Switching Speed					
Enabled			0.25		µs
Disabled			12		µs

+3 V SUPPLY

T_A = 25°C, G = +1, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		230		MHz
	G = −1, V_{OUT} = 1 V p-p		45		MHz
	G = +2, V_{OUT} = 0.02 V p-p		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 100 Ω		7		MHz
Slew Rate	G = +2, V_{OUT} = 1 V step		85		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		45		ns
Settling Time to 0.01%	G = +2, V_{OUT} = 2 V step		96		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (dBc) SFDR	f_C = 100 kHz, V_{OUT} = 2 V p-p, G = +2		−105		dBc
	f_C = 1 MHz, V_{OUT} = 1 V p-p, G = −1		−84		dBc
	f_C = 2 MHz, V_{OUT} = 1 V p-p, G = −1		−77		dBc
	f_C = 5 MHz, V_{OUT} = 1 V p-p, G = −1		−60		dBc
Input Voltage Noise	f = 10 Hz		2.3		nV/√Hz
	f = 100 kHz		1		nV/√Hz
Input Current Noise	f = 10 Hz		31		pA/√Hz
	f = 100 kHz		2.8		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−500	−30	+500	uV
Input Offset Voltage Drift			0.2		µV/°C
Input Bias Current		−17	−11	−4	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = 0.5 V to 2.5 V	95	108		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode/differential		10 M/10 k		Ω
Input Capacitance	Common mode/differential		3/11		pF
Input Common-Mode Voltage Range			0.1 to 2.1		V
Common-Mode Rejection	V_{CM} = +1.1 V to +1.9 V	−90	−124		dB
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time	V_{IN} = 0 V to +3 V, G = +2		83		ns
+Output Voltage Swing	R_L = 1 kΩ	2.85	2.97		V
−Output Voltage Swing	R_L = 1 kΩ	0.15	0.01		V
+Output Voltage Swing	R_L = 100 Ω	2.8	2.92		V
−Output Voltage Swing	R_L = 100 Ω	0.2	0.05		V
Output Current	45 dBc SFDR		60		mA
Short-Circuit Current	Sinking/sourcing		120		mA
Capacitive Load Drive	30% overshoot, G = +2		39		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.5	2.7	2.9	mA
	$\overline{\text{DISABLE}}$ = 0 V		0.15		
Positive Power Supply Rejection	$+V_S$ = 2.7 V to 3.7 V, $-V_S$ = 0 V	−96	−121		dB
Negative Power Supply Rejection	$+V_S$ = 3 V, $-V_S$ = −0.3 V to 0.7 V	−96	−120		dB

Parameter	Conditions	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$ PIN (ADA4897-1)					
$\overline{\text{DISABLE}}$ Voltage	Enabled		>+V_S −0.5		V
	Disabled		<−V_S + 2		V
Input Current					
Enabled	$\overline{\text{DISABLE}}$ = +3 V		−2.5		μA
Disabled	$\overline{\text{DISABLE}}$ = 0 V		−40		μA
Switching Speed					
Enabled			0.25		μs
Disabled			12		μs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	±0.7 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 7 lists the θ_{JA} for the ADA4896-2/ADA4897-1.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead Dual MSOP (ADA4896-2)	222	°C/W
8-Lead Dual LFCSP (ADA4896-2)	61	°C/W
8-Lead Single SOIC (ADA4897-1)	133	°C/W
6-Lead Single SOT-23 (ADA4897-1)	306	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4896-2/ADA4897-1 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4896-2/ADA4897-1. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality. The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4896-2/ADA4897-1 drive at the output.

The quiescent power is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^{\ 2}}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes, reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the dual 8-lead LFCSP (61°C/W), the dual 8-lead MSOP (222°C/W), the single 8-lead SOIC (133°C/W), and the single 6-lead SOT-23 (306°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

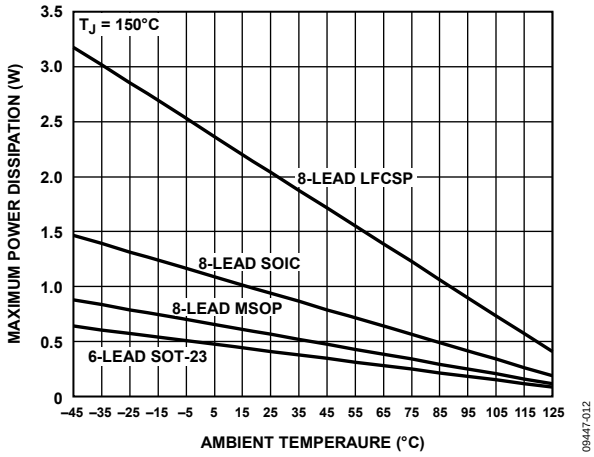


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

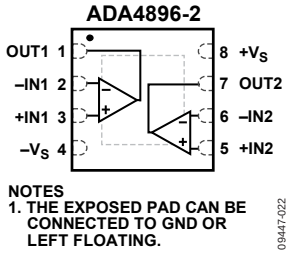


Figure 4. 8-Lead LFCSP Pin Configuration

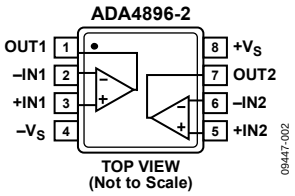


Figure 5. 8-Lead MSOP Pin Configuration

Table 8. ADA4896-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT1	Output 1.
2	–IN1	Inverting Input 1.
3	+IN1	Noninverting Input 1.
4	$-V_S$	Negative Supply.
5	+IN2	Noninverting Input 2.
6	–IN2	Inverting Input 2.
7	OUT2	Output 2.
8	$+V_S$	Positive Supply.
	EPAD	Exposed Pad. The exposed pad can be connected to GND or left floating.

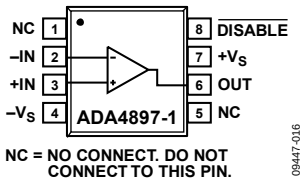


Figure 6. 8-Lead SOIC Pin Configuration

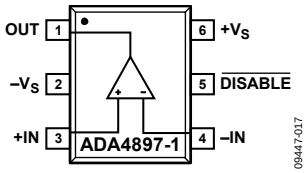


Figure 7. 6-Lead SOT-23 Pin Configuration

Table 9. ADA4897-1 Pin Function Descriptions

Pin No.			
SOIC	**SOT-23**	**Mnemonic**	**Description**
1, 5	N/A	NC	Do not connect to this pin.
2	4	–IN	Inverting Input.
3	3	+IN	Noninverting Input.
4	2	$-V_S$	Negative Supply.
6	1	OUT	Output.
7	6	$+V_S$	Positive Supply.
8	5	$\overline{\text{DISABLE}}$	Disable.

TYPICAL PERFORMANCE CHARACTERISTICS

R_L = 1 kΩ,unless otherwise noted.When G > +1, R_F = 249 Ω and when G = +1, R_F = 0 Ω.

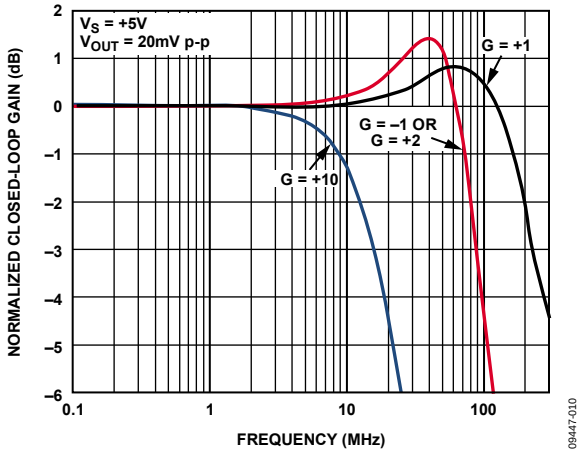


Figure 8. Small Signal Frequency Response vs. Gain

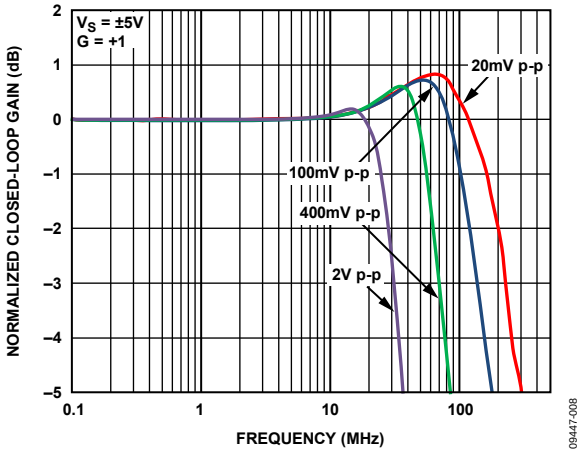


Figure 11. Frequency Response for Various V_{OUT}

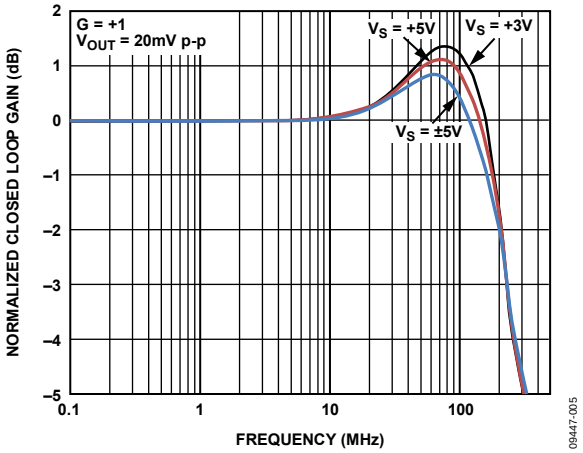


Figure 9. Small Signal Frequency Response vs. Supply Voltage

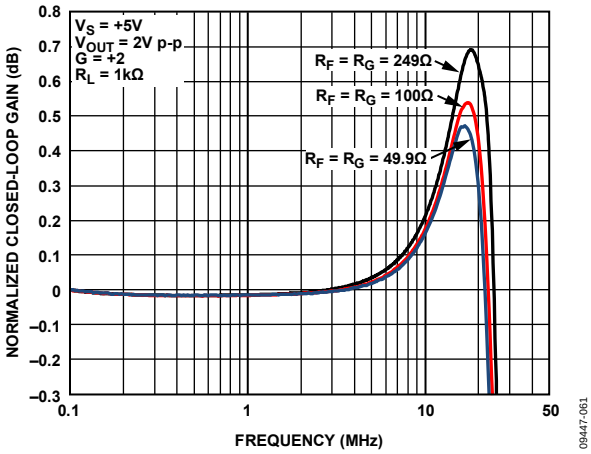


Figure 12. 0.1 dB Bandwidth at Selected R_F Value

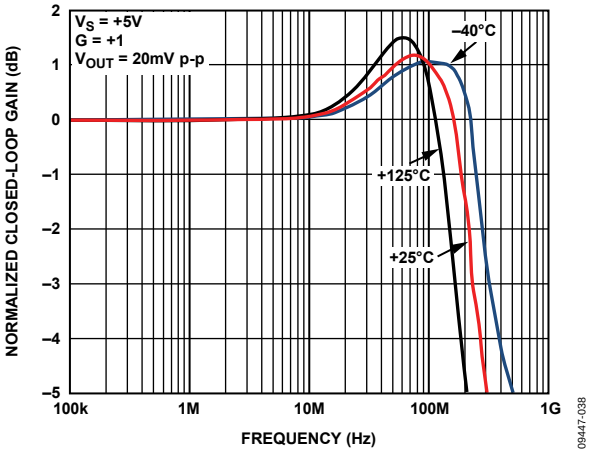


Figure 10. Small Signal Frequency Response vs. Temperature

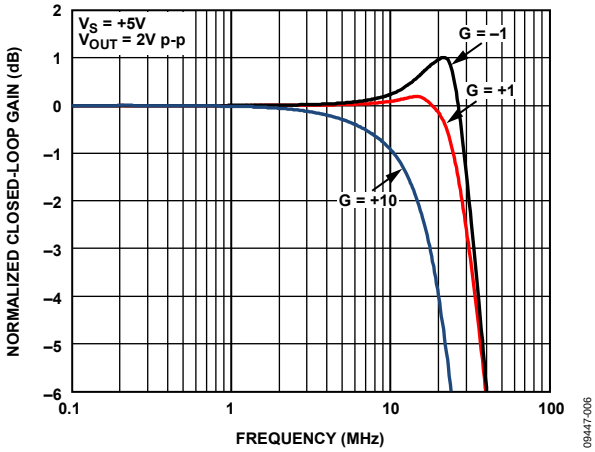


Figure 13. Large Signal Frequency Response vs. Gain

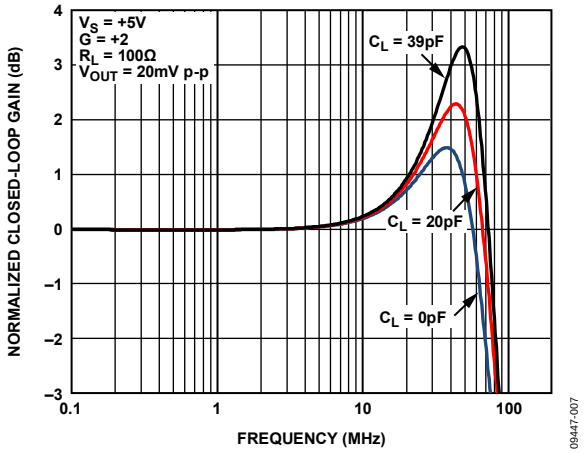


Figure 14. Small Signal Frequency Response vs. Capacitive Load

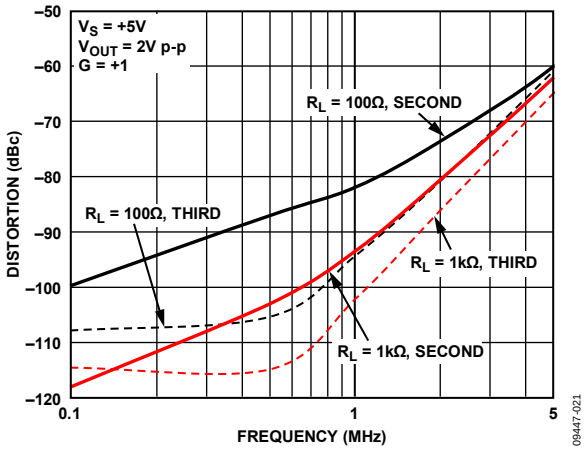


Figure 15. Harmonic Distortion vs. Frequency, G = +1

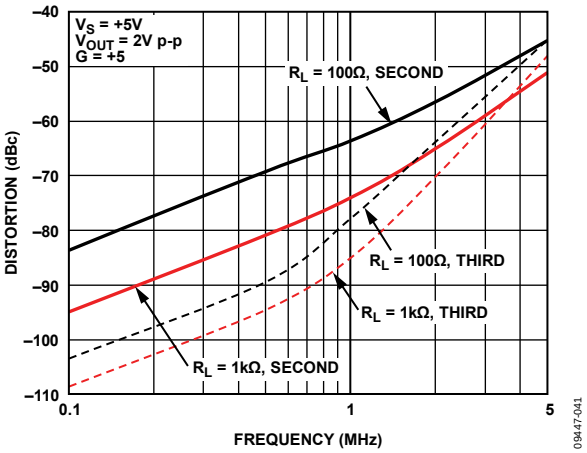


Figure 16. Harmonic Distortion vs. Frequency, G = +5

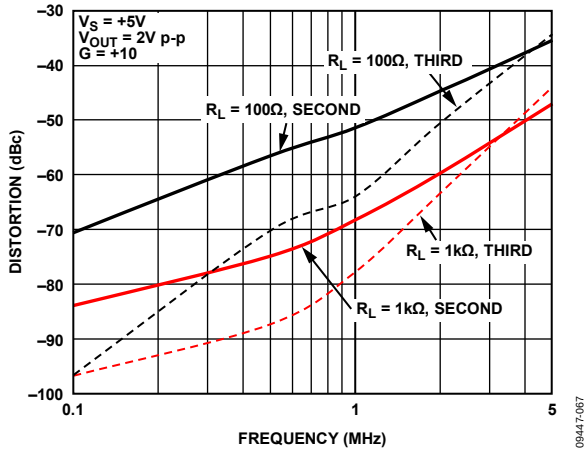


Figure 17. Harmonic Distortion vs. Frequency, G = +10

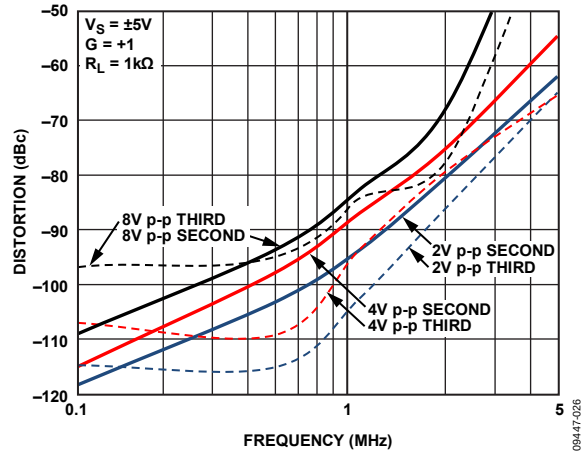


Figure 18. Harmonic Distortion vs. Frequency for Various Output Voltages

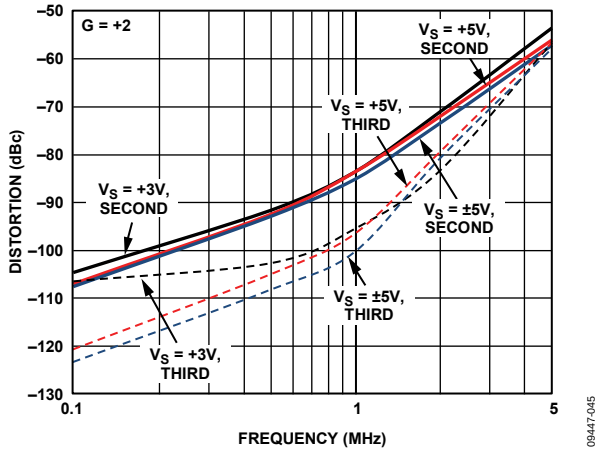


Figure 19. Harmonic Distortion vs. Frequency for Various Supplies

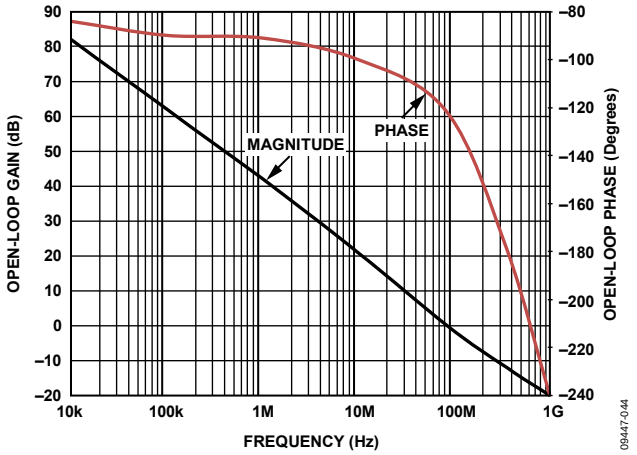


Figure 20. Open-Loop Gain and Phase vs. Frequency

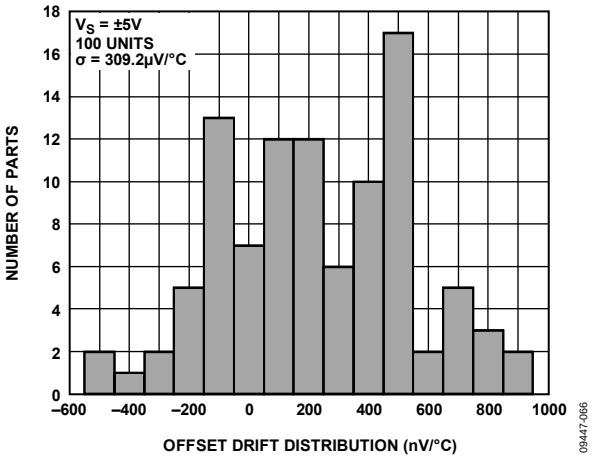


Figure 23. Input Offset Voltage Drift Distribution

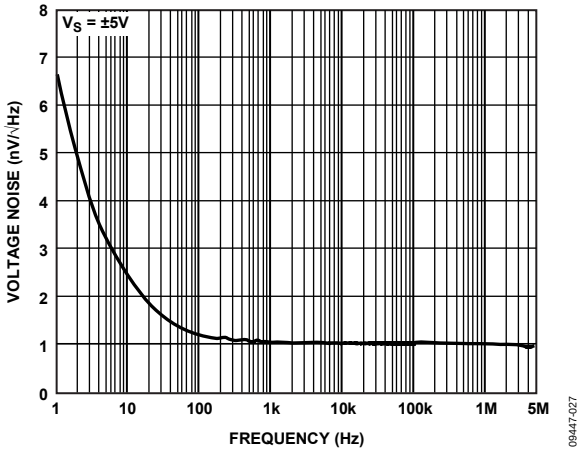


Figure 21. Voltage Noise vs. Frequency

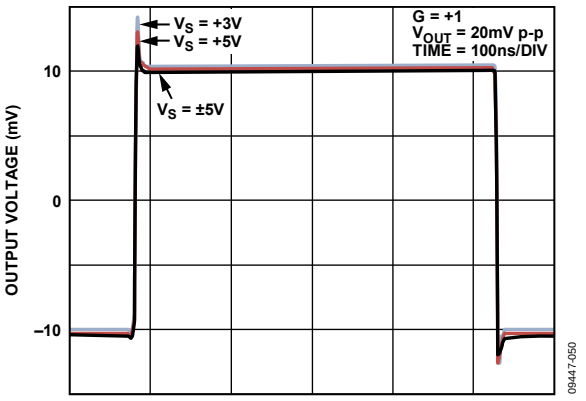


Figure 24. Small Signal Transient Response for Various Supplies

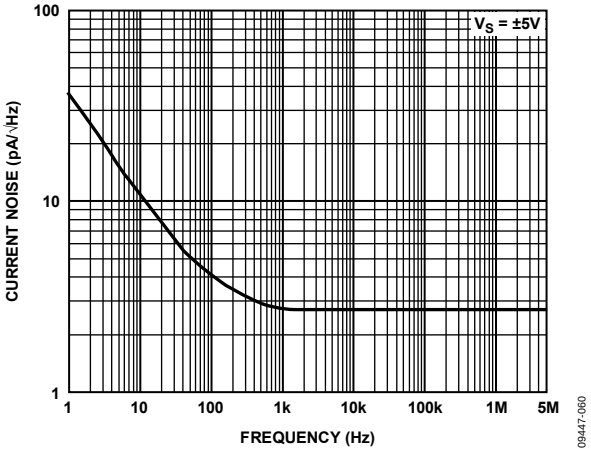


Figure 22. Current Noise vs. Frequency

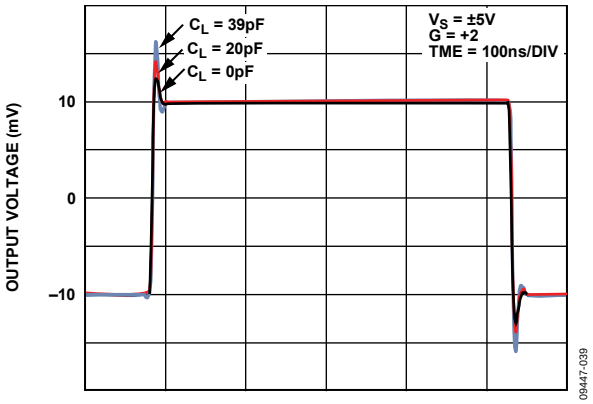


Figure 25. Small Signal Transient Response for Various Capacitive Loads

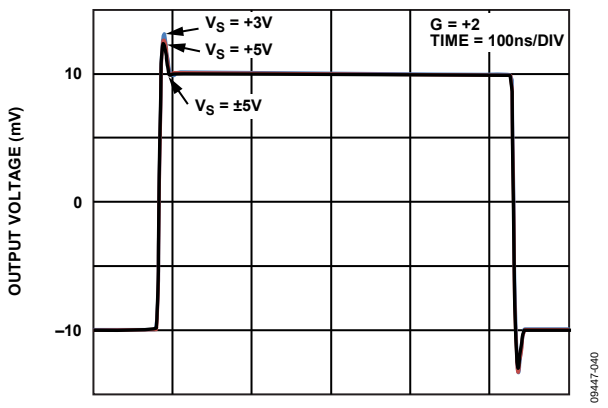


Figure 26. Small Signal Transient Response for Various Supplies, G = +2

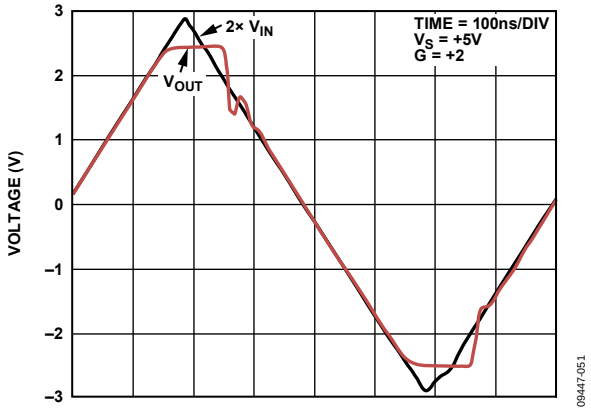


Figure 29. Output Overdrive Recovery

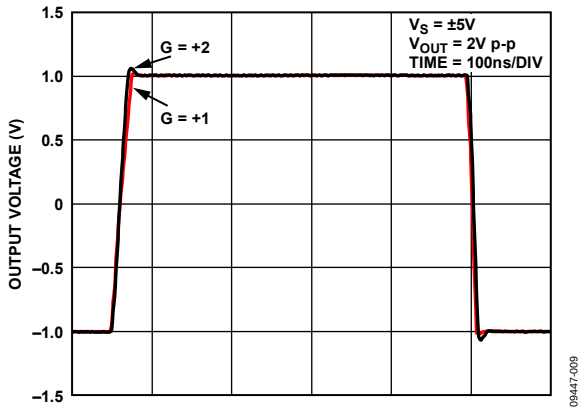


Figure 27. Large Signal Transient Response for Various Gains

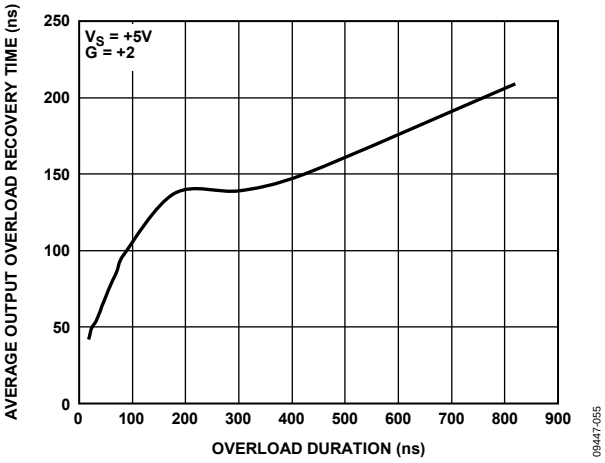


Figure 30. Output Recovery Time vs. Overload Duration

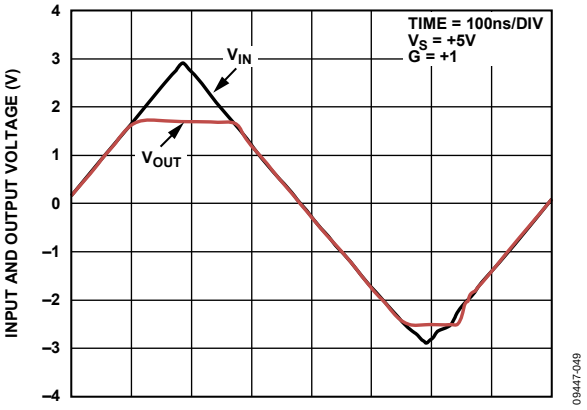


Figure 28. Input Overdrive Recovery

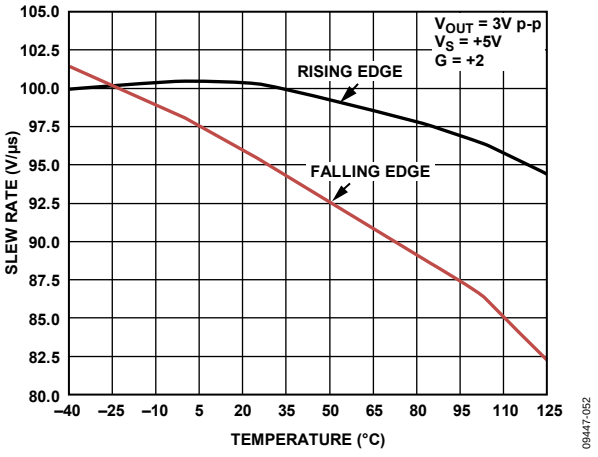


Figure 31. Slew Rate vs. Temperature

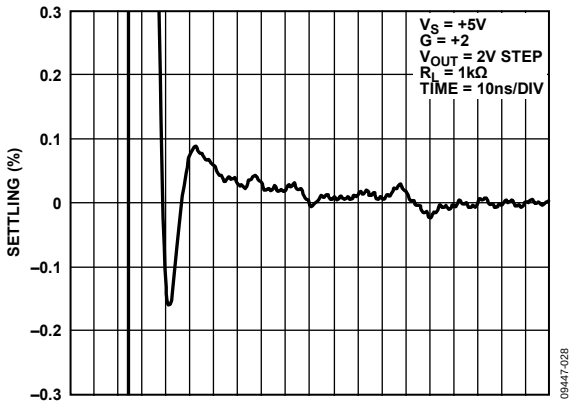


Figure 32. Settling Time to 0.1%

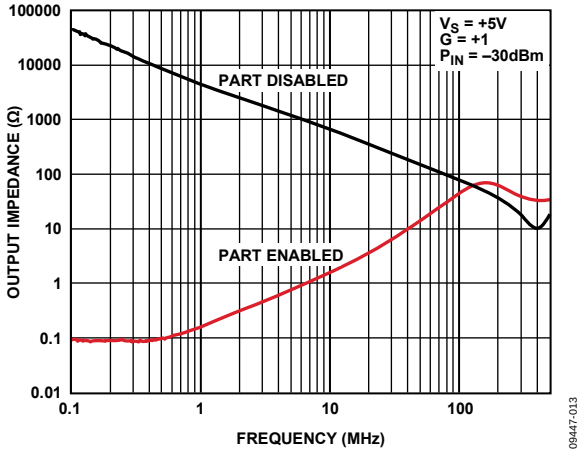


Figure 35. Output Impedance vs. Frequency

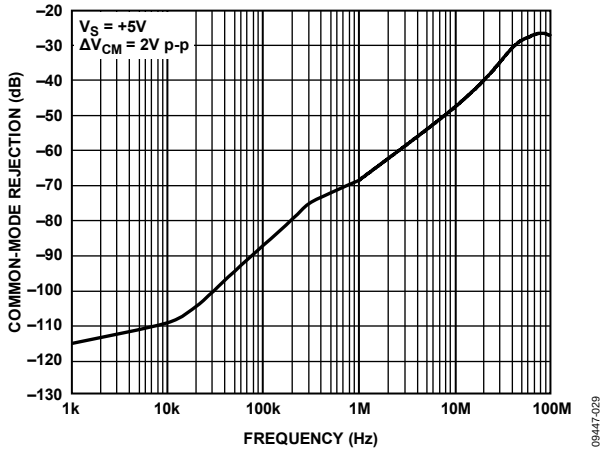


Figure 33. CMRR vs. Frequency

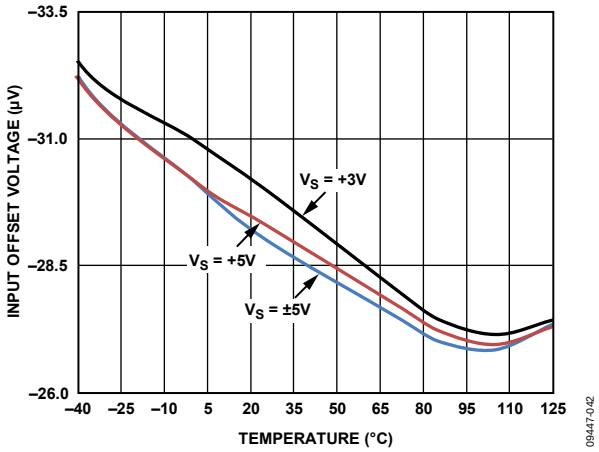


Figure 36. Input Offset Voltage vs. Temperature for Various Supplies

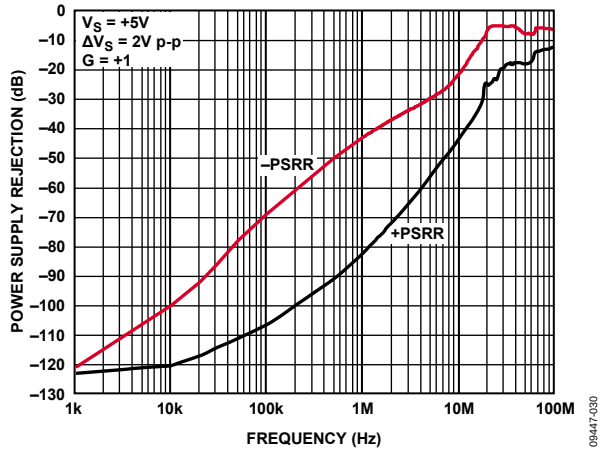


Figure 34. PSRR vs. Frequency

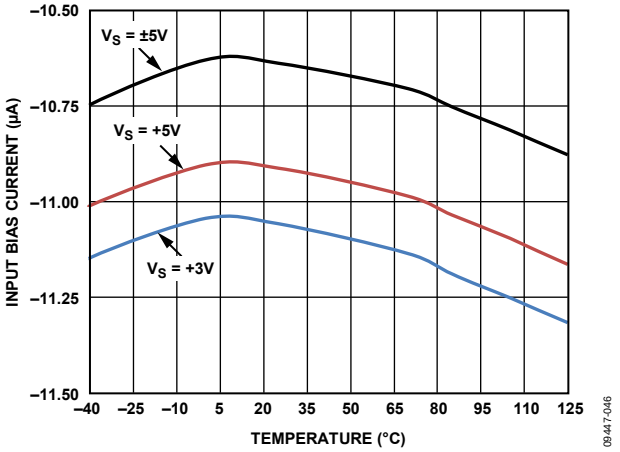


Figure 37. Input Bias Current vs. Temperature for Various Supplies

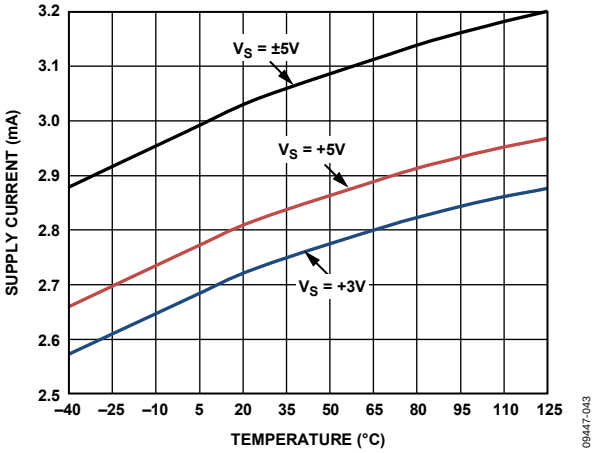


Figure 38. Supply Current vs. Temperature for Various Supplies

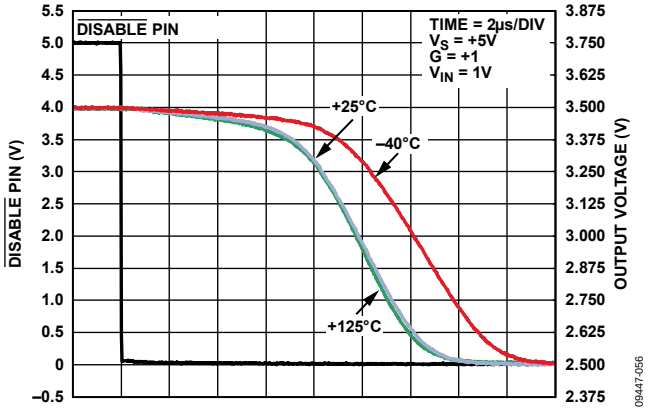


Figure 41. Turn-Off Time vs. Temperature

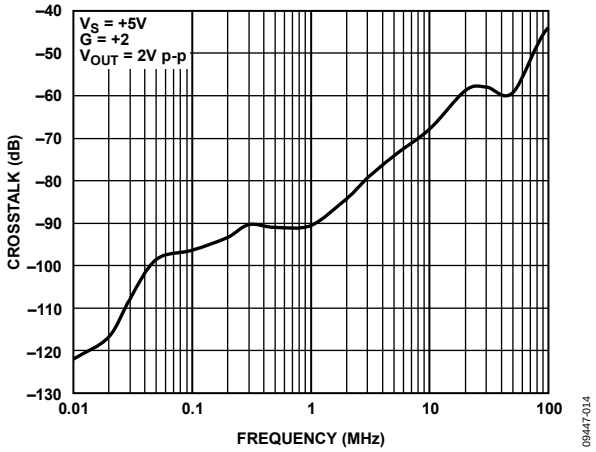


Figure 39. Crosstalk OUT1 to OUT2 (ADA4896-2 Only)

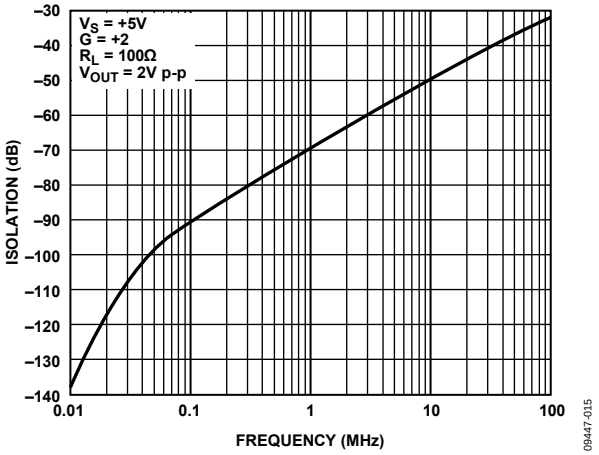


Figure 42. Forward Isolation vs. Frequency

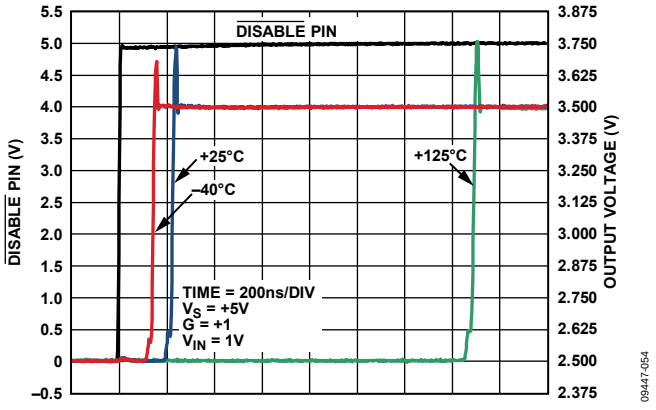


Figure 40. Turn-On Time vs. Temperature

THEORY OF OPERATION

AMPLIFIER DESCRIPTION

The ADA4896-2/ADA4897-1 are 1 nV/√Hz input noise amplifiers that consume 3 mA from supplies ranging from 3 V to 10 V. Utilizing the Analog Devices XFCB3 process, the bandwidth is in excess of 200 MHz and unity gain stable and the input structure results in an extremely low input of 1/f noise for a high speed amplifier. The rail-to-rail output stage is designed to drive a heavy feedback load required to achieve an overall low output referred noise. Unlike other low noise unity gain stable amplifiers, the large signal bandwidth has been enhanced beyond the typical fundamental limits to meet more demanding system requirements. The maximum offset of 500 µV and drift of 1 µV/°C make the ADA4896-2/ADA4897-1 an excellent amplifier choice even when the noise is not needed because there is minimal power penalty in achieving the low input noise or the high bandwidth.

INPUT PROTECTION

The ADA4896-2/ADA4897-1 are fully protected from ESD events, withstanding human body model ESD events of 2.5 kV and charge device model events of 1 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 43.

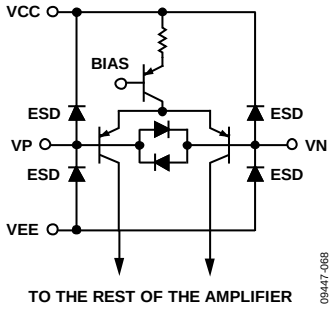


Figure 43. Input Stage and Protection Diodes

For differential voltages above approximately 0.7 V, the diode clamps start to conduct. Too much current can cause damage due to excessive heating. If large differential voltages must be sustained across the input terminals, it is recommended that the current through the input clamps be limited to below 10 mA. Series input resistors that are sized appropriately for the expected differential overvoltage provide the needed protection.

The ESD clamps start to conduct for input voltages that are more than 0.7 V above the positive supply and input voltages more than 0.7 V below the negative supply. It is recommended that the fault current be limited to less than 10 mA if an overvoltage condition is expected.

DISABLE OPERATION

Figure 44 shows the ADA4897-1 power-down circuitry. If the $\overline{\text{DISABLE}}$ pin is left unconnected, the base of the input PNP transistor is pulled high through the internal pull-up resistor to the positive supply and the part is turned on. Pulling the $\overline{\text{DISABLE}}$ pin to ≥2 V below the positive supply turns the part off, reducing the supply current to approximately 18 µA for a 5 V voltage supply.

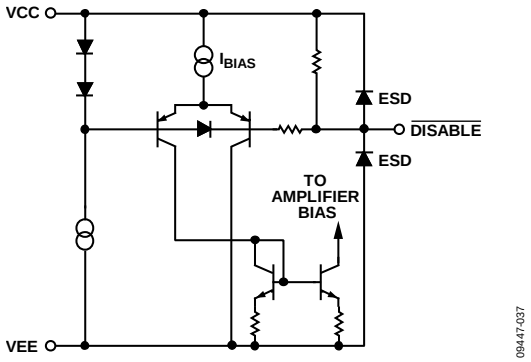


Figure 44. $\overline{\text{DISABLE}}$ Circuit

The $\overline{\text{DISABLE}}$ pin is protected with ESD clamps, as shown in Figure 44. Voltages beyond the power supplies cause these diodes to conduct. For protection of the $\overline{\text{DISABLE}}$ pin, the voltage to this pin should not exceed 0.7 V of the supply voltage, or the input current should be restricted to less than 10 mA with a series resistor.

When the amplifier is disabled, its output goes to a high impedance state. The output impedance decreases as frequency increases; this effect can be observed in Figure 35. In disable mode, a forward isolation of 50 dB can be achieved at 10 MHz. Figure 42 shows the forward isolation vs. frequency data.

DC ERRORS

Figure 45 shows a typical connection diagram and the major dc error sources.

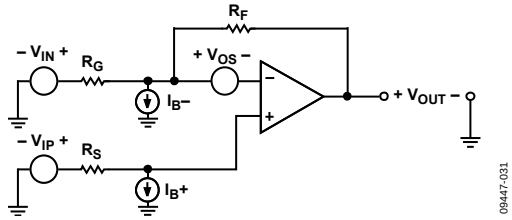


Figure 45. Typical Connection Diagram and DC Error Sources

The ideal transfer function (all error sources set to 0 and infinite dc gain) can be written as

$$V_{OUT} = \left(1+\frac{R_F}{R_G}\right)\times V_{IP} - \left(\frac{R_F}{R_G}\right)\times V_{IN} \quad (1)$$

This reduces to the familiar forms for inverting and noninverting op amp gain expressions, as follows:

(Noninverting gain, V_{IN} = 0 V)

$$V_{OUT} = \left(1+\frac{R_F}{R_G}\right)\times V_{IP} \quad (2)$$

(Inverting gain, V_{IP} = 0 V)

$$V_{OUT} = \left(\frac{-R_F}{R_G}\right)\times V_{IN} \quad (3)$$

The total output voltage error is the sum of errors due to the amplifier offset voltage and input currents. The output error due to the offset voltage can be estimated as

$$V_{OUT_{ERROR}} = \left(V_{OFFSET_{NOM}} + \frac{VCM}{CMRR} + \frac{V_P - V_{PNOM}}{PSRR} + \frac{V_{OUT}}{A}\right)\times\left(1+\frac{R_F}{R_G}\right) \quad (4)$$

where:

$V_{OFFSET_{NOM}}$ is the offset voltage at the specified supply voltage, which is measured with the input and output at midsupply.
VCM is the common-mode voltage.
V_P is the power supply voltage.
V_{PNOM} is the specified power supply voltage.
CMRR is the common-mode rejection ratio.
PSRR is the power supply rejection ratio.
A is the dc open-loop gain.

The output error due to the input currents can be estimated as

$$V_{OUT_{ERROR}} = (R_F \,||\, R_G)\times\left(1+\frac{R_F}{R_G}\right)I_{B-} - R_S \times\left(1+\frac{R_F}{R_G}\right)\times I_{B+} \quad (5)$$

Note that setting R_S equal to $R_F||R_G$ compensates for the voltage error due to the input bias current.

NOISE CONSIDERATIONS

Figure 46 illustrates the primary noise contributors for the typical gain configurations. The total rms output noise is the root-mean-square of all the contributions.

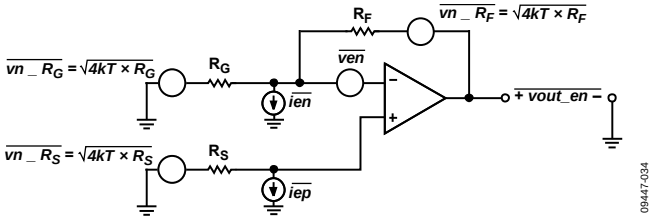


Figure 46. Noise Sources in Typical Connection

The output noise spectral density can be calculated by

$$\overline{vout\_en} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2\left[4kTRs + \overline{iep}^2 R_S{}^2 + \overline{ven}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + \overline{ien}^2 R_F{}^2} \quad (6)$$

where:

k is Boltzmann's Constant.
T is the absolute temperature, degrees Kelvin.
$\overline{ien}$ is the amplifier input current noise spectral density, pA/√Hz.
$\overline{ven}$ is the amplifier input voltage spectral density, nV/√Hz.
R_S is the source resistance, as shown in Figure 46.
R_F and R_G are the feedback network resistances, as shown in Figure 46.

Source resistance noise, amplifier voltage noise ($\overline{ven}$), and the voltage noise from the amplifier current noise ($\overline{iep} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$). Note that with a 1 nV/√Hz input voltage noise and 2.8 pA/√Hz input current, the noise contributions of the amplifier are relatively small for source resistances between approximately 50 Ω and 700 Ω. Figure 47 shows the total RTI noise due to the amplifier vs. the source resistance. In addition, the value of the feedback resistors used impacts the noise. It is recommended that the value of the feedback resistors be maintained between 250 Ω and 1 kΩ to keep the total noise low.

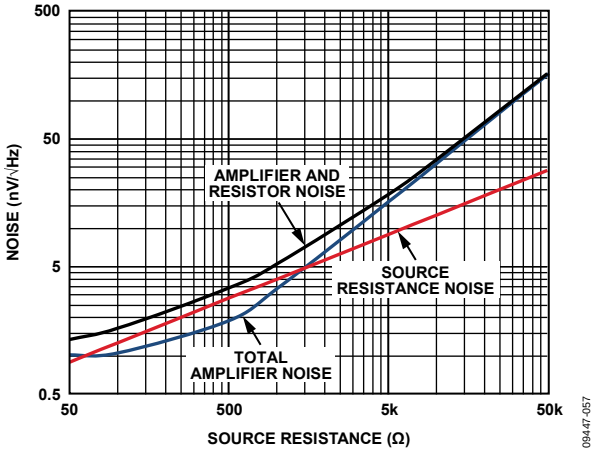


Figure 47. RTI Noise vs. Source Resistance

CAPACITANCE DRIVE

Capacitance at the output of an amplifier creates a delay within the feedback path that, if within the bandwidth of the loop, can create excessive ringing and oscillation. The ADA4897-1/ADA4896-2 show the most peaking at a gain of +2, as demonstrated in Figure 8.

Putting a small snub resistor (R_{SNUB}) in series with the amplifier output and the capacitive load mitigates the problem. Figure 48 shows the effect of using a snub resistor (R_{SNUB}) on reducing the peaking for the worst-case frequency response (gain of +2). Using R_{SNUB} = 100 Ω eliminates the peaking entirely, with the trade-off that the closed-loop gain is reduced by 0.8 dB due to attenuation at the output. R_{SNUB} can be adjusted from 0 Ω to 100 Ω to maintain an acceptable level of peaking and closed-loop gain, as shown in Figure 48.

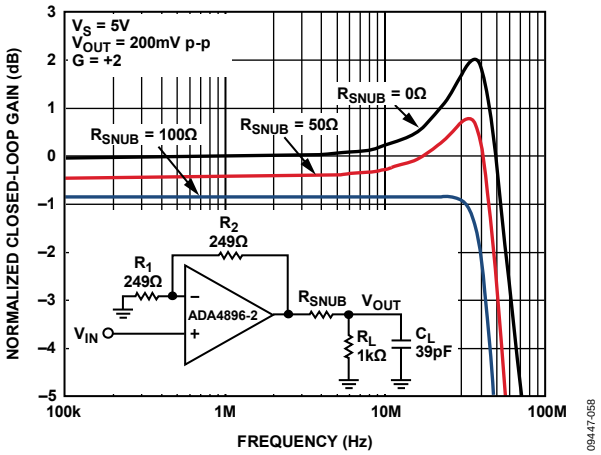


Figure 48. Using a Snub Resistor to Reduce Peaking Due to Output Capacitive Load

APPLICATIONS INFORMATION

TYPICAL PERFORMANCE VALUES

To reduce design time and eliminate uncertainty, Table 10 provides a convenient reference for typical gains, component values, and performance parameters. The supply voltage used is 5 V. The bandwidth is obtained with a small signal output of 200 mV p-p, and the slew rate is obtained with a 2 V output step. Note that as the gain increases, the small-signal bandwidth decreases, as is expected from the gain bandwidth product relationship. In addition, the phase margin improves with higher gains, and the amplifier becomes more stable. As a result, the peaking in the frequency response is reduced (see Figure 49).

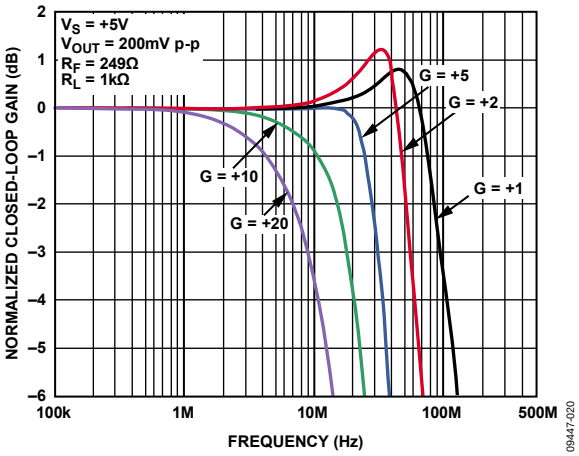


Figure 49. Small Signal Frequency Response at Various Gains

Table 10. Recommended Values and Typical Performance

Gain	R_F (Ω)	R_G (Ω)	−3 dB BW (MHz)	Slew Rate (t_R/t_F) (V/µs)	Peaking (dB)	Output Voltage Noise Only (nV/√Hz)	Total Output Noise Including Resistors (nV/√Hz)
+1	0	N/A	92	78/158	0.8	1	1.0
+2	249	249	54	101/140	1.2	2	3.6
+5	249	61.9	30	119/137	0	5	6.8
+10	249	27.4	17	87/88	0	10	12.0
+20	249	13.0	9	37/37	0	20	21.1

LOW NOISE GAIN SELECTABLE AMPLIFIER

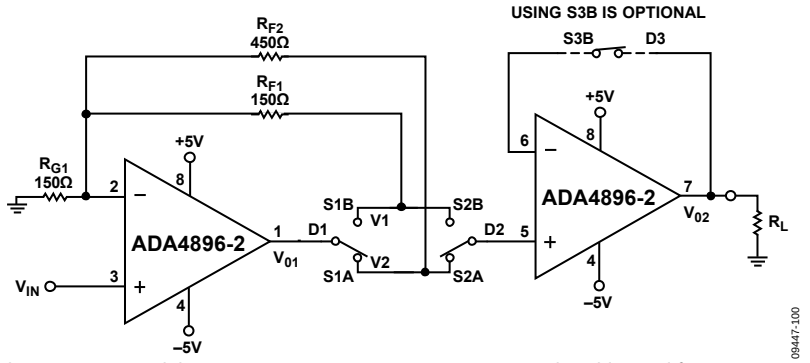


Figure 50. Using the ADA4896-2 and the ADG633 to Construct a Low Noise Gain Selectable Amplifier to Drive a Low Resistive Load

A gain selectable amplifier makes processing a wide range of input signals possible. The traditional gain selectable amplifier involves switches in the feedback loops connecting to the inverting input. In this case the switch resistance degrades the noise performance of the amplifier, as well as adding significant capacitance on the inverting input node. The noise and capacitance issue can be especially bothersome when working with low noise amplifiers. Also, the switch resistances contribute to nonlinear gain error, which is undesirable.

Figure 50 presents an innovative switching technique used in the gain selectable amplifier such that the 1 nV/Hz noise performance of the ADA4896-2 is preserved, while the nonlinear gain error is much reduced. With this technique, one can also choose switches with minimal capacitance, which optimizes the bandwidth of the circuit. In this circuit, the switches are implemented with the ADG633 and they are configured such that either S1A and S2A are on, or S1B and S2B are on. In this example, when the S1A and S2A switches are on, the first stage amplifier gain is +4. When the S1B and S2B switches are on, the first stage amplifier gain is +2. The first set of switches of the ADG633 is put in the output side of the feedback loop and the second set of switches is used to sample at a point (V1 and V2) where switch resistances and nonlinear resistances do not matter. This way, the gain error can be reduced while preserving the noise performance of the ADA4896-2/ADA4897-1.

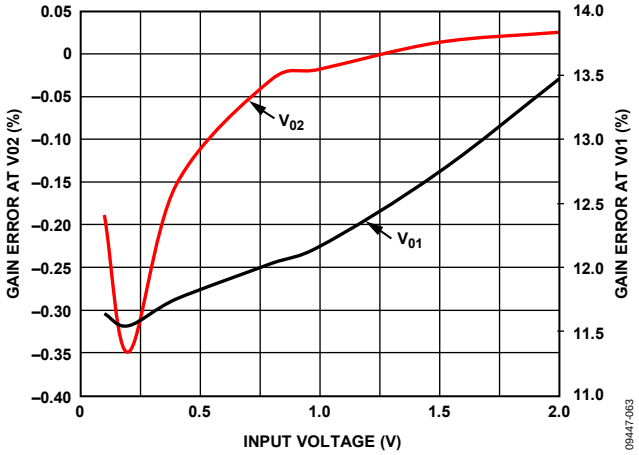


Figure 51. Gain Errors at V_{01} vs. V_{02}

It should be noted that the input bias current of the output buffer can cause problems with the impedance of the S2A and S2B sampling switches. Both sampling switches are not only nonlinear with voltage but with temperature as well. If this is an issue, place the unused switch of the ADG633 in the feedback path of the output buffer, as shown in Figure 50, to balance the bias currents.

The following derivation shows that sampling at V1 yields the desired signal gain without gain error. R_S denotes the switch resistance. V2 can be derived with the same method.

$$V_{01} = V_{IN} \times \left(1 + \frac{R_{F1} + R_{S1}}{R_{G1}}\right) \quad (1)$$

$$V_1 = V_{01} \times \left(\frac{R_{F1} + R_{G1}}{R_{F1} + R_{G1} + R_{S1}}\right) \quad (2)$$

Substituting (1) into (2), the following derivation is obtained

$$V_1 = V_{IN} \times \left(1 + \frac{R_{F1}}{R_{G1}}\right) \quad (3)$$

Figure 51 compares the gain errors when the output signal is sampled at V_{01} vs. V_{02} for a range of dc inputs. Note that sampling at V_{02} reduces the gain error significantly, as predicted in Equation 3. Figure 52 shows the normalized frequency response of the circuit at V_{02}.

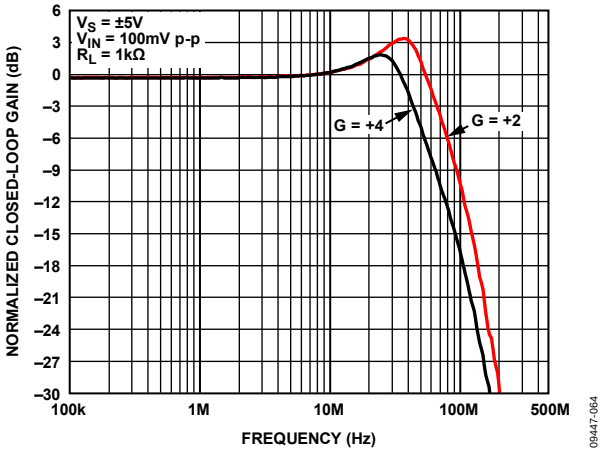


Figure 52. Frequency Response of V_{02}/V_{IN}

MEDICAL ULTRASOUND APPLICATIONS

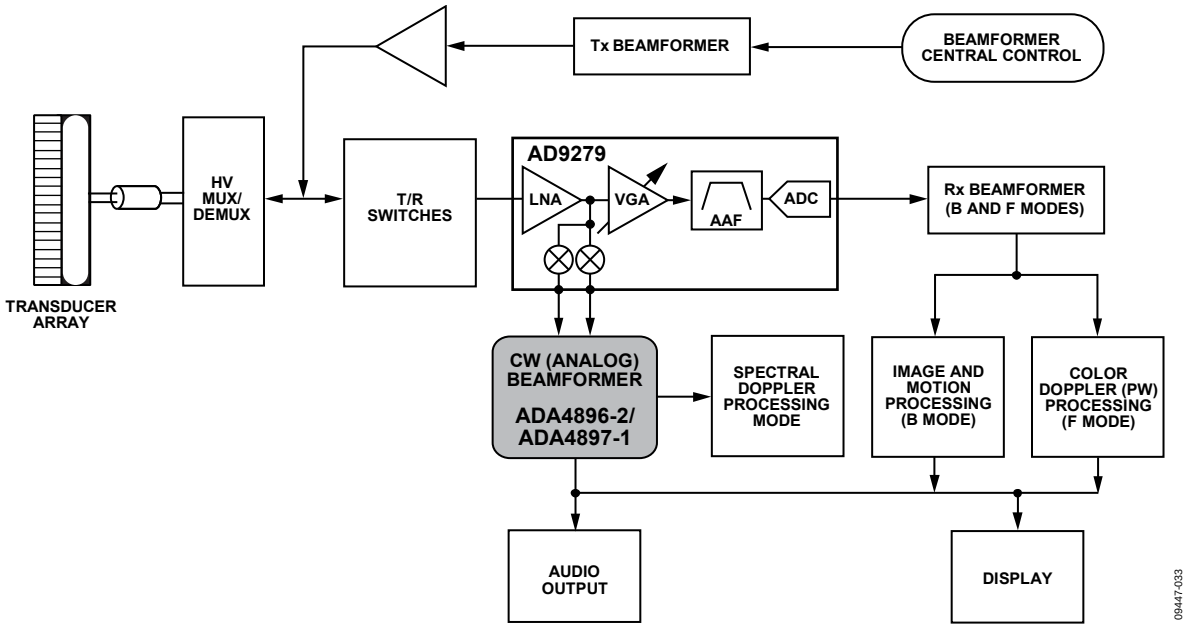


Figure 53. Simplified Ultrasound System Block Diagram

Overview of the Ultrasound System

Medical ultrasound systems are among the most sophisticated signal processing systems in widespread use today. By transmitting acoustic energy into the body and receiving and processing the returning reflections, ultrasound systems can generate images of internal organs and structures, map blood flow and tissue motion, and provide highly accurate blood velocity information. Figure 53 shows a simplified block diagram of an ultrasound system.

The ultrasound system consists of two main operations, the time gain control (TGC) operation and the continuous wave (CW) Doppler operation. The AD9279 integrates the essential components of these two operations into a single IC. It contains eight channels of a variable gain amplifier (VGA) with a low noise preamplifier (LNA), an antialiasing filter (AAF), an analog-to-digital converter (ADC), and an I/Q demodulator with programmable phase rotation. For detailed information about how to use the AD9279 in the ultrasound system, refer to the AD9279 data sheet.

ADA4896-2/ADA4897-1 in the Ultrasound System

The ADA4896-2/ADA4897-1 are used in the CW Doppler path in the ultrasound application after the I/Q demodulators of the AD9279. Doppler signals can be typically between 100 Hz to 100 kHz.The low noise floor, high dynamic range of the ADA4896-2/ADA4897-1 makes them an excellent choice for processing weak Doppler signals.

The rail-to-rail output feature and the high output current drive of the ADA4896-2/ADA4897-1 make them a suitable candidate for the I-to-V converter, summer, and as a ADC driver. Figure 54 shows an interconnection block diagram of all eight channels of the AD9279. Two stages of ADA4896-2 amplifiers are used. The first stage does an I-to-V conversion and filters the high frequency content that results from the demodulation process. The second stage of ADA4896-2 amplifiers is used to sum the output currents of multiple AD9279, to provide gain, and to drive the AD7982, an 18-bit SAR ADC.

The output-referred noise of the CW signal path depends on the LNA gain and the selection of the first stage summing amplifier and the value of R_{FILT}. To determine the output referred noise, it is important to know the active low-pass filter (LPF) values R_A, R_{FILT}, and C_{FILT}, as shown as Figure 54. Typical filter values for all eight channels of a single AD9279 are 100 Ω for R_A, 500 Ω for R_{FILT}, and 2.0 nF for C_{FILT}; these values implement a 100 kHz single-pole LPF.

The gain of the I-to-V converter can be increased by increasing the filter resistor, R_{FILT}. To keep the corner frequency the same, decrease the filter capacitor, C_{FILT}, by the same factor. The factor limiting the magnitude of the gain is the output swing and drive capability of the op amp selected for the I-to-V converter, in this example, the ADA4896-2/ADA4897-1. Because any amplifier has limited drive capability, there is a finite number of channels that can be summed.

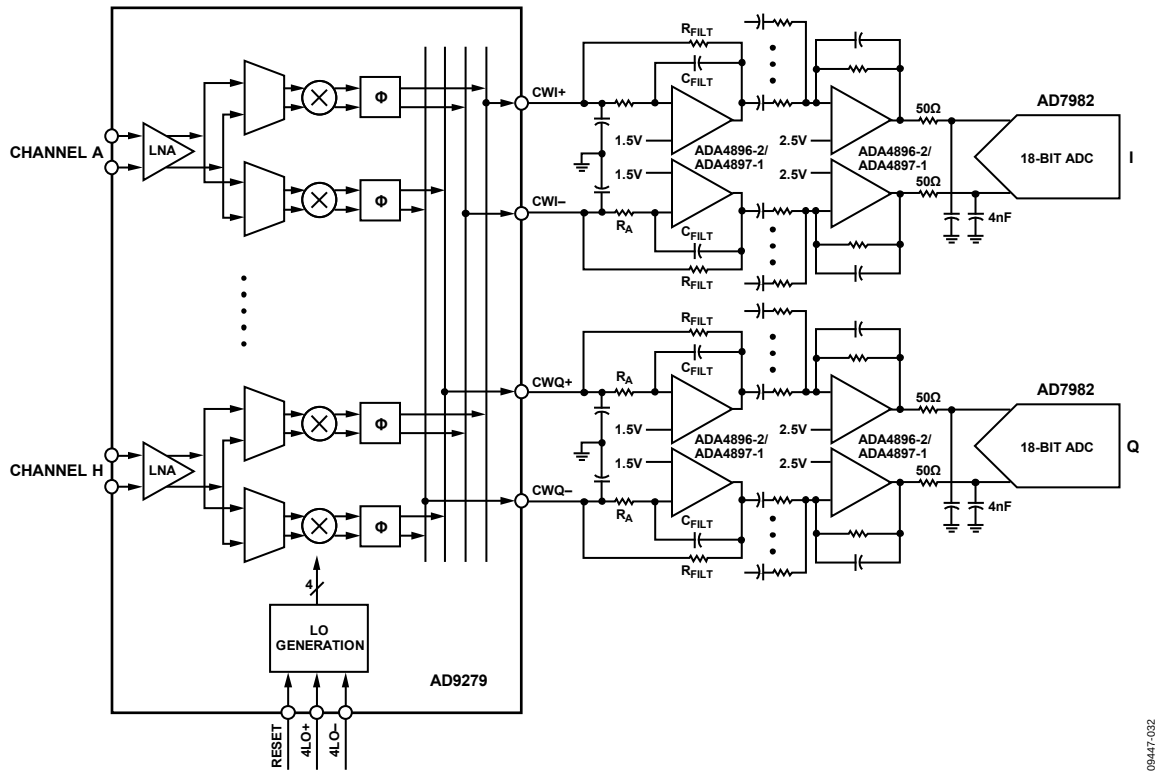


Figure 54. Using the ADA4896-2/ADA4897-1 as Filters, I-to-V Converters, Current Summers, and ADC Drivers After the I/Q Outputs of the AD9279

LAYOUT CONSIDERATIONS

To ensure optimal performance, careful and deliberate attention must be paid to the board layout, signal routing, power supply bypassing, and grounding.

GROUND PLANE

It is important to avoid ground in the areas under and around the input and output of the ADA4896-2/ADA4897-1. Stray capacitance created between the ground plane and the input and output pads of a device are detrimental to high speed amplifier performance. Stray capacitance at the inverting input, along with the amplifier input capacitance, lowers the phase margin and can cause instability. Stray capacitance at the output creates a pole in the feedback loop. This can reduce phase margin and can cause the circuit to become unstable.

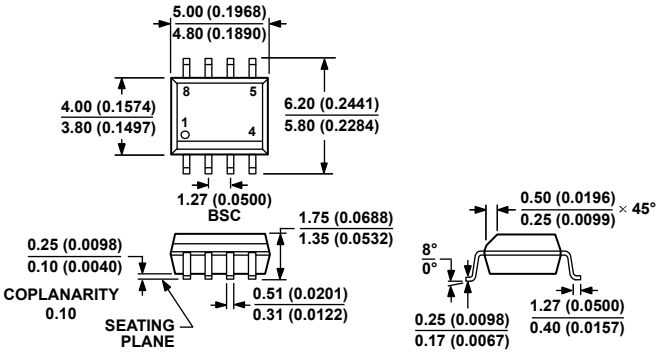
POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect in the performance of the ADA4896-2/ADA4897-1. A parallel connection of capacitors from each of the power supply pins to ground works best. Smaller value capacitors offer better high frequency response, whereas larger value electrolytics offer better low frequency performance. Paralleling different values and sizes of capacitors helps to ensure that the power supply pins are provided a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier. This can be especially important when the amplifier PSR is starting to roll off—the bypass capacitors can help lessen the degradation in PSR performance.

Starting directly at the ADA4896-2/ADA4897-1 power supply pins, the smallest value capacitor should be placed on the same side of the board as the amplifier, and as close as possible to the amplifier power supply pin. The ground end of the capacitor should be connected directly to the ground plane. Keeping the capacitor's distance short but equal from the load is important and can improve distortion performance. This process should be repeated for the next largest value capacitor.

It is recommended that a 0.1 µF ceramic 0508 case be used. The 0508 case size offers low series inductance and excellent high frequency performance. A 10 µF electrolytic capacitor should be placed in parallel with the 0.1 µF capacitor. Depending on the circuit parameters, some enhancement to performance can be realized by adding additional capacitors. Each circuit is different and should be individually analyzed for optimal performance.

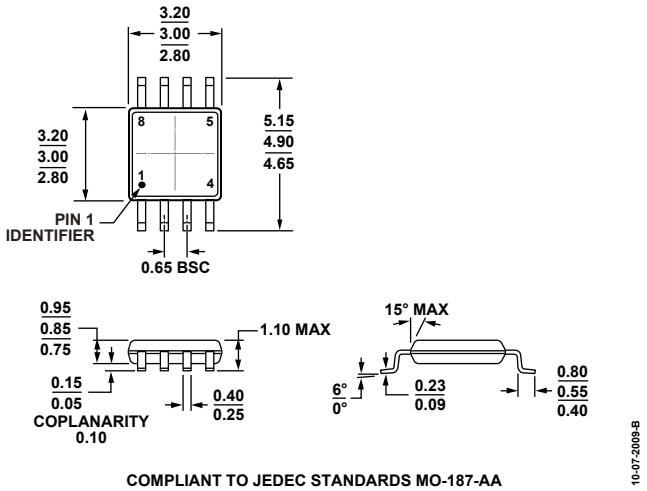
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 56. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

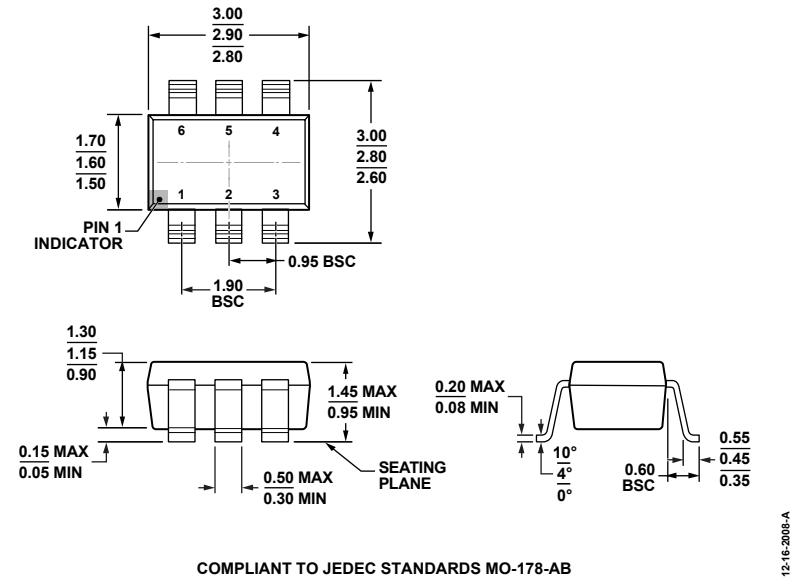


Figure 57. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

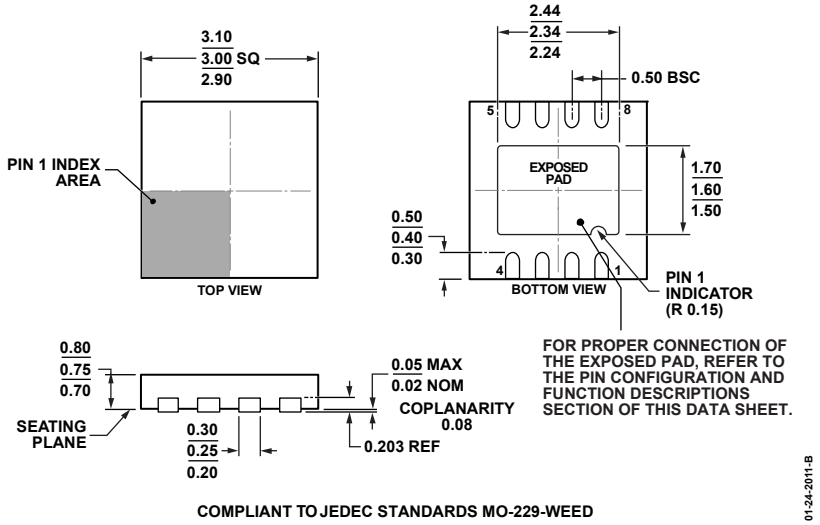


Figure 58. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4896-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	50	H2P
ADA4896-2ARMZ-R7	−40°C to +125°C	8-Lead MSOP	RM-8	1,000	H2P
ADA4896-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP	RM-8	3,000	H2P
ADA4896-2ACPZ-R2	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-11	250	H2P
ADA4896-2ACPZ-R7	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-11	1,500	H2P
ADA4896-2ACPZ-RL	−40°C to +125°C	8-Lead LFCSP_WD	CP-8-11	5,000	H2P
ADA4896-2ACP-EBZ		Evaluation Board for the 8-Lead LFCSP			
ADA4896-2ARM-EBZ		Evaluation Board for the 8-Lead MSOP			
ADA4897-1ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADA4897-1ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000	
ADA4897-1ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	2,500	
ADA4897-1ARJZ-R2	−40°C to +125°C	6-Lead SOT-23	RJ-6	250	H2K
ADA4897-1ARJZ-R7	−40°C to +125°C	6-Lead SOT-23	RJ-6	3,000	H2K
ADA4897-1ARJZ-RL	−40°C to +125°C	6-Lead SOT-23	RJ-6	10,000	H2K
ADA4897-1AR-EBZ		Evaluation Board for the 8-Lead SOIC_N			
ADA4897-1ARJ-EBZ		Evaluation Board for the 6-Lead SOT-23			

[1] Z = RoHS Compliant Part.

NOTES