LF to 4 GHz
High Linearity Y-Mixer

Preliminary Technical Data

ADL5350

FEATURES

Broadband RF, IF, and LO ports
Conversion loss: 6 dB
Noise figure: 6 dB
High input IP3: 26 dBm
High input P_{1dB}: 17 dBm
Low LO drive level
Single-ended design: no need for baluns
Single-supply operation: 3 V @ 10 mA
Miniature 8-lead 3 mm x 2 mm LFCSP package
RoHS compliant

APPLICATIONS

Cellular base station
Point-to-point radio links
RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

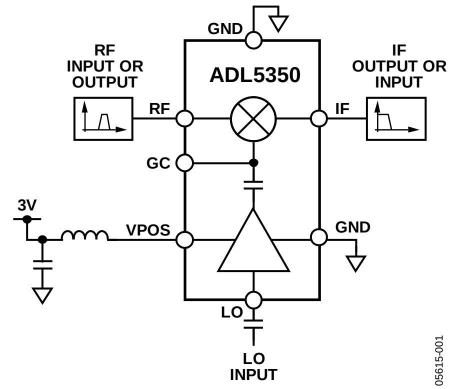

Figure 1.

GENERAL DESCRIPTION

The ADL5350 is a high linearity, up-and-down converting mixer capable of operating over a broad input frequency range. It is well suited for demanding cellular base-station mixer designs that require high sensitivity and efficient blocker immunity. Based on a GaAs pHEMT single-ended mixer architecture, the ADL5350 provides excellent input linearity and low noise figure without the need for a high power level, local oscillator (LO) drive.

In 850 MHz/900 MHz receive applications, the ADL5350 provides a typical conversion loss of only 6 dB. The integrated LO amplifier allows a low LO drive level, typically only 4 dBm for most applications. The input IP3 is typically greater than 25 dBm, with an input compression point of 17 dBm. The high input linearity of the ADL5350 makes the device an excellent mixer for communications systems that require high blocker immunity, such as GSM 850/900 and 800 MHz CDMA2000. At 2 GHz, a slightly greater supply current is required to obtain similar performance.

For low frequency applications, the ADL5350 provides access to the gate contact of the output-mixing device. This allows an external LO coupling capacitor to be applied between the VPOS pin and GC pin, helping to improve the LO drive to the switching device. Using a single 100 pF capacitor allows high performance at the lower LO frequencies.

The single-ended broadband RF/IF port allows the device to be customized for a desired band of operation using simple external filter networks. The LO to RF isolation is based on the LO rejection of the RF port filter network. Greater isolation may be achieved using higher order filter networks as described in the Applications section of this data sheet.

The ADL5350 is fabricated on a GaAs pHEMT high performance IC process. The ADL5350 is available in a 3 mm × 2 mm 8-lead LFCSP package. It operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. PrC

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SPECIFICATIONS

820 MHz RECEIVE PERFORMANCE

V_S = 3 V, T_A = 25°C, LO power = 4 dBm, re: 50 Ω, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
RF Frequency Range	750	850	975	MHz	
LO Frequency Range	500	780	945	MHz	Low Side LO
IF Frequency Range	30	70	250	MHz	
Conversion Loss		6.3		dB	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz
SSB Noise Figure		5.6		dB	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz
Input Third-Order Intercept		27.6		dBm	f_{RF1} = 819 MHz, f_{RF2} = 821 MHz, f_{LO} = 750 MHz f_{IF} = 70 MHz, each RF tone 0 dBm
Input 1 dB Compression Point		17.8		dBm	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz
LO to IF Leakage		−28		dBc	LO Power = 4 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz
LO to RF Leakage		−16		dBc	LO Power = 4 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz
RF to IF Leakage		−17		dBc	RF Power = 0 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz
IF/2 Spurious		−50		dBc	RF Power = 0 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz
Supply Voltage	2.7	3	5.5	V	
Supply Current		10		mA	LO Power = 4 dBm

1950 MHz RECEIVE PERFORMANCE

V_S = 3 V, T_A = 25°C, LO power = 6 dBm, re: 50 Ω, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions
RF Frequency Range	1800	1950	2050	MHz	
LO Frequency Range	1420	1760	2000	MHz	Low Side LO
IF Frequency Range	50	190	380	MHz	
Conversion Loss		7.2		dB	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz
SSB Noise Figure		6.8		dB	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz
Input Third-Order Intercept		26.6		dBm	f_{RF1} = 1949 MHz, f_{RF2} = 1951 MHz, f_{LO} = 1760 MHz f_{IF} = 190 MHz, each RF tone 0 dBm
Input 1 dB Compression Point		16		dBm	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz
LO to IF Leakage		−12.5		dBc	LO Power = 6 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz
LO to RF Leakage		−10.5		dBc	LO Power = 6 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz
RF to IF Leakage		−10		dBc	RF Power = 0 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz
IF/2 Spurious		−54		dBc	RF Power = 0 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz
Supply Voltage	2.7	3	5.5	V	
Supply Current		24		mA	LO Power = 6 dBm

SPUR TABLES

All spur tables are $N \times f_{RF} - M \times f_{LO}$-mixer spurious products for 0 dBm input power, unless otherwise noted.

450 MHz SPUR TABLE

Table 3.

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
N	**0**	−5.7	−16.2	−25.5	−16.2	−23.9	−22.3	−27.1	−24.7	−27.1	−26.8	−38.6	−30.2	−29.9	−27.2	−29.2	−34.8
	1	−24.9	−5.7	−30.1	−18.8	−25.2	−24.0	−24.3	−37.1	−26.5	−53.1	−32.0	−44.0	−59.3	−46.0	−52.3	−43.3
	2	−47.4	−57.5	−51.1	−60.2	−53.8	−55.2	−52.5	−50.8	−57.7	−51.4	−65.0	−53.1	−63.9	−77.5	−68.7	−75.5
	3	−70.5	−75.3	−70.2	−79.7	−69.5	−76.6	−66.9	−74.5	−73.0	−74.7	−75.5	−71.4	−74.6	−75.3	−75.6	−76.1
	4	−78.4	−73.1	−82.4	−79.3	−79.5	−77.5	−84.5	−77.8	−82.2	−77.6	−88.4	−82.7	−77.9	−72.8	−77.1	−83.6
	5	−82.7	−76.6	−77.1	−89.8	−77.6	−76.1	−79.3	−79.3	−83.1	−81.1	−78.4	−79.6	−80.2	−77.9	−85.6	−79.1
	6	−90.6	−79.2	−82.2	−84.3	−81.2	−96.3	−75.8	−80.1	−80.7	−76.9	−82.5	−74.4	−84.0	−88.9	−89.6	−77.9
	7	−78.9	−74.4	−77.0	−83.2	−80.1	−86.3	−78.9	−87.2	−76.5	−81.5	−82.8	−83.6	−88.7	−73.5	−78.3	−78.4
	8	−77.3	−73.6	−79.0	−80.4	−78.6	−79.6	−83.3	−81.0	−77.4	−70.4	−77.0	−79.7	−90.7	−78.0	−76.2	−77.0
	9	−80.8	−78.5	−76.7	−78.7	−84.8	−80.4	−81.1	−76.9	−80.7	−79.6	−76.0	−91.3	−90.5	−91.4	−96.8	−75.7
	10	−78.9	−77.1	−77.0	−84.0	−87.0	−81.2	−84.4	−90.2	−75.8	−77.5	−90.4	−82.8	−83.0	−87.9	−81.9	−83.1
	11	−77.5	−80.4	−78.7	−86.7	−79.1	−76.4	−85.9	−78.7	−83.4	−85.2	−78.6	−92.3	−80.3	−75.7	−78.3	−75.4
	12	−81.3	−81.6	−81.3	−76.8	−81.5	−78.5	−78.5	−89.7	−74.4	−73.3	−77.0	−78.5	−75.2	−75.4	−91.3	−90.7
	13	−79.9	−81.3	−77.4	−78.7	−79.7	−76.7	−77.7	−85.8	−77.0	−78.9	−84.5	−75.0	−81.0	−78.6	−75.8	−82.0
	14	−82.7	−77.6	−79.6	−76.3	−82.3	−79.8	−79.2	−83.5	−83.5	−91.4	−78.9	−102.8	−75.6	−80.2	−79.5	−87.4
	15	−79.7	−82.9	−79.6	−75.7	−78.8	−78.6	−78.7	−79.8	−77.7	−78.4	−78.7	−80.6	−79.0	−80.4	−87.0	−80.3

820 MHz SPUR TABLE

Table 4.

		M															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
N	**0**	−6.22	−14.7	−12.8	−13.3	−14.2	−30.1	−27.1	−20.4	−20.2	−22.1	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
	1	−18.8	−6.22	−33	−20.3	−21.4	−44.5	−38.5	−43.1	−39	−31.3	−33.1	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
	2	−44.6	−71.6	−50	−64.8	−51.7	−53.7	−60.1	−64.3	−74.8	−61.5	−56.8	−55.1	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
	3	−73.4	−76.8	−69.8	−72.8	−75.5	−79.6	−97.5	−72.3	−79.5	−84.4	−77.8	−74.9	−74.5	N.M.[1]	N.M.[1]	N.M.[1]
	4	−78.2	−77.8	−85.8	−91.3	−80.8	−78.2	−80.9	−76.1	−80.3	−79.4	−81.1	−79.3	−78.1	−77.6	N.M.[1]	N.M.[1]
	5	−82.1	−80.8	−85.2	−81.4	−87.1	−79.5	−84.7	−108	−90.2	−84.5	−76.4	−75.1	−80.9	−78.8	−83.3	N.M.[1]
	6	−77.6	−78.6	−80.6	−78.3	−83.2	−70.8	−77.5	−86.8	−84.9	−81.7	−76.7	−81	−79.4	−78.6	−77.1	−79.5
	7	−80.2	−76.6	−83.1	−75.8	−82.4	−78.2	−78.7	−80.7	−83	−76.5	−88.9	−77.7	−77.3	−80.2	−78.9	−78.1
	8	−83.5	−80.6	−81.7	−79	−84.1	−78.4	−79.5	−86.3	−79	−76.1	−86.7	−79.5	−88.8	−73.9	−79.7	−77.4
	9	N.M.[1]	−78.7	−76.3	−78.1	−82.6	−78.2	−78.5	−87.7	−82.1	−76.7	−94.1	−81.2	−87.5	−80.3	−81.9	−74.9
	10	N.M.[1]	N.M.[1]	−78.7	−78.4	−80.8	−75.4	−76.6	−86	−84	−81.2	−75.5	−72.5	−78.1	−77.1	−81.8	−78.5
	11	N.M.[1]	N.M.[1]	N.M.[1]	−79	−76.7	−81.5	−79.1	−78.2	−76.1	−83	−75	−77.8	−84.1	−79.1	−79.1	−84.2
	12	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−76.4	−78.8	−77	−79.4	−81.8	−78.6	−82.8	−79.3	−76.8	−75.8	−82.2	−81.2
	13	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−82	−77.7	−80.8	−79.8	−76.6	−79.3	−82.1	−94.9	−74.6	−83.3	−75.9
	14	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−84.2	−78	−81.7	−80.3	−79.3	−77.7	−75.8	−86.9	−77.3	−77
	15	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−77	−79.5	−82.2	−80.7	−75.3	−76.1	−79.7	−78.6

[1] N.M. indicates that a frequency was not measured. N.M. spurs are either less than −100 dBm or correspond to a frequency greater than 5995 MHz.

1950 MHz SPUR TABLE

Table 5.

	M															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	−7.8	−2.08	−16.6	−31.7	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
1	−9.6	−7.81	−36.2	−27.2	−41.1	−28	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
2	−54.7	−74.9	−54	−62	−58.5	−78.6	−57.2	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
3	−81.1	−78.6	−78.7	−85.4	−82.1	−75.6	−79.6	−79.4	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
4	N.M.[1]	−78	−83.8	−86.4	−84.1	−79.2	−77.5	−77.2	−81.9	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
5	N.M.[1]	N.M.[1]	−73.9	−82.8	−82.3	−87.8	−80.1	−74.7	−79.3	−82.1	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
6	N.M.[1]	N.M.[1]	N.M.[1]	−80.1	−82.1	−86.7	−83.4	−80.7	−88.2	−79.5	−86.3	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
7	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−79	−80.6	−80	−76.5	−81.4	−81.8	−75.2	−77.4	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]
8	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−79.6	−83.2	−81.5	−81.5	−85.5	−80.9	−79.3	−79.5	N.M.[1]	N.M.[1]	N.M.[1]
9	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−83.7	−89	−83.1	−79.7	−80.6	−81	−82.9	−78.7	N.M.[1]	N.M.[1]
10	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−80.9	−76.4	−82.7	−79.2	−78.8	−77.9	−80.7	−79.6
11	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−77.8	−81.8	−79.7	−88.3	−73.9	−80.9	−79.5
12	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−79.6	−78.7	−77.6	−87.1	−86.6	−76.7
13	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−74.4	−81.6	−83	−82.9	−80.7
14	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−78.9	−82	−74.6	−80.4
15	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	N.M.[1]	−78.7	−73.1	−78.1

[1] N.M. indicates that a frequency was not measured. N.M. spurs are either less than −100 dBm or correspond to a frequency greater than 5995 MHz.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Supply Voltage, V_S	6.0 V
RF Input Level	20 dBm
LO Input Level	20 dBm
Internal Power Dissipation	324 mW
θ_{JA}	154.3 °C/W
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

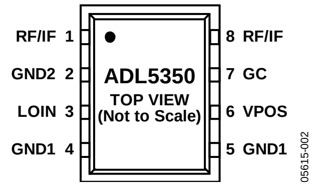

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 8	RF/IF	RF and IF Input/Output Ports. These nodes are internally tied together. RF and IF port separation is achieved using external tuning networks.
2	GND2	Device Common (DC Ground) for RFIF Switching Circuitry.
3	LOIN	LO Input, AC-Coupled.
4, 5	GND1	Device Common (DC Ground) for LO Buffer Circuitry.
6	VPOS	Positive Supply Voltage for the Drain of the LO Buffer. A series RF choke is needed on the supply line to provide proper ac-loading of the LO buffer amplifier.
7	GC	Gate Contact of Mixing Device. Typically not connected for high frequency mixing. Connecting capacitor between GC and VPOS permits low frequency applications.

TYPICAL PERFORMANCE CHARACTERISTICS

820 MHz CHARACTERISTICS

V_{POS} = 3 V, RF Frequency = 820 MHz, IF Frequency = 70 MHz, RF Level = −10 dBm, LO Level = 4 dBm, Temperature = 25°C, unless otherwise noted.

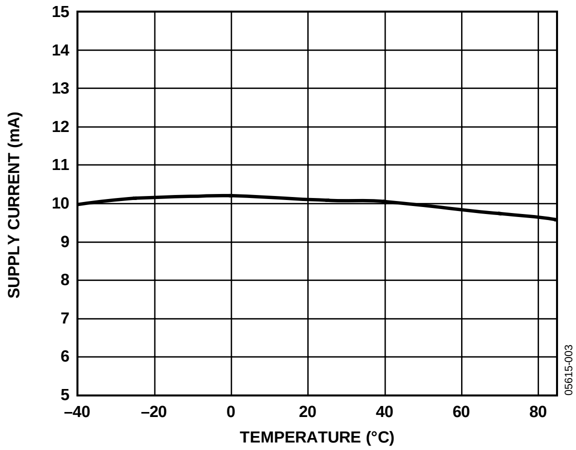

Figure 3. Current vs. Temperature

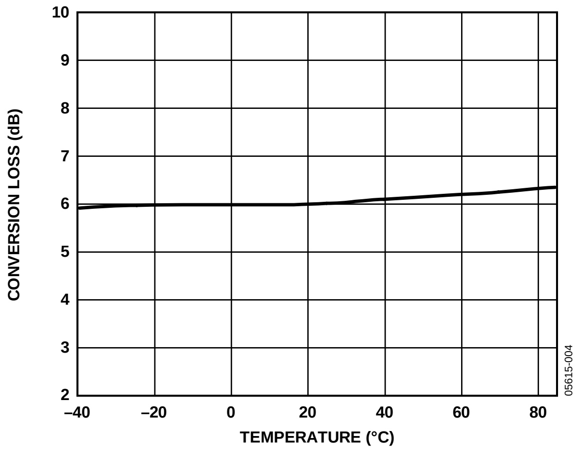

Figure 4. Conversion Loss vs. Temperature

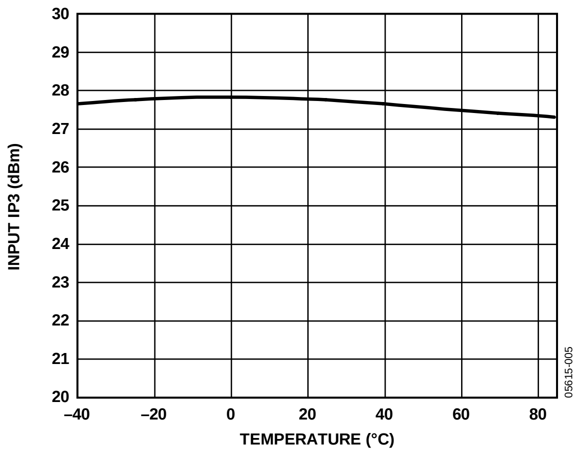

Figure 5. IIP3 vs. Temperature

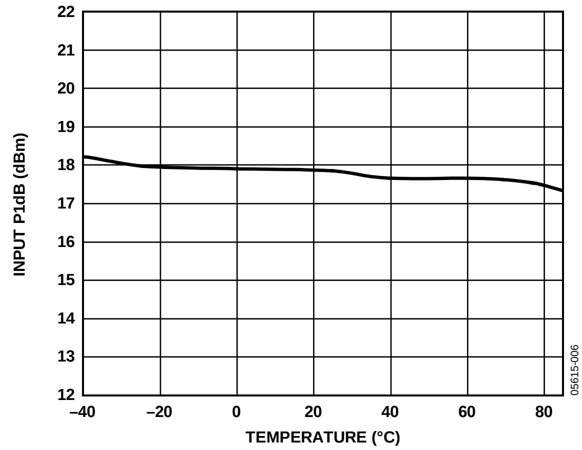

Figure 6. Input Compression vs. Temperature

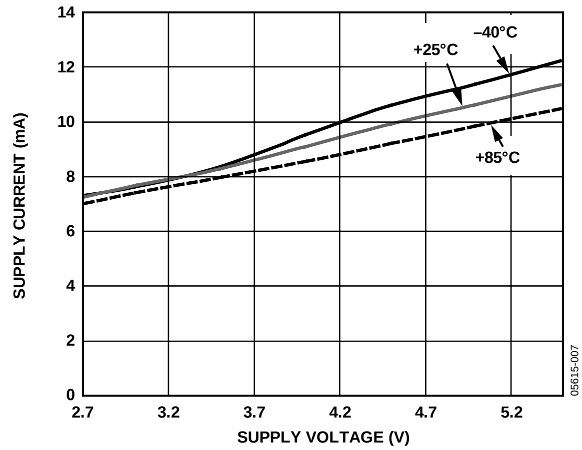

Figure 7. Current vs. VPOS

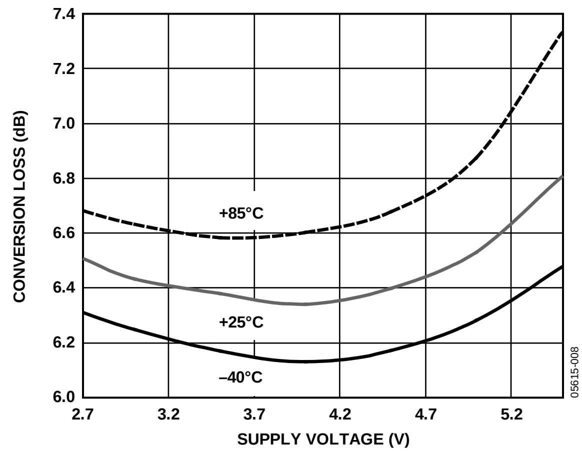

Figure 8. Conversion Loss vs. VPOS

820 MHz CHARACTERISTICS

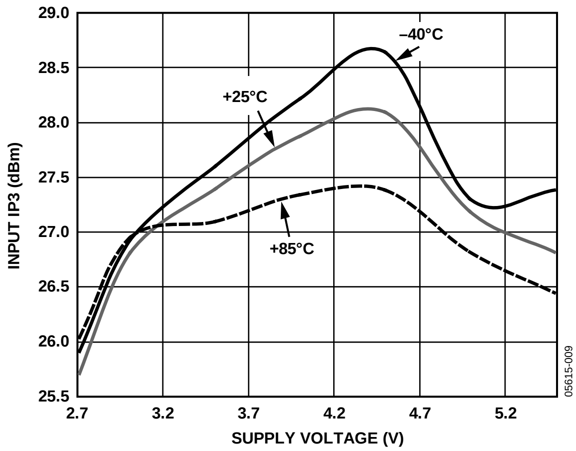

Figure 9. IIP3 vs. VPOS

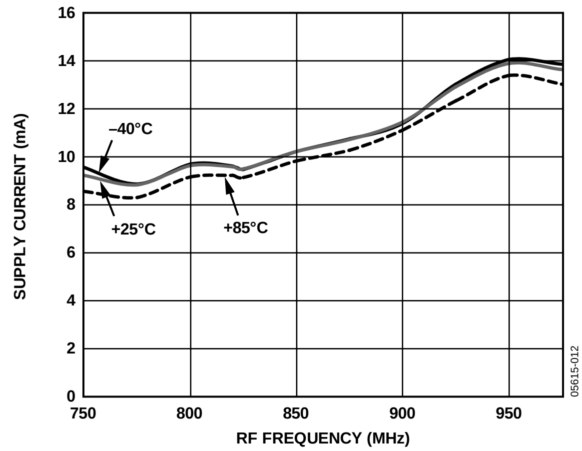

Figure 12. Current vs. RF Frequency

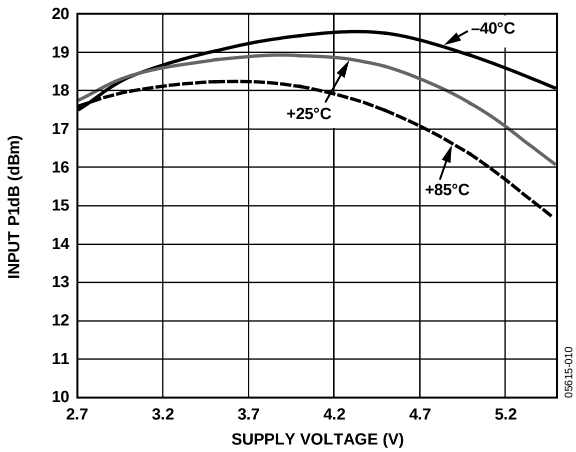

Figure 10. Input Compression vs. VPOS

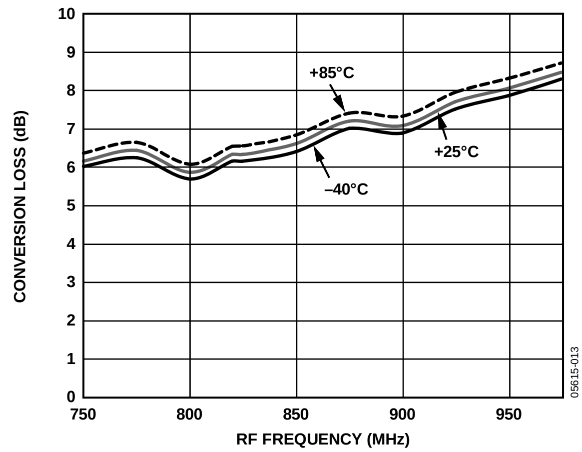

Figure 13. Conversion Loss vs. RF Frequency

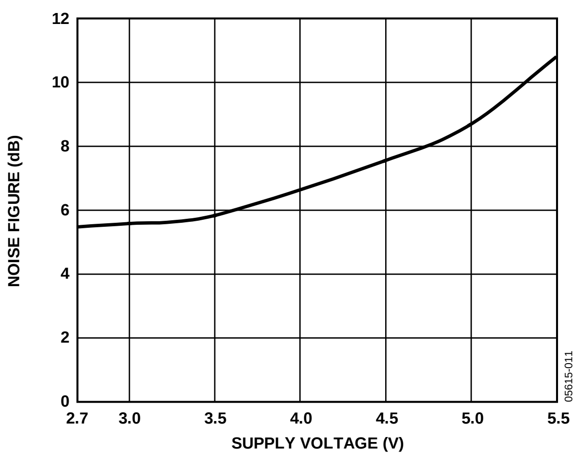

Figure 11. Noise Figure vs. VPOS

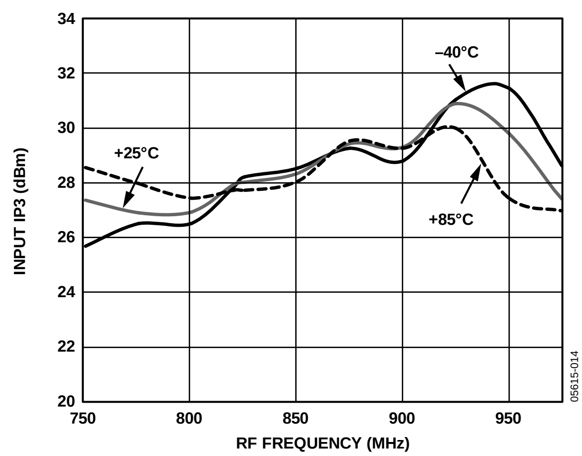

Figure 14. IIP3 vs. RF Frequency

820 MHz CHARACTERISTICS

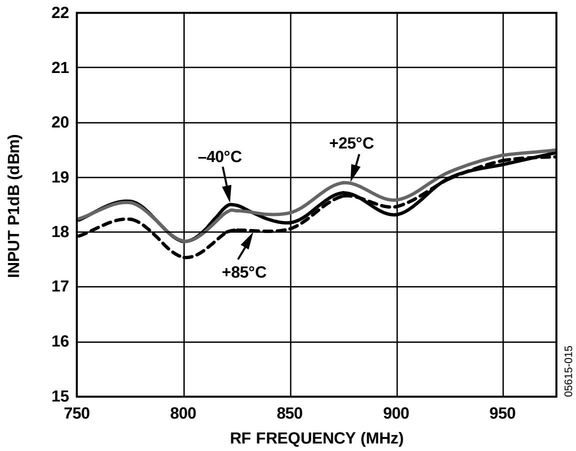

Figure 15. Input Compression vs. RF Frequency

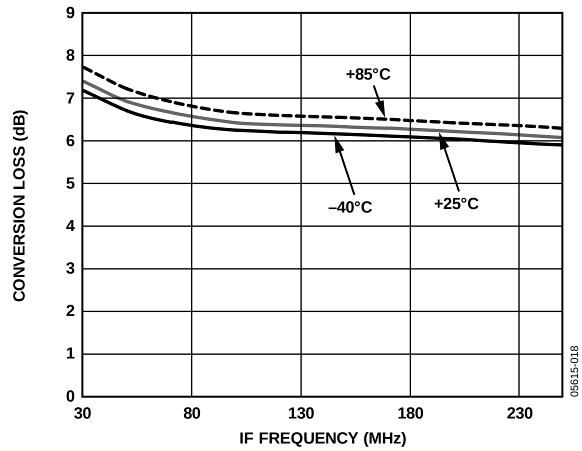

Figure 18. Conversion Loss vs. IF Frequency

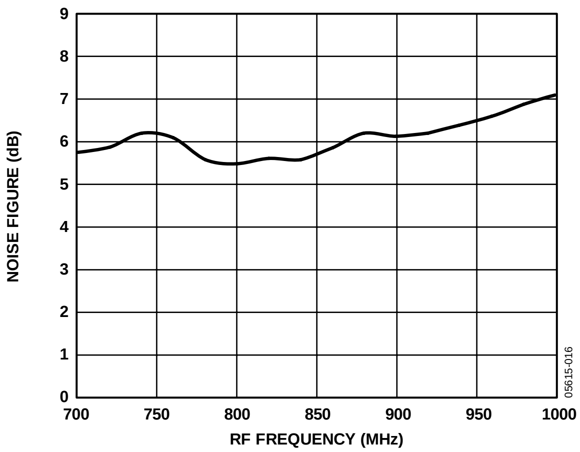

Figure 16. Noise Figure vs. RF Frequency

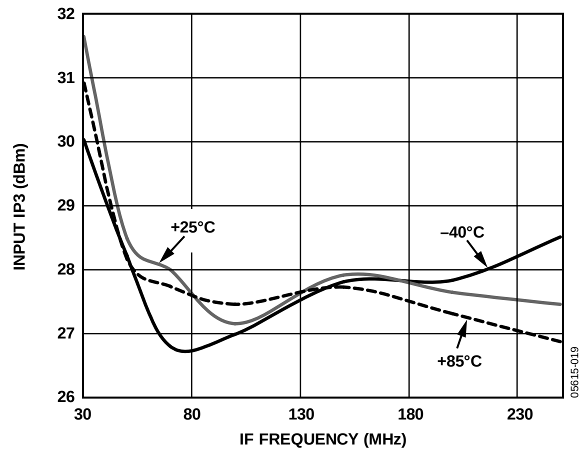

Figure 19. IIP3 vs. IF Frequency

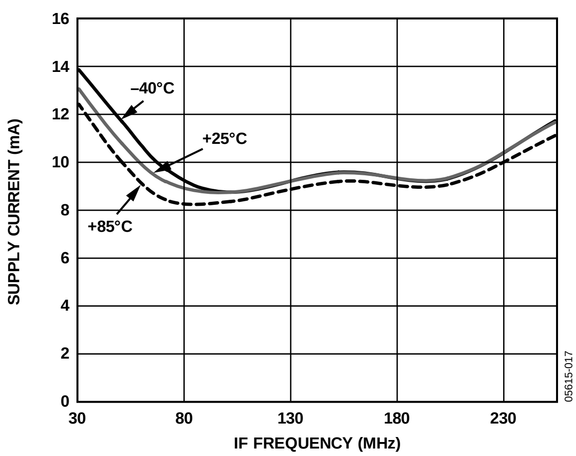

Figure 17. Current vs. IF Frequency

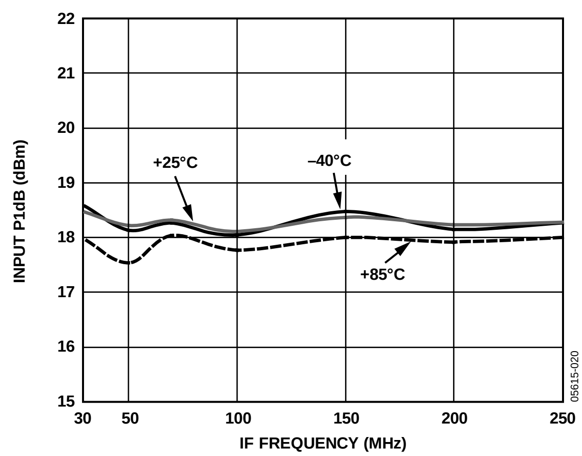

Figure 20. Input Compression vs. IF Frequency

820 MHz CHARACTERISTICS

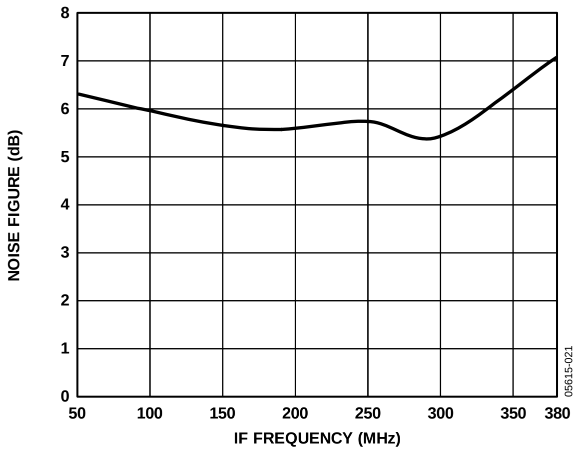

Figure 21. Noise Figure vs. IF Frequency

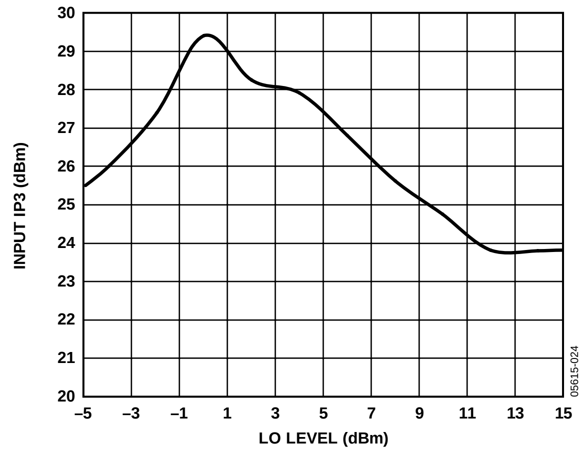

Figure 24. IIP3 vs. LO Level

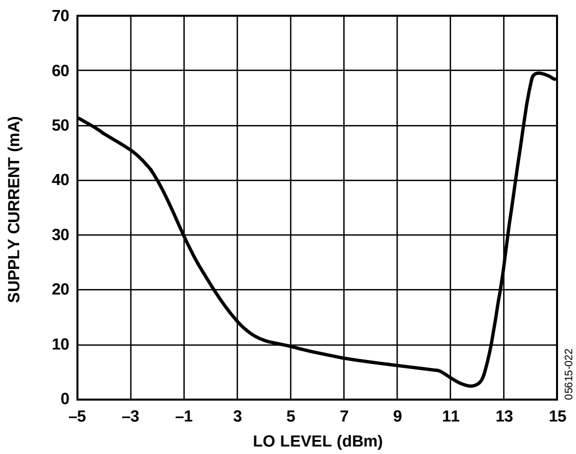

Figure 22. Current vs. LO Level

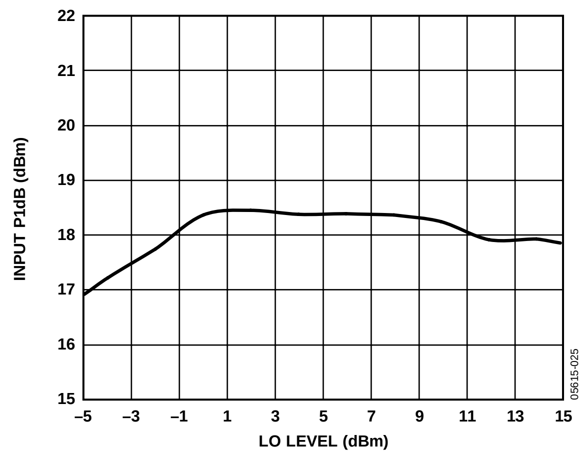

Figure 25. Input Compression vs. LO Level

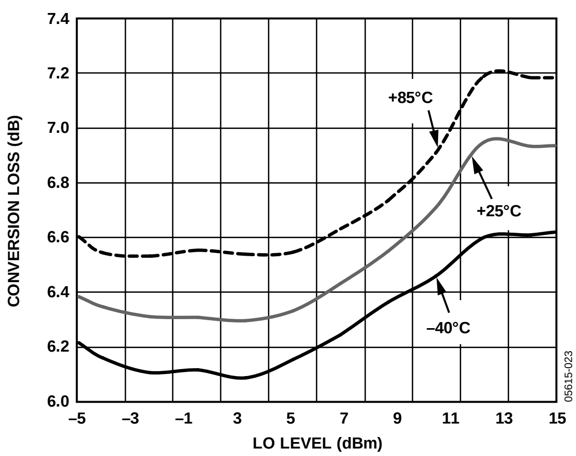

Figure 23. Conversion Loss vs. LO Level

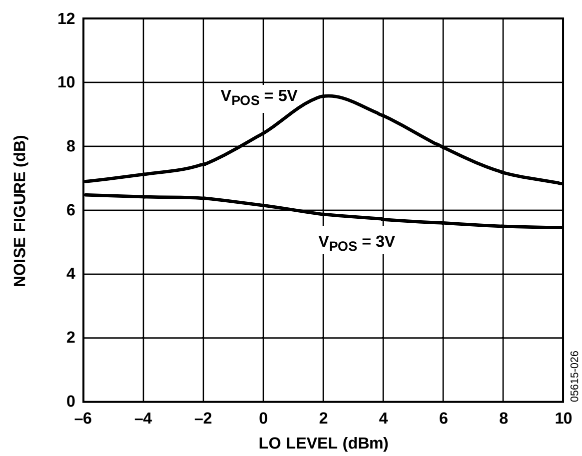

Figure 26. Noise Figure vs. LO Level

820 MHz CHARACTERISTICS

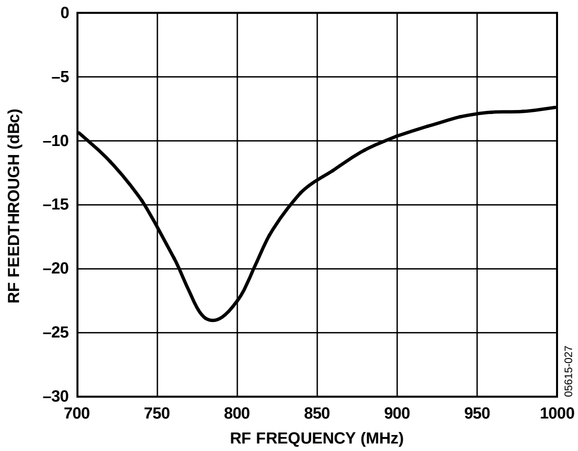

Figure 27. RF to IF Feedthrough vs. RF Frequency

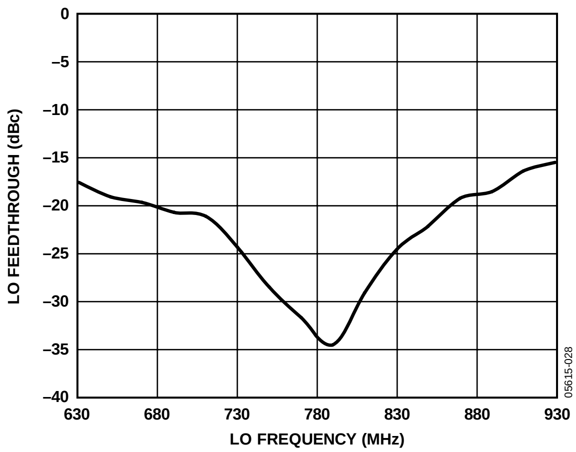

Figure 28. LO to IF Feedthrough vs. LO Frequency

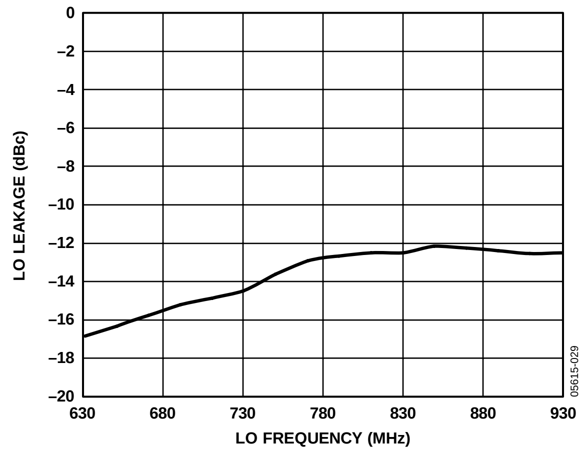

Figure 29. LO to RF Leakage vs. LO Frequency

1950 MHz CHARACTERISTICS

V_{POS} = 3 V, RF Frequency = 1950 MHz, IF Frequency = 190 MHz, RF Level = −10 dBm, LO Level = 6 dBm, Temperature = 25°C, unless otherwise noted.

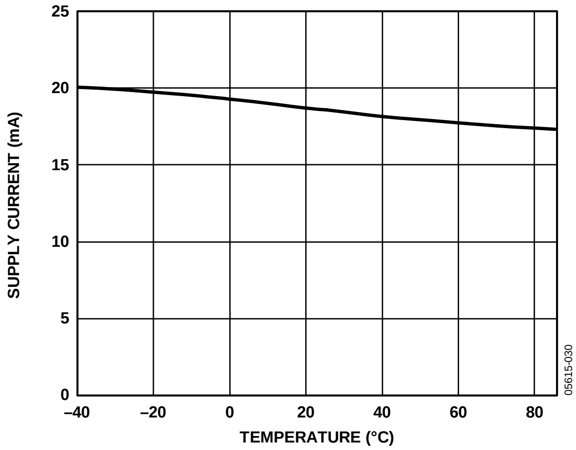

Figure 30. Current vs. Temperature

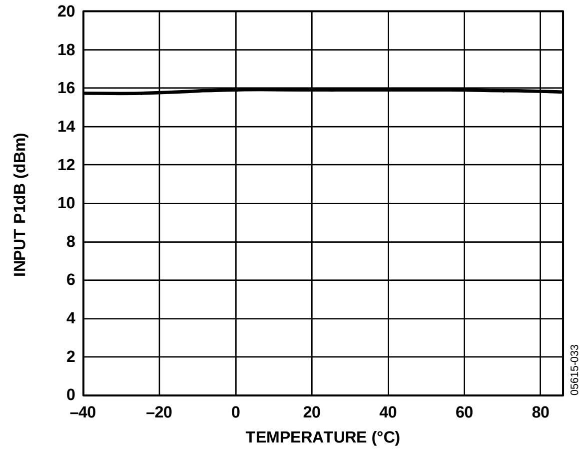

Figure 33. Input Compression vs. Temperature

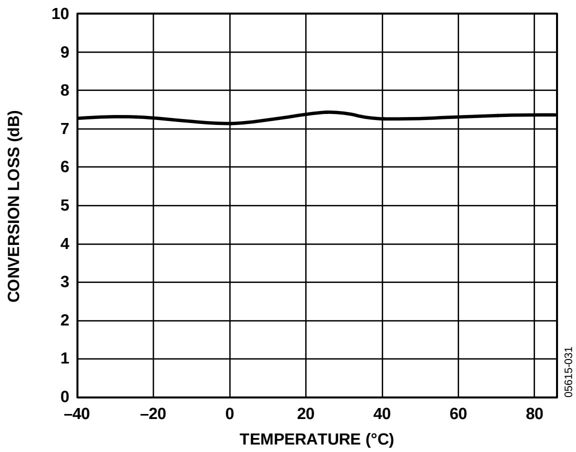

Figure 31. Conversion Loss vs. Temperature

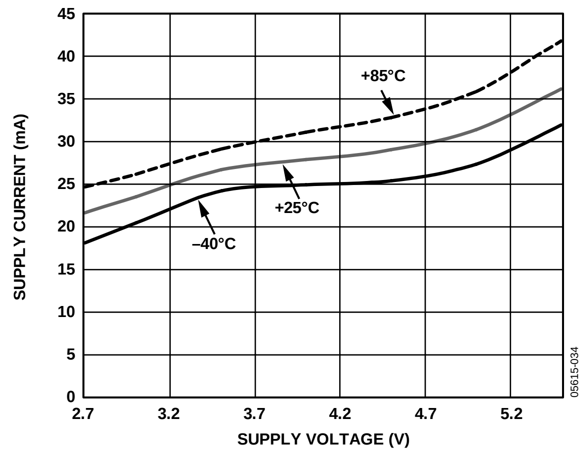

Figure 34. Current vs. VPOS

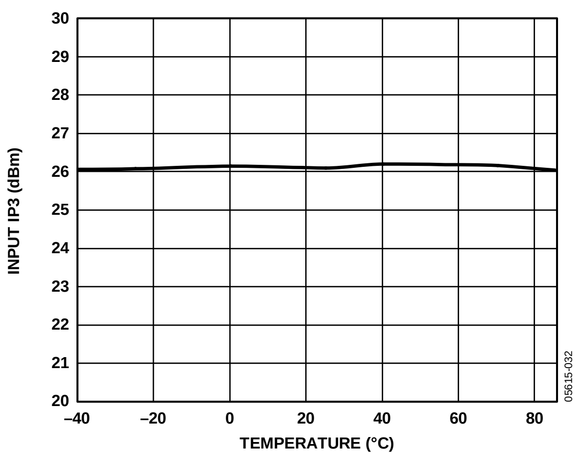

Figure 32. IIP3 vs. Temperature

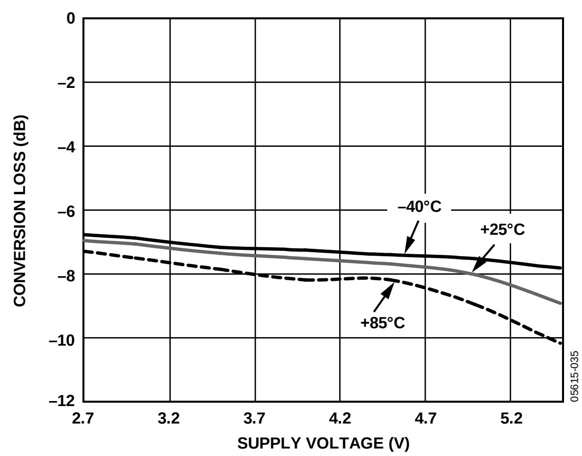

Figure 35. Conversion Loss vs. VPOS

1950 MHz CHARACTERISTICS

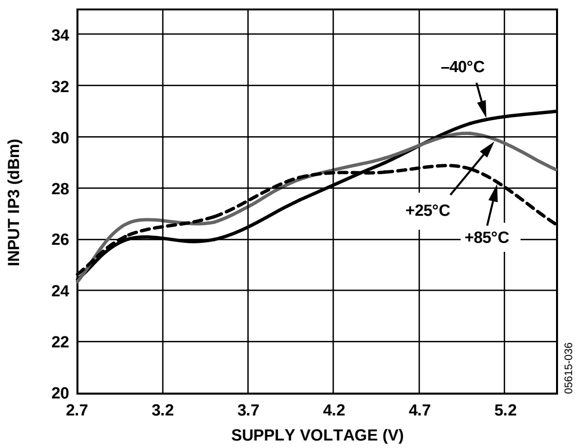

Figure 36. IIP3 vs. VPOS

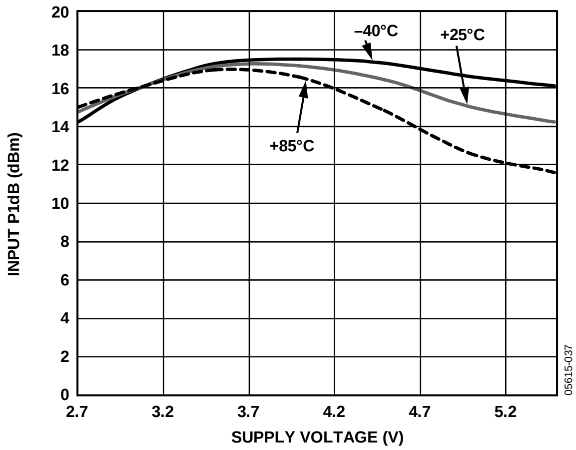

Figure 37. Input Compression vs. VPOS

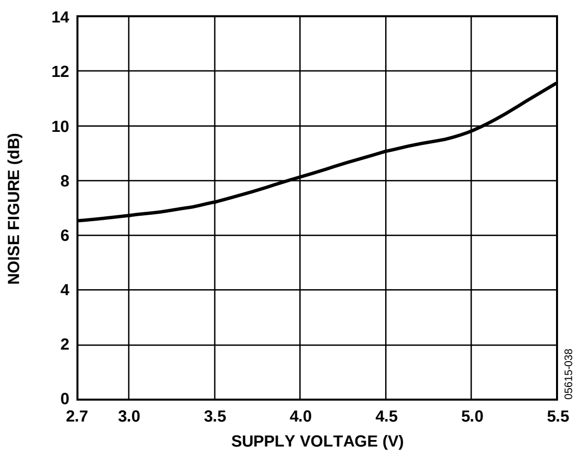

Figure 38. Noise Figure vs. VPOS

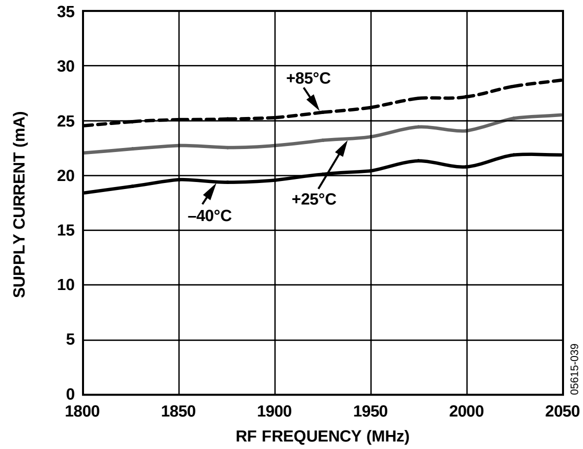

Figure 39. Current vs. RF Frequency

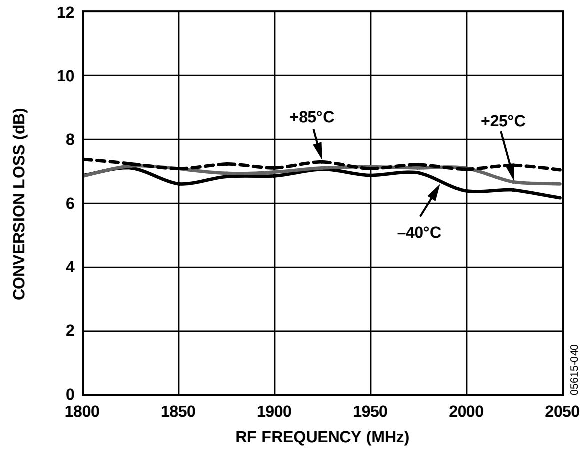

Figure 40. Conversion Loss vs. RF Frequency

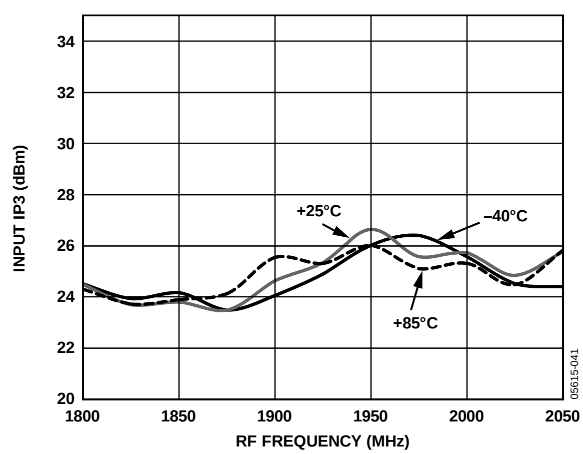

Figure 41. IIP3 vs. RF Frequency

1950 MHz CHARACTERISTICS

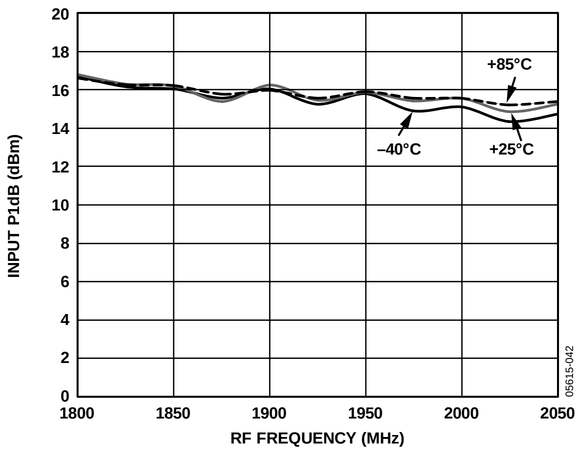

Figure 42. Input Compression vs. RF Frequency

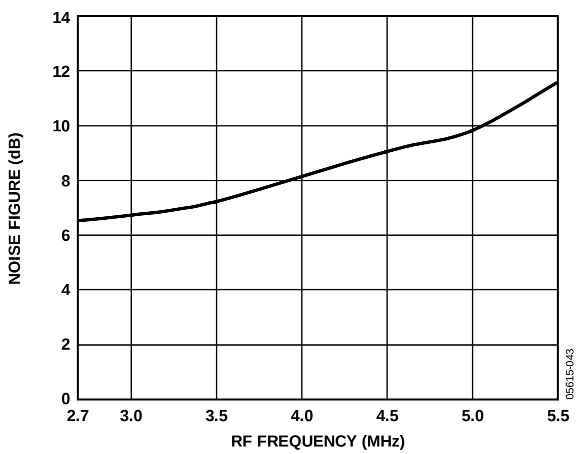

Figure 43. Noise Figure vs. RF Frequency

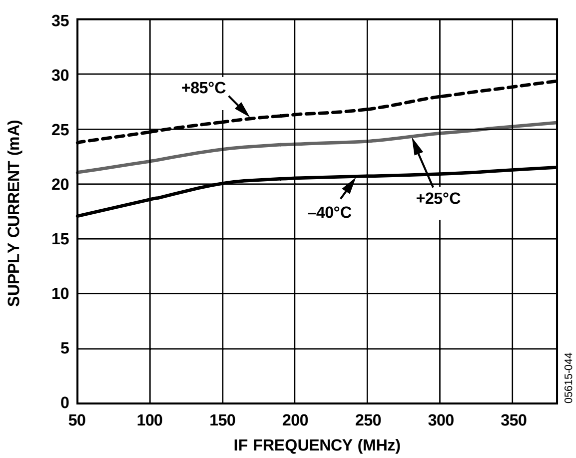

Figure 44. Current vs. IF Frequency

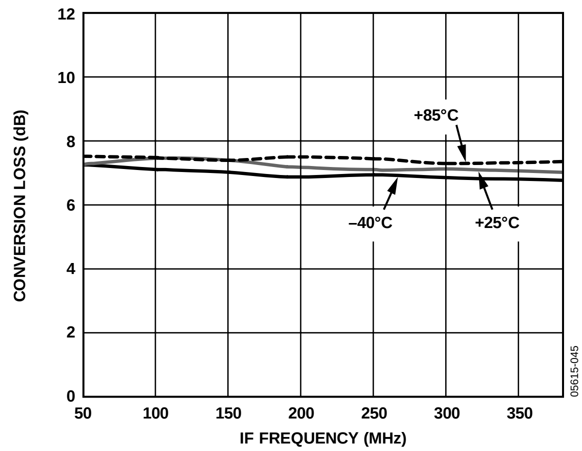

Figure 45. Conversion Loss vs. IF Frequency

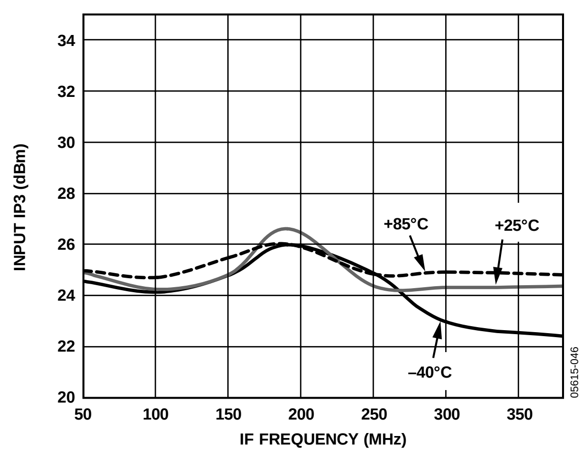

Figure 46. IIP3 vs. IF Frequency

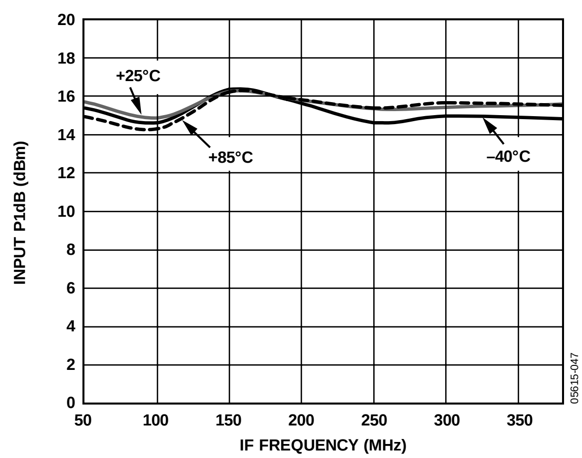

Figure 47. Input Compression vs. IF Frequency

1950 MHz CHARACTERISTICS

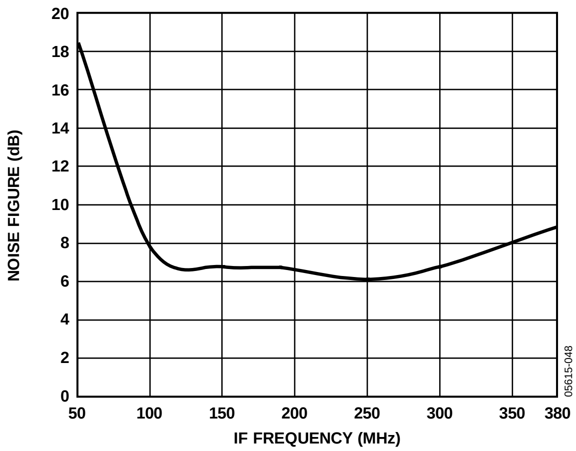

Figure 48. Noise Figure vs. IF Frequency

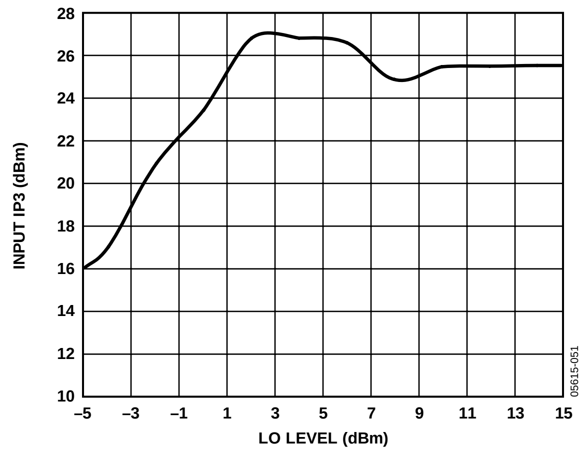

Figure 51. IIP3 vs. LO Level

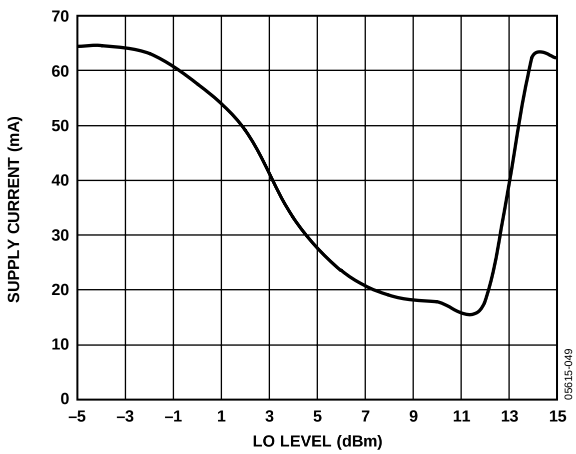

Figure 49. Current vs. LO Level

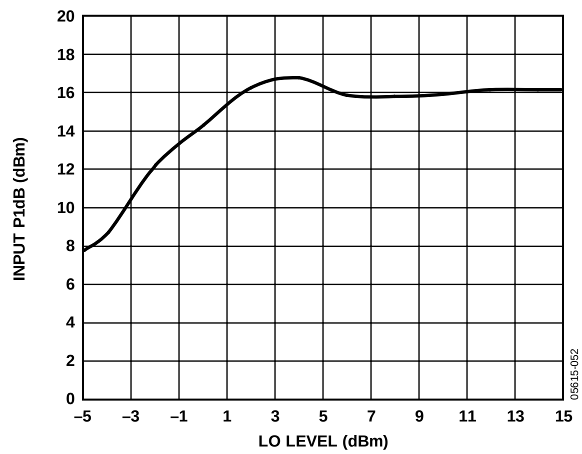

Figure 52. Input Compression vs. LO Level

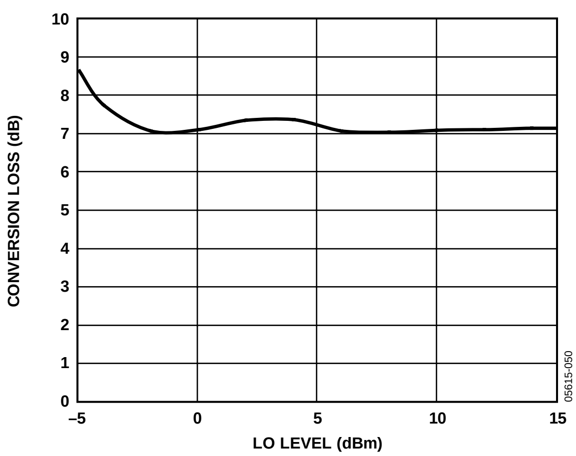

Figure 50. Conversion Loss vs. LO Level

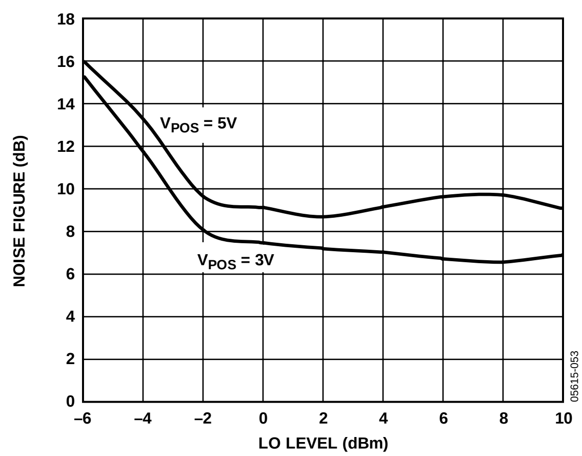

Figure 53. Noise Figure vs. LO Level

1950 MHz CHARACTERISTICS

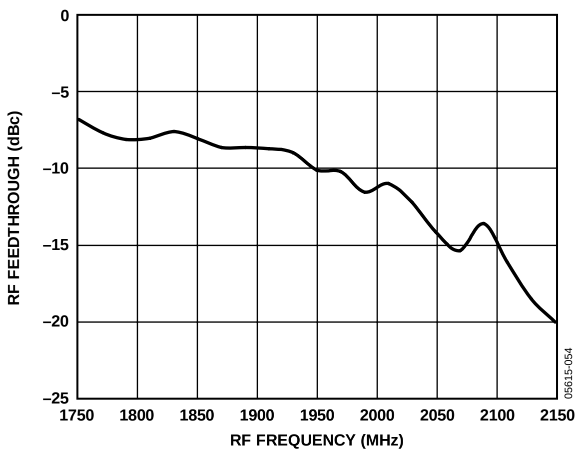

Figure 54. RF to IF Feedthrough vs. RF Frequency

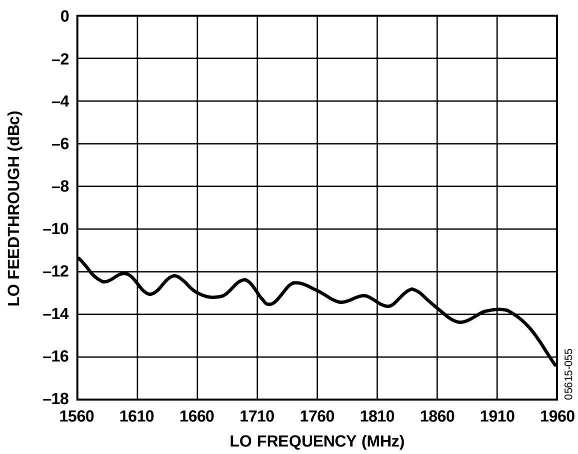

Figure 55. LO to IF Feedthrough vs. LO Frequency

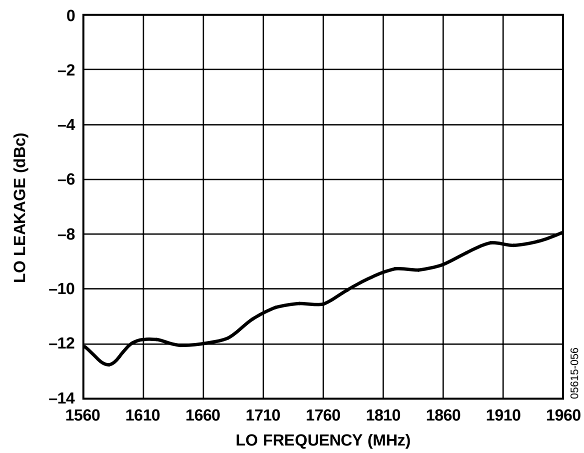

Figure 56. LO to RF Leakage vs. LO Frequency

FUNCTIONAL DESCRIPTION

CIRCUIT DESCRIPTION

The ADL5350 is a GaAs MESFET, single-ended passive mixer with an integrated LO buffer amplifier. The device relies on the varying drain to source channel conductance of a FET junction to modulate an RF signal. A simplified schematic is shown in Figure 57.

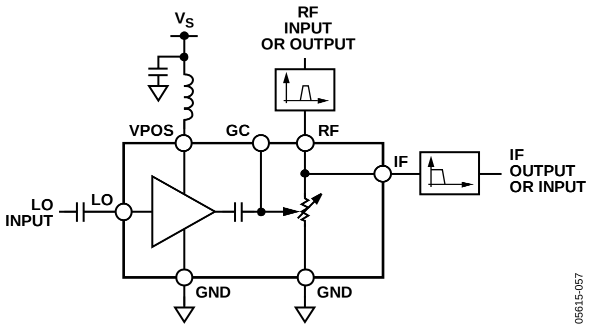

Figure 57. Simplified Schematic

The LO signal is applied to the gate contact of a FET-based buffer amplifier. The buffer amplifier provides sufficient gain of the LO signal to drive the resistive switch. Additionally, feedback circuitry provides the necessary bias to the FET buffer amplifier and RF/IF ports to achieve optimum modulation efficiency for common cellular frequencies. The GC node is the "gate-contact" of the RF/IF port resistive switch. The GC node enables external control of the bias level of the switching FET, allowing the user to override the internal bias generation circuitry, and allow further optimization of the mixer's dynamic performance at frequencies outside of the 800 MHz to 2000 MHz band.

The mixing of RF and LO signals is achieved by switching the channel conductance from the RF/IF port to ground at the rate of the LO. The RF signal is passed through an external band-pass network to help reject image bands and reduce the broadband noise presented to the mixer. The band-limited RF signal is presented to the time-varying load of the RF/IF port, which causes the envelope of the RF signal to be amplitude modulated at the rate of the LO. A filter network applied to the IF port is necessary to reject the RF signal and pass the wanted mixing product. In a down-conversion application, the IF filter network is designed to pass the difference frequency and present an open circuit to the incident RF frequency. Similarly, for an up-conversion application, the filter is designed to pass the sum frequency and reject the incident RF. As a result, the frequency response of the mixer is determined by the response characteristics of the external RF/IF filter networks.

IMPLEMENTATION PROCEDURE

The ADL5350 is a simple single-ended mixer that relies on off-chip circuitry to achieve effective RF dynamic performance. The following steps should be followed to achieve optimum performance (see Figure 58 for component designations):

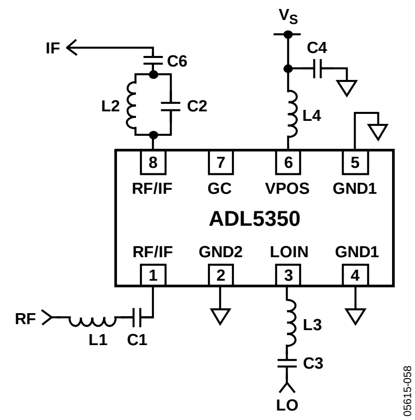

Figure 58. Reference Schematic

1. Tune LO buffer supply inductor for lowest supply current.

To start this procedure, it is necessary to provide an initial guess. Table 8 can be used as a starting point. It is not necessary to terminate or populate the RF and IF port networks to complete this first step. The RFIF pins can be left open while tuning the LO buffer networks.

Table 8. Recommended LO Bias Inductor

Desired LO Frequency	Recommended LO Bias Inductor (L4)[1]
380 MHz	68 nH
750 MHz	24 nH
1000 MHz	18 nH
1750 MHz	3.8 nH
2000 MHz	2.1 nH

[1]The bias inductor should have a self-resonant frequency greater than the intended frequency of operation.

To test the supply current consumption, power up the device and apply the desired LO signal. Next, attempt to increase and decrease the LO frequency. If the current consumption increases as the LO frequency is decreased, then increase the value of L4. If the current consumption decreases as the LO frequency also decreases, then decrease the value of L4. After determining the optimum inductor value, the current consumption should be minimized at the desired LO frequency.

2. Tune the LO port input network for optimum return loss.

Typically, a bandpass network is used to pass the LO signal to the LOIN pin. It is desirable to block high frequency harmonics of the LO from the mixer core. LO harmonics cause higher RF frequency images to be down converted to the desired IF frequency, and result in a sensitivity degradation. If the intended LO source has poor harmonic distortion and spectral purity, it may be necessary to employ a higher order bandpass filter network. Figure 58 illustrates a simple L-C bandpass filter used to pass the fundamental frequency of the LO source. Capacitor C3 is a simple DC block, while the series-inductor (L3), along with the gate-to-source capacitance of the buffer amplifier, form a low-pass network. The native gate input of the LO buffer (FET) presents a rather high input impedance alone. The gate bias is generated internally using feedback that can result in a positive return loss at the intended LO frequency. If a better than −10 dB return loss is desired, it may be necessary to add shunt resistor to ground before the coupling capacitor (C3) to present a lower loading impedance to the LO source .

3. Design the RF and IF filter networks.

Figure 58 depicts simple LC tank filter networks for the IF and RF port interfaces. The RF port LC network is designed to pass the RF input signal. The series LC tank has a resonant frequency at $1/(2\pi\sqrt{LC})$. At resonance, the series reactances cancel, which presents a series short to the RF signal. A parallel LC tank is used on the IF port to reject the RF and LO signals. At resonance, the parallel LC tank presents an open circuit.

It is necessary to accommodate for the board parasitics, finite Q, and self-resonant frequencies of the LC components when designing the RF, IF, and LO filter networks. Table 9 provides suggested values for initial prototyping.

Table 9. Suggested RF, IF, and LO Filter Networks for Low-Side LO Injection

RF Frequency	L1[1]	C1	L2	C2	L3	C3
450 MHz	8.3 nH	10 pF	10 nH	10 pF	10 nH	100 pF
850 MHz	6.8 nH	4.7 pF	4.7 nH	5.6 pF	8.2 nH	100 pF
1950 MHz	1.7 nH	1.5 pF	1.7 nH	1.2 pF	3.5 nH	100 pF
2400 MHz	0.67 nH	1 pF	1.5 nH	0.7pF	3.0 nH	100 pF

[1] The inductor should have a self-resonant frequency greater than the intended frequency of operation. L1 should be a high Q inductor for optimum NF performance.

APPLICATIONS

LOW FREQUENCY APPLICATIONS

Using an external capacitor from the GC pin to VPOS makes it possible to operate the ADL5350 at frequencies below 100 MHz. This capacitor is required because the internal capacitor between the LO buffer and the gate of the device is only 4 pF. This capacitance combined with the gate resistance causes a high-pass filter corner of 80 MHz.

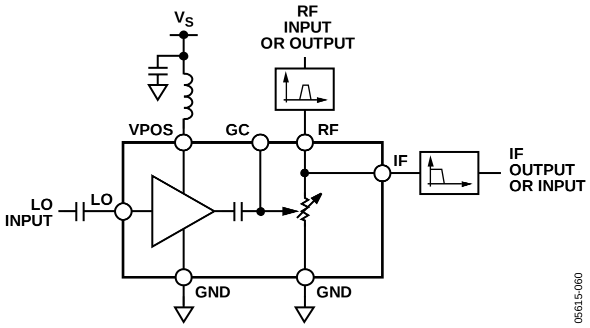

Figure 59. Block Diagram

This high-pass filter corner decreases the LO energy that is reaching the mixer core. Using a 47 pF capacitor between VPOS and GC reduces this corner frequency to 7 MHz.

The circuit in Figure 60 is designed for a RF of 70 MHz and an IF of 10.7 MHz. The LO is at 59.3 MHz (Low Side LO). The series resonant circuit is designed for 70 MHz and the parallel resonant circuit is designed for 65 MHz.

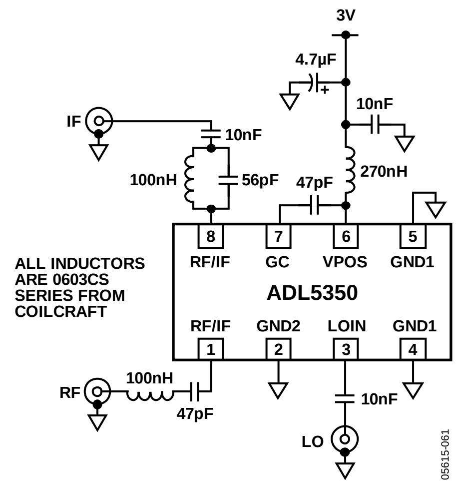

Figure 60. 70 MHz to 10.7 MHz Down-Conversion Schematic

70 MHz RECEIVE PERFORMANCE

V_S = 3 V, T_A = 25°C, LO power = 4 dBm, re: 50 Ω, unless otherwise noted.

Table 10.

Parameter		Unit
RF Frequency	60	MHz
LO Frequency	59.3	MHz
IF Frequency	10.7	MHz
Conversion Loss	6.7	dB
SSB Noise Figure	6.7	dB
Input Third-Order Intercept	27.3	dBm
Supply Voltage	3	V
Supply Current	18	mA

Table 11 shows the spur performance for RF = 70 MHz and LO = 59.3 MHz; RFin = −5 dBm, Loin=4 dBm; all values in dBc referenced to RFin.

Note that higher order spurious components falling in-band do become an issue as the bandwidth of the desired signal increases. Therefore, while operation at IF frequencies as low as 10 MHz is possible, the bandwidth of this signal needs to be taken into consideration.

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Table 11. $N \times f_{RF} - M \times f_{LO}$-Mixer Spurious Products

		M															
		0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	11.0	12.0	13.0	14.0	15.0
N	0.0	−6.8	−30.5	−23.3	−30.5	−28.9	−34.9	−41.1	−45.7	−37.8	−39.7	−42.3	−37.5	−48.8	−40.1	−39.1	−37.4
	1.0	−15.3	−6.8	−18.1	−37.3	−19.8	−22.6	−41.5	−24.2	−26.9	−42.4	−27.7	−30.1	−43.4	−30.2	−32.9	−44.3
	2.0	−51.5	−66.0	−57.8	−57.4	−63.1	−57.8	−55.6	−59.2	−56.3	−55.7	−61.3	−57.1	−55.7	−58.3	−56.8	−57.6
	3.0	−71.4	−78.8	−73.1	−75.1	−80.6	−81.8	−78.3	−78.2	−72.3	−82.3	−77.7	−82.4	−76.3	−73.3	−74.3	−79.2
	4.0	−82.9	−78.6	−81.0	−84.2	−79.7	−77.5	−76.6	−79.0	−74.9	−75.0	−75.8	−76.3	−89.2	−76.7	−87.9	−76.1
	5.0	−76.2	−82.9	−78.6	−75.4	−78.7	−84.9	−77.6	−79.2	−84.5	−85.0	−75.9	−81.3	−74.9	−98.6	−73.6	−90.4
	6.0	−88.6	−74.6	−79.1	−80.2	−77.1	−76.1	−85.8	−76.2	−81.2	−82.9	−89.7	−75.4	−82.9	−85.4	−78.1	−75.9
	7.0	−90.6	−76.7	−79.9	−80.6	−81.0	−83.4	−73.1	−76.8	−77.9	−84.6	−80.0	−78.4	−73.2	−75.2	−79.3	−90.9
	8.0	−81.8	−80.4	−84.6	−84.9	−79.5	−83.1	−80.1	−78.6	−89.9	−78.7	−75.3	−77.0	−81.6	−86.3	−85.0	−77.1
	9.0	−90.2	−78.3	−80.2	−71.9	−73.9	−85.8	−82.2	−86.6	−80.2	−78.7	−79.1	−71.2	−78.8	−76.0	−84.5	−81.8
	10.0	−78.2	−82.1	−80.3	−73.5	−86.6	−86.1	−81.0	−86.0	−78.2	−86.2	−87.1	−83.7	−79.8	−75.0	−83.8	−82.4
	11.0	−77.6	−85.8	−78.4	−85.1	−86.6	−80.1	−79.4	−78.8	−69.3	−82.8	−81.6	−94.2	−81.7	−80.5	−84.1	−77.2
	12.0	−89.4	−90.8	−80.8	−71.7	−73.4	−75.5	−82.2	−76.8	−72.1	−78.0	−76.3	−84.9	−85.6	−78.7	−71.8	−85.1
	13.0	−80.0	−82.5	−79.6	−82.0	−78.9	−78.5	−73.4	−80.4	−84.9	−81.5	−79.4	−79.1	−76.1	−82.8	−77.8	−71.7
	14.0	−86.3	−85.6	−89.2	−85.6	−82.7	−74.4	−88.1	−77.6	−74.4	−79.0	−85.4	−89.1	−88.4	−77.2	−81.1	−80.0
	15.0	−84.4	−81.9	−81.1	−87.9	−77.7	−83.3	−78.4	−81.9	−90.0	−73.3	−84.6	−77.8	−81.7	−81.2	−93.2	−71.4

HIGH FREQUENCY APPLICATIONS

The ADL5350 can be used at extended frequencies with some careful attention to board and component parasitics. Figure 61 is an example of a 2.3 GHz to 2.5 GHz down-conversion using a low-side LO. The performance of this circuit is depicted in Figure 62. Note that the inductor and capacitor values are very small, especially for the RF and IF ports. Above 2.5 GHz, it is necessary to consider alternate solutions to avoid unreasonably small inductor and capacitor values.

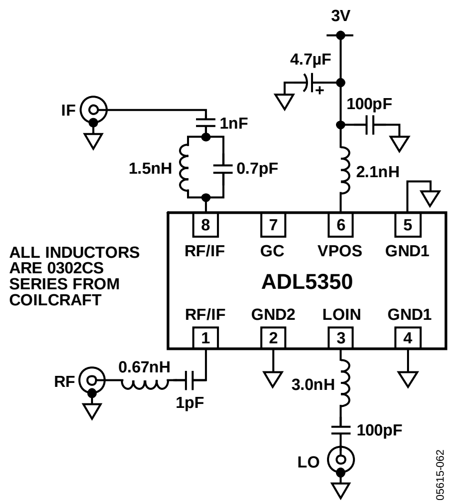

Figure 61. 2.3 GHz to 2.5 GHz Down-Conversion Schematic

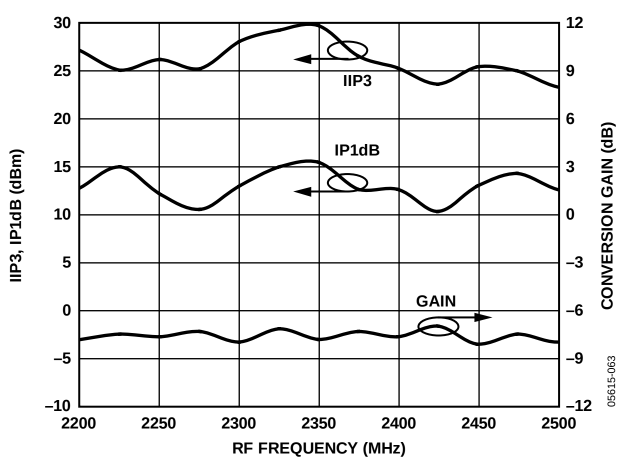

Figure 62. Measured Performance for Circuit in Figure 61 Using Low-Side LO Injection and 374 MHz IF

The typical networks used for cellular applications below 2.5 GHz utilize band-select and band-reject networks on the RF and IF ports. At higher RF frequencies, these networks are not easily realized using lumped element components (discrete Ls and Cs). As a result, it is necessary to consider alternate filter network topologies to allow more reasonable values of inductors and capacitors.

Figure 63 depicts a cross-over filter network approach to provide isolation between the RF and IF ports for a down-converting application. The cross-over network essentially provides a high-pass filter to allow the RF signal to pass to the RF/IF node (Pin 1 and Pin 8), while presenting a low-pass filter, (which is actually band-pass when considering the DC blocking capacitor, C_{AC}). This allows the difference component ($f_{RF} - f_{LO}$) to be passed to the desired IF load.

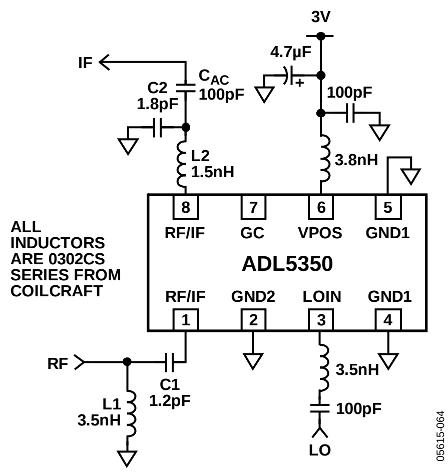

Figure 63. 3.3 GHz to 3.8 GHz Down-Conversion Schematic

When designing the RF and IF port networks, it is important to remember that the networks share a common node (the RF/IF pins). In addition, the opposing network presents some loading impedance to the target network being designed. Classic audio crossover filter design techniques can be applied to help derive component values. However, some caution must be applied when selecting component values. At high RF frequencies, the board parasitics may significantly influence the final optimum inductor and capacitor component selections. Some empirical testing may be necessary to optimize the RF and IF port filter networks. The performance of the circuit depicted in Figure 63 is provided in Figure 64.

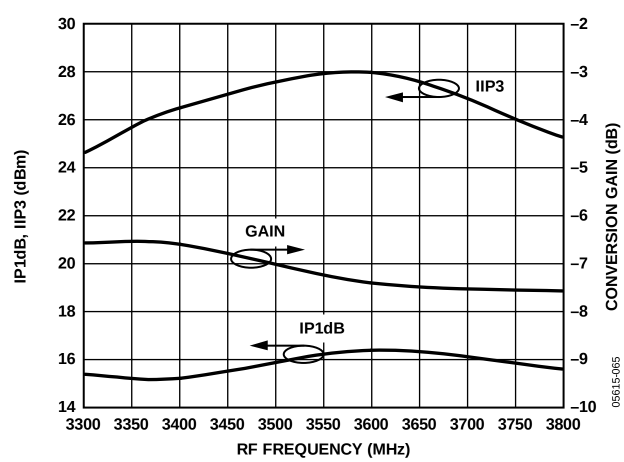

Figure 64. Measured Performance for Circuit in Figure 63

EVALUATION BOARD

An evaluation board is available for the ADL5350. The evaluation board has two halves: a low band designated as Board A, and a high band board designated as Board B. The schematic for the evaluation board is presented in Figure 65.

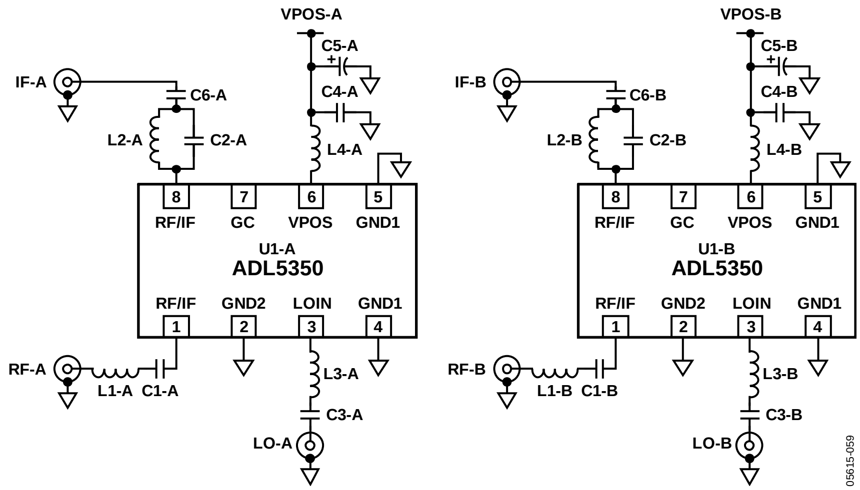

Figure 65. Evaluation Board

Table 12. Evaluation Board Configuration Options

Component	Function	Default Conditions
C4-A, C4-B,	Supply Decoupling. C4-A and C4-B provide local bypassing of the supply.	C4-A = C4-B = 100 pF
C5-A, C5-B	C5-A and C5-B are used to filter the ripple of a noisy supply line. These are not always necessary.	C5-A = C5-B = 4.7 µF
L1-A, L1-B,	RF Input Network.	L1-A = 6.8 nH (0603CS from Coilcraft)
C1-A, C1-B	Designed to provide series resonance at the intended RF frequency.	L1-B = 1.7 nH (0302CS from Coilcraft)
		C1-A = 4.7 pF, C1-B = 1.5 pF
L2-A, L2-B,	IF Output Network.	L2-A = 4.7 nH (0603CS from Coilcraft)
C2-A, C2-B,	Designed to provide parallel resonance at the geometric mean of the RF and LO frequencies.	L2-B = 1.7 nH (0302CS from Coilcraft)
C6-A, C6-B		C2-A = 5.6 pF, C2-B = 1.2 pF
		C6-A = C6-B = 1 nF
L3-A, L3-B,	LO Input Network.	L3-A = 8.2 nH (0603CS from Coilcraft)
C3-A, C3-B	Designed to block DC and optimize LO voltage swing at LOIN.	L3-B = 3.5 nH (0302CS from Coilcraft)
		C3-A = C3-B = 100 pF
L4-A, L4-B	LO Buffer Amp Choke.	L4-A = 24 nH (0603CS from Coilcraft)
	Provides bias and ac loading impedance to LO buffer amp.	L4-B = 3.8 nH (0302CS from Coilcraft)

OUTLINE DIMENSIONS

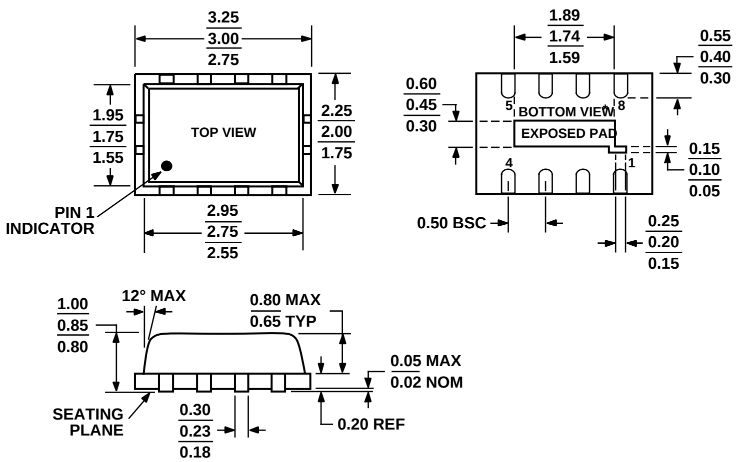

Figure 66. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
2 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5350ACPZ-R2[1]	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-1	Q7	250, Reel
ADL5350ACPZ-R7[1]	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-1	Q7	3000, Reel
ADL5350ACPZ-WP[1]	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP_VD]	CP-8-1	Q7	50, Waffle Pack
ADL5350-EVAL		Evaluation Board			1

[1] Z = Pb-free part.

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