30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifier

ADA4096-2

FEATURES

Input overvoltage protection, 32 V above and below the supply rails
Rail-to-rail input and output swing
Low power: 60 µA per amplifier typical
Unity-gain bandwidth
  800 kHz typical @ V_{SY} = ±15 V
  550 kHz typical @ V_{SY} = ±5 V
  465 kHz typical @ V_{SY} = ±1.5 V
Single-supply operation: 3 V to 30 V
Low offset voltage: 300 µV maximum
High open-loop gain: 120 dB typical
Unity-gain stable
No phase reversal
Qualified for automotive applications

APPLICATIONS

Battery monitoring
Sensor conditioners
Portable power supply control
Portable instrumentation

PIN CONFIGURATIONS

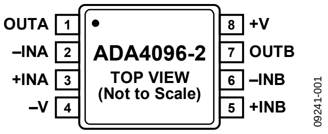

Figure 1. 8-Lead, MSOP (RM-8)

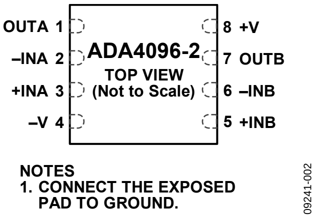

Figure 2. 8-Lead LFCSP (CP-8-10)

GENERAL DESCRIPTION

The ADA4096 operational amplifier features micropower operation and rail-to-rail input and output ranges. The extremely low power requirements and guaranteed operation from 3 V to 30 V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 27 nV/√Hz voltage noise density, recommends them for battery-powered audio applications. Capacitive loads to 200 pF are handled without oscillation.

The ADA4096-2 has overvoltage protection inputs and diodes that allow the voltage input to extend 32 V above and below the supply rails, making this device ideal for robust industrial applications.

The ADA4096-2 features a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up; this is called overvoltage protection, or OVP.

The dual ADA4096-2 is available in 8-lead LFCSP (2 mm × 2 mm) and 8-lead MSOP packages. The ADA409x family is specified over the extended industrial temperature range (–40°C to +125°C) and is part of the growing selection of 30 V, low power op amps from Analog Devices, Inc. (see Table 1).

Table 1. Low Power, 30 V Operational Amplifiers

Op Amp	Rail-to-Rail I/O	PJFET	Low Noise
Dual	ADA4091-2	AD8682	AD8622
Quad	ADA4091-4	AD8684	AD8624

Rev. 0

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REVISION HISTORY

7/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS, $V_{SY} = \pm 1.5$ V

$V_{SY} = \pm 1.5$ V, $V_{CM} = V_{SY}/2$, $T_A = 25°C$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	300	µV
		0°C ≤ T_A ≤ +125°C			450	µV
		−40°C ≤ T_A ≤ +125°C			900	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		1		µV/°C
Input Bias Current	I_B			±10	±15	nA
		−40°C ≤ T_A ≤ +125°C			±16	nA
Input Offset Current	I_{OS}			±0.1	±1.5	nA
		−40°C ≤ T_A ≤ +125°C			±3	nA
Input Voltage Range			−1.5		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to ±1.5 V	63	77		dB
		−40°C ≤ T_A ≤ +125°C	58			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −1.4 V to +1.4 V	92	94		dB
		−40°C ≤ T_A ≤ +125°C	84			dB
		R_L = 2 kΩ, V_O = −1.3 V to +1.3 V	86	92		dB
		−40°C ≤ T_A ≤ +125°C	77			dB
MATCHING CHARACTERISTICS						
Offset Voltage		T_A = 25°C		100	300	µV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	1.48	1.49		V
		−40°C ≤ T_A ≤ +125°C	1.45			V
		R_L = 2 kΩ to GND	1.45	1.46		V
		−40°C to +125°C	1.40			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−1.49	−1.48	V
		−40°C ≤ T_A ≤ +125°C			−1.45	V
		R_L = 2 kΩ to GND		−1.48	−1.47	V
		−40°C ≤ T_A ≤ +125°C			−1.40	V
Short-Circuit Limit	I_{SC}	Source/sink		±10		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		102		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3 V to 36 V	100			dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	$V_O = V_{SY}/2$		40		µA
		−40°C ≤ T_A ≤ +125°C			80	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.25		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		501		kHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		465		kHz
Phase Margin	Φ_M			51		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		97		kHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.7		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

ELECTRICAL SPECIFICATIONS, V_{SY} = ±5 V

V_{SY} = ±5.0 V, V_{CM} = $V_{SY}/2$, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	300	μV
		−40°C ≤ T_A ≤ +125°C			500	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		μV/°C
Input Bias Current	I_B			±10	±15	nA
		−40°C ≤ T_A ≤ +125°C			±19	nA
Input Offset Current	I_{OS}			±1.5	±2	nA
		−40°C ≤ T_A ≤ +125°C			±3	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −5 V to +5 V	73	86		dB
		−40°C ≤ T_A ≤ +125°C	68			dB
		V_{CM} = −3 V to +3 V	91	103		dB
		−40°C ≤ T_A ≤ +125°C	85			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±4.8 V	102	111		dB
		−40°C ≤ T_A ≤ +125°C	99			dB
		R_L = 2 kΩ, V_O = ±4.7 V	94	103		dB
		−40°C ≤ T_A ≤ +125°C	88			dB
MATCHING CHARACTERISTICS						
Offset Voltage		T_A = 25°C		100	300	μV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	4.96	4.97		V
		−40°C ≤ T_A ≤ +125°C	4.95			V
		R_L = 2 kΩ to GND	4.80	4.90		V
		−40°C ≤ T_A ≤ +125°C	4.70			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−4.98	−4.97	V
		−40°C ≤ T_A ≤ +125°C			−4.95	V
		R_L = 2 kΩ to GND		−4.90	−4.80	V
		−40°C ≤ T_A ≤ +125°C			−4.75	V
Short-Circuit Limit	I_{SC}	Source/sink		±10		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		71		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3 V to 36 V	100			dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	V_O = $V_{SY}/2$		47	55	μA
		−40°C ≤ T_A ≤ +125°C			75	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.3		V/μs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		595		kHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		550		kHz
Phase Margin	Φ_M			52		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		114		kHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.7		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

ELECTRICAL SPECIFICATIONS, V_{SY} = ±15 V

V_{SY} = ±15.0 V, V_{CM} = V_{SY}/2, V_O = 0.0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	300	µV
		−40°C ≤ T_A ≤ +125°C			500	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
Input Bias Current	I_B			±3	±10	nA
		−40°C ≤ T_A ≤ +125°C			±15	nA
Input Offset Current	I_{OS}			±0.1	±1.5	nA
		−40°C ≤ T_A ≤ +125°C			±3	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15 V to +15 V	82	95		dB
		−40°C ≤ T_A ≤ +125°C	75			dB
		V_{CM} = −13 V to +13 V	95	107		dB
		−40°C ≤ T_A ≤ +125°C	89			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = ±14.7 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
		R_L = 2 kΩ, V_O = ±11 V	100	112		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Input Capacitance						
Differential Mode	C_{DM}			2.5		pF
Common Mode	C_{CM}			7		pF
MATCHING CHARACTERISTICS						
Offset Voltage		T_A = 25°C		100	300	µV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	14.92	14.94		V
		−40°C ≤ T_A ≤ +125°C	14.90			V
		R_L = 2 kΩ to GND	14.0	14.3		V
		−40°C ≤ T_A ≤ +125°C	12.0			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−14.96	−14.80	V
		−40°C ≤ T_A ≤ +125°C			−14.75	V
		R_L = 2 kΩ to GND		−14.75	−14.65	V
		−40°C ≤ T_A ≤ +125°C			−14.0	V
Short-Circuit Limit	I_{SC}	Source/sink		±10		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3 V to 36 V	100			dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	V_O = V_{SY}/2		60	75	µA
		−40°C ≤ T_A ≤ +125°C			100	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.4		V/µs
Settling Time	t_S	To 0.1%, 10 V step		23.4		µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		786		kHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		800		kHz
Phase Margin	Φ_M			60		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		152		kHz
Channel Separation	CS	f = 1 kHz		100		dB

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.7		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	
Operating Condition	$-V \le V_{IN} \le +V$
Overvoltage Condition[1]	$(-V) - 32\,V \le V_{IN} \le (+V) + 32\,V$
Differential Input Voltage[2]	$\pm V_{SY}$
Input Current	±5 mA
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Performance not guaranteed during overvoltage conditions.
[2] Limit the input current to ±5 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow. The exposed pad is soldered to the application board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-10)	76	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

±1.5 V CHARACTERISTICS

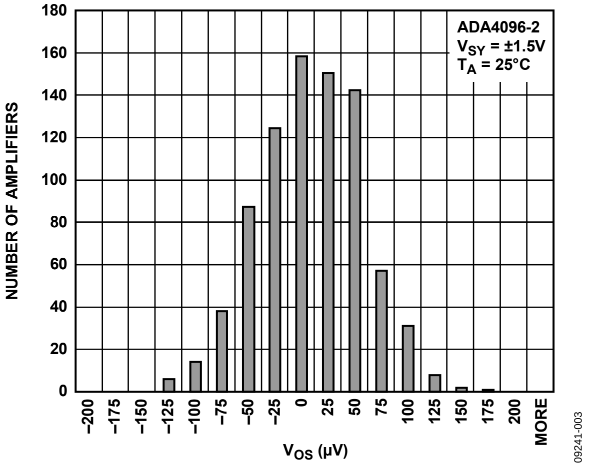


Figure 3. Input Offset Voltage Distribution

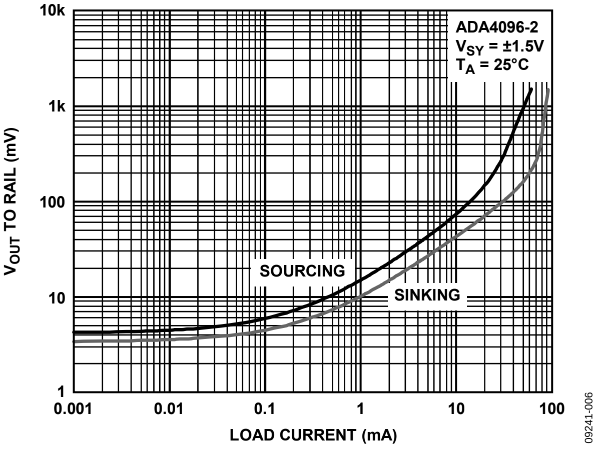


Figure 6. Dropout Voltage vs. Load Current

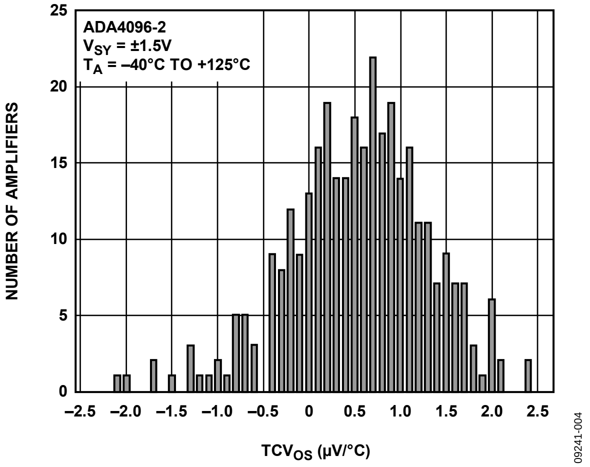


Figure 4. Offset Voltage Drift Distribution

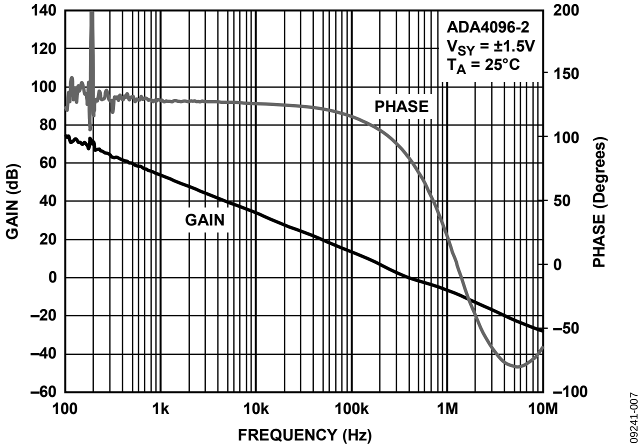


Figure 7. Open-Loop Gain and Phase vs. Frequency

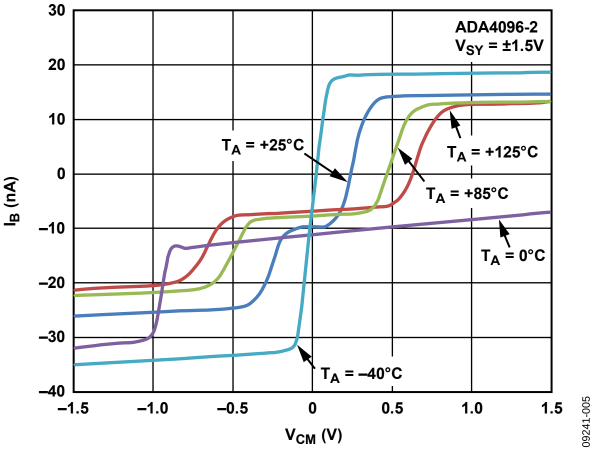


Figure 5. Input Bias Current vs. V_{CM} and Temperature

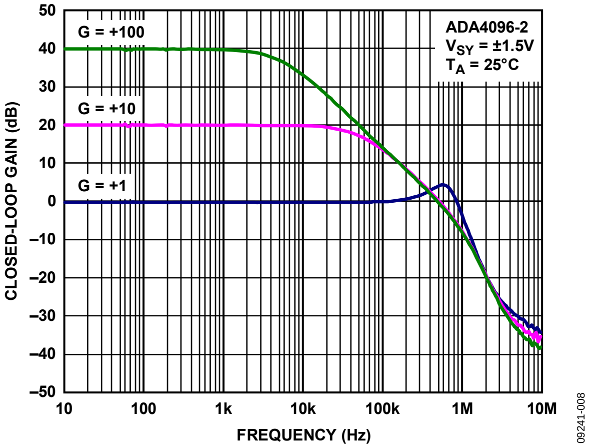


Figure 8. Closed-Loop Gain vs. Frequency

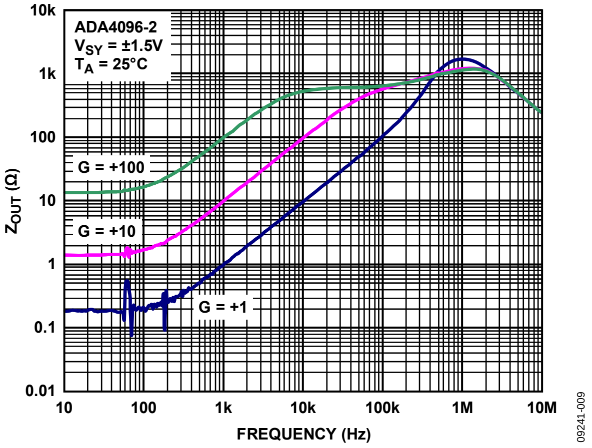


Figure 9. Output Impedance vs. Frequency

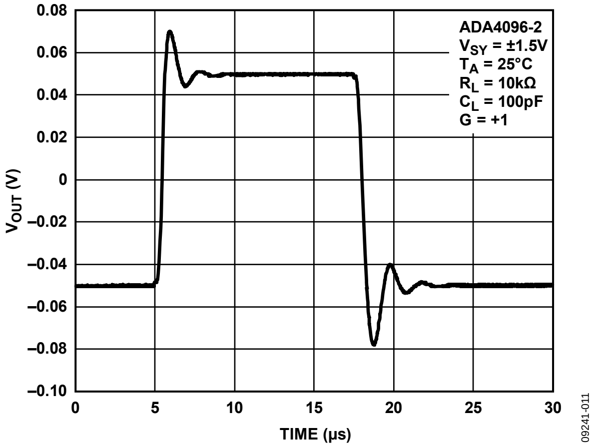


Figure 12. Small Signal Transient Response

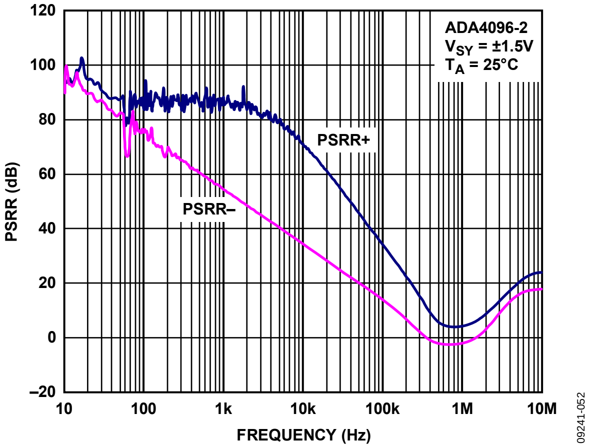


Figure 10. PSRR vs. Frequency

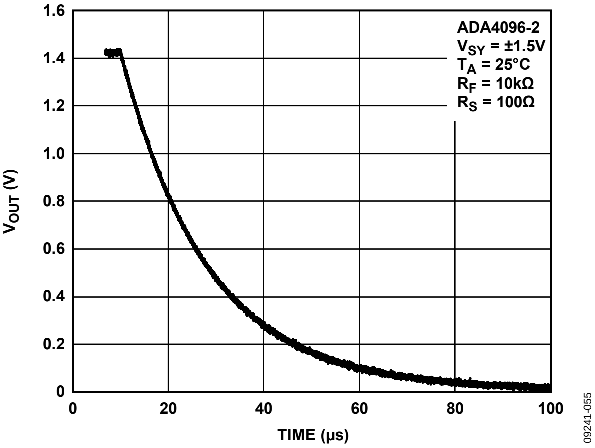


Figure 13. Positive Overload Recovery

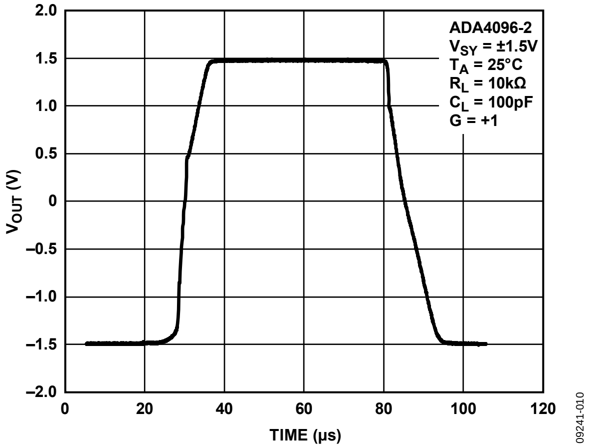


Figure 11. Large Signal Transient Response

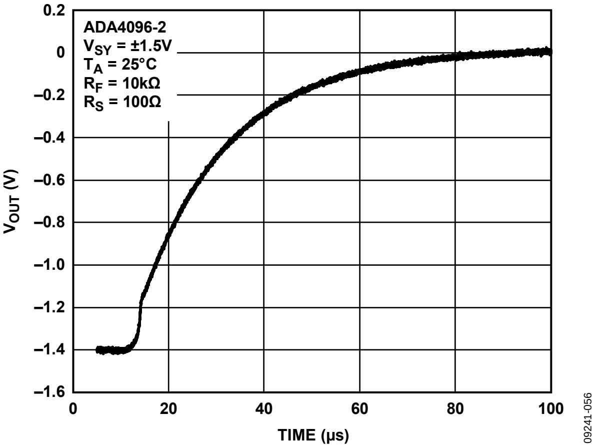


Figure 14. Negative Overload Recovery

±5 V CHARACTERISTICS

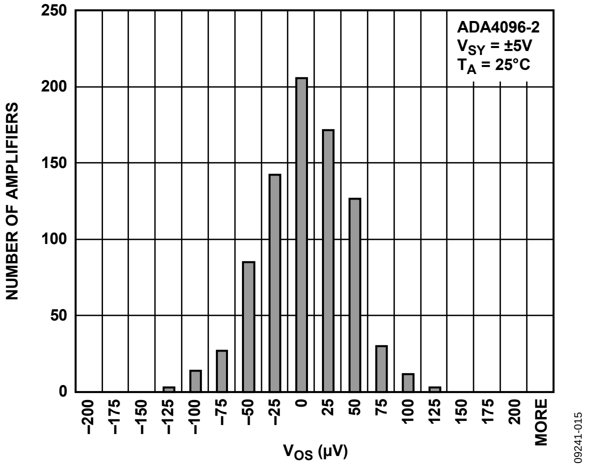


Figure 15. Input Offset Voltage Distribution

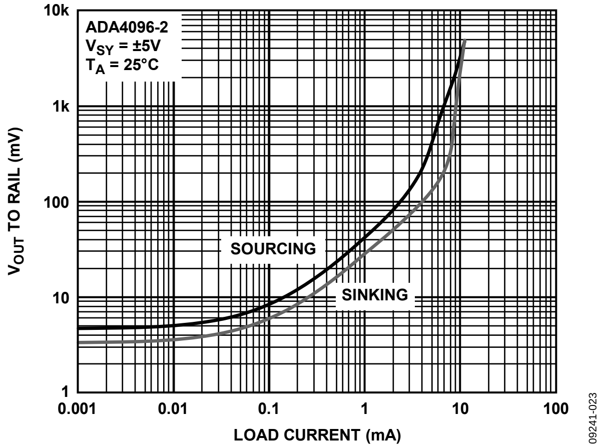


Figure 18. Dropout Voltage vs. Load Current

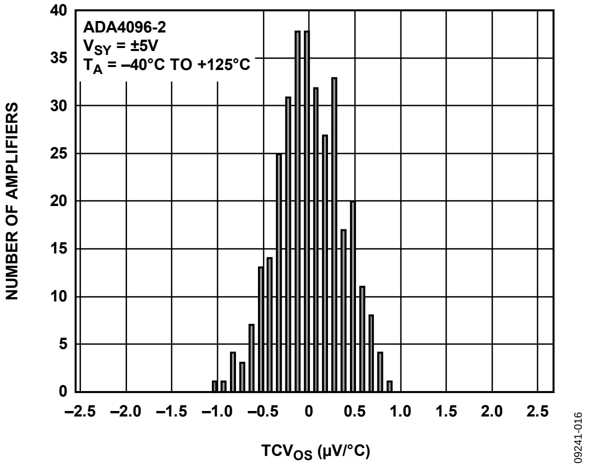


Figure 16. Offset Voltage Drift Distribution

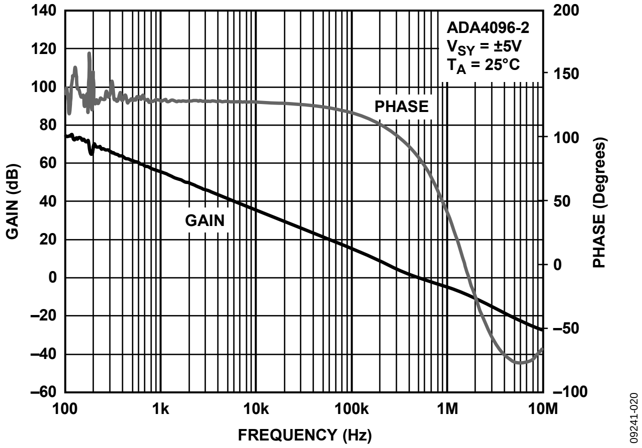


Figure 19. Open-Loop Gain and Phase vs. Frequency

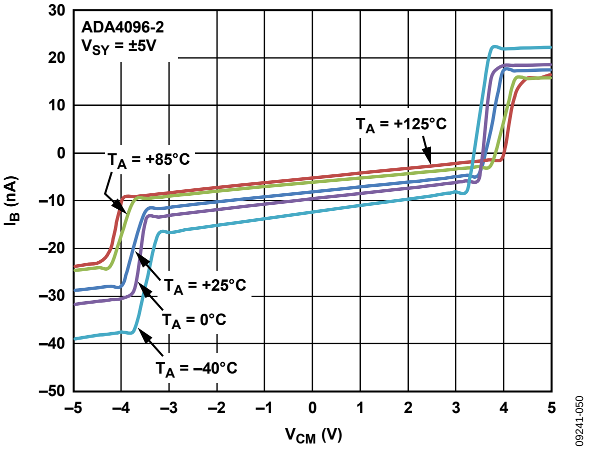


Figure 17. Input Bias Current vs. V_{CM} and Temperature

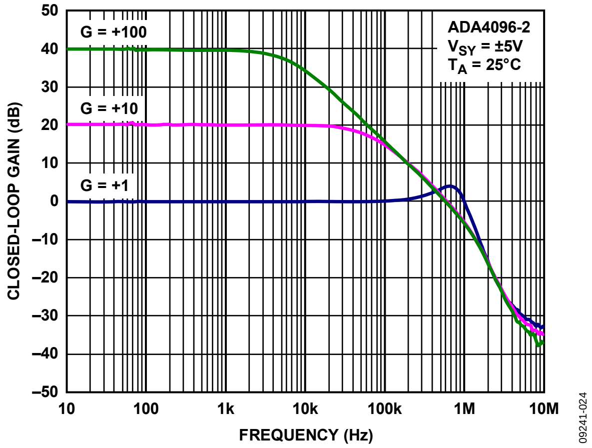


Figure 20. Closed-Loop Gain vs. Frequency

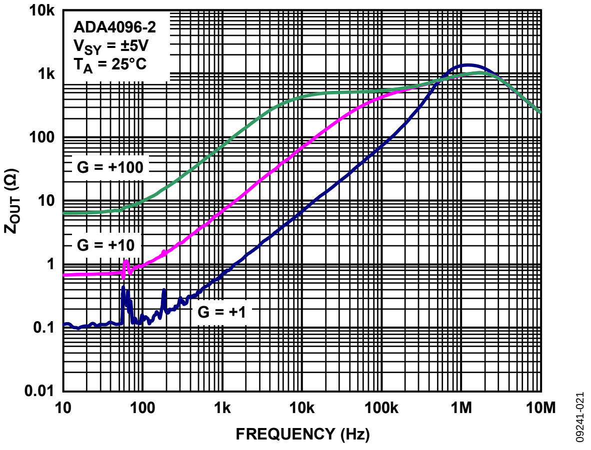


Figure 21. Output Impedance vs. Frequency

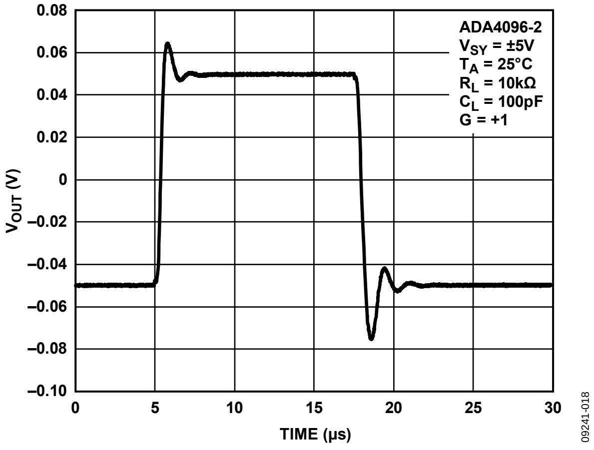


Figure 24. Small Signal Transient Response

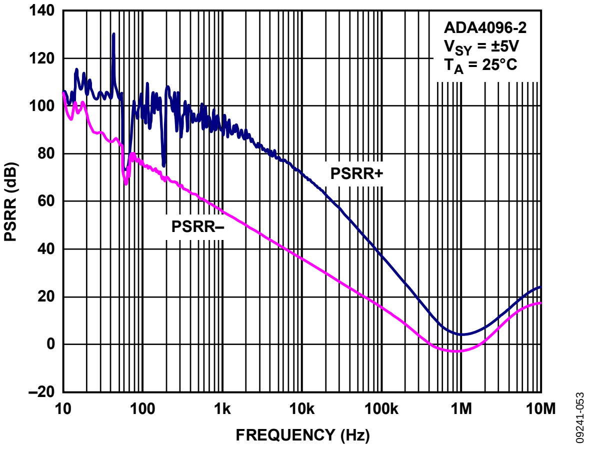


Figure 22. PSRR vs. Frequency

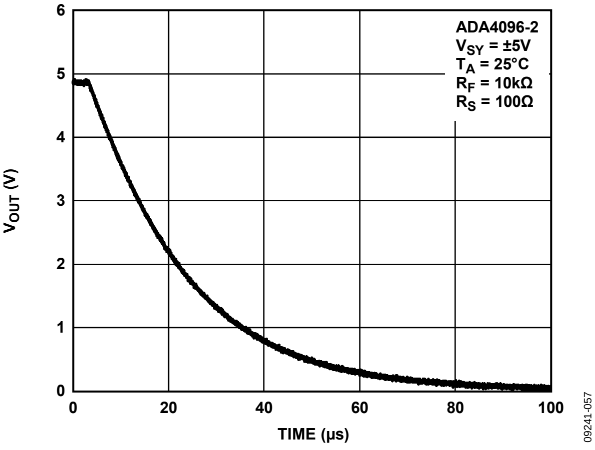


Figure 25. Positive Overload Recovery

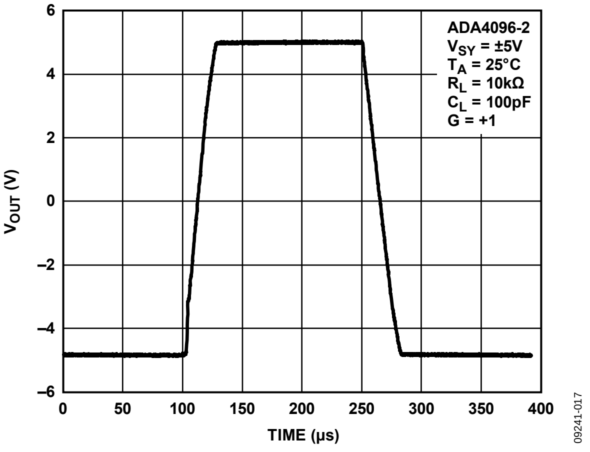


Figure 23. Large Signal Transient Response

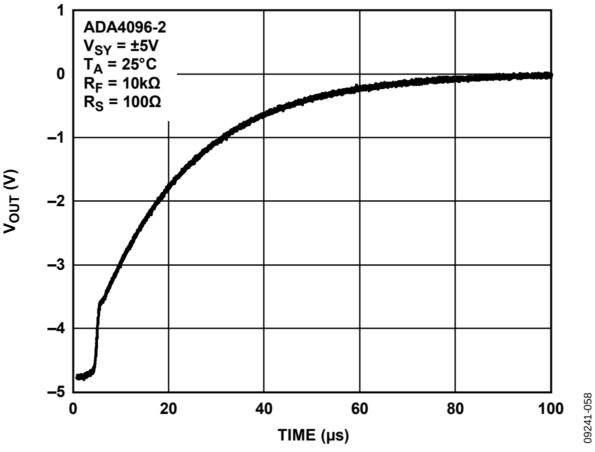


Figure 26. Negative Overload Recovery

±15 V CHARACTERISTICS

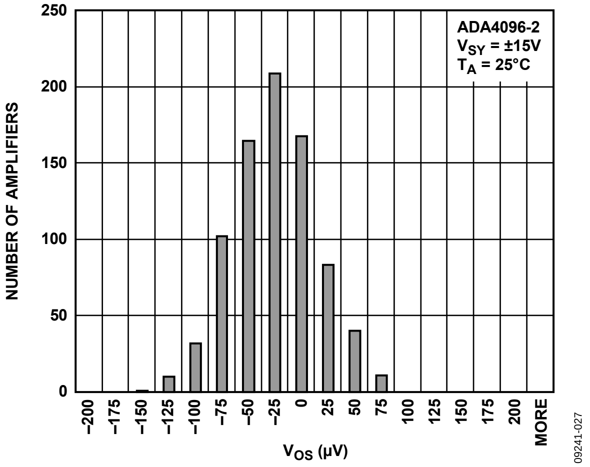


Figure 27. Input Offset Voltage Distribution

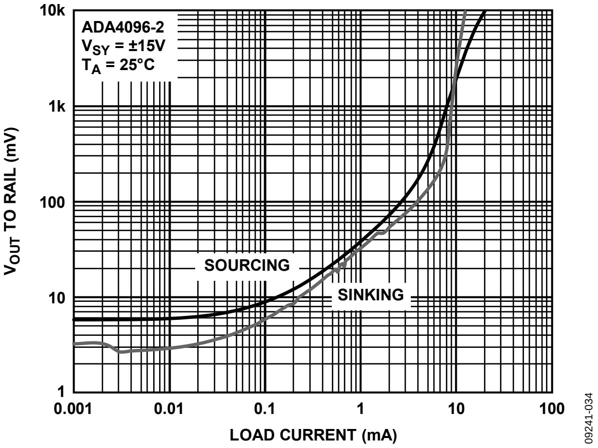


Figure 30. Dropout Voltage vs. Load Current

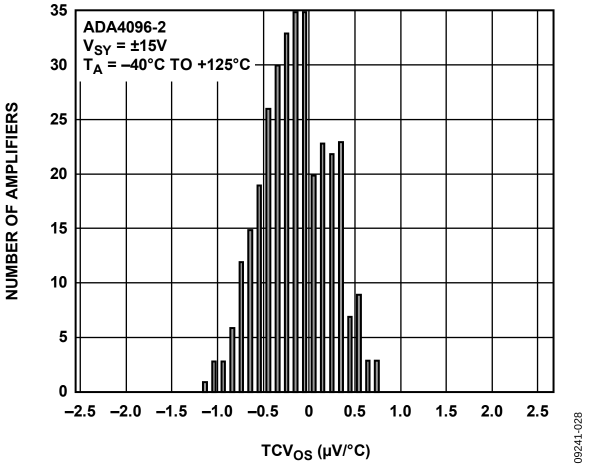


Figure 28. Offset Voltage Drift Distribution

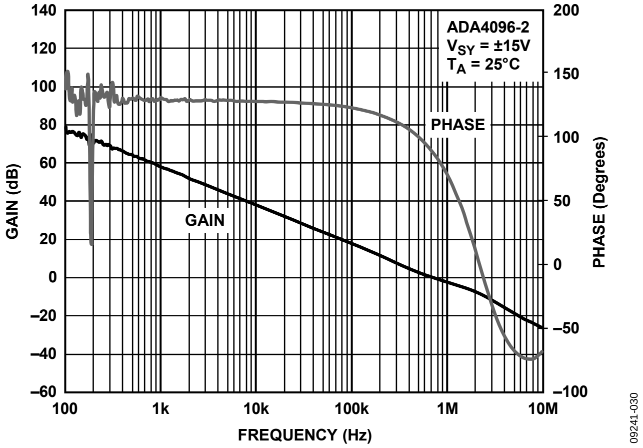


Figure 31. Open-Loop Gain and Phase vs. Frequency

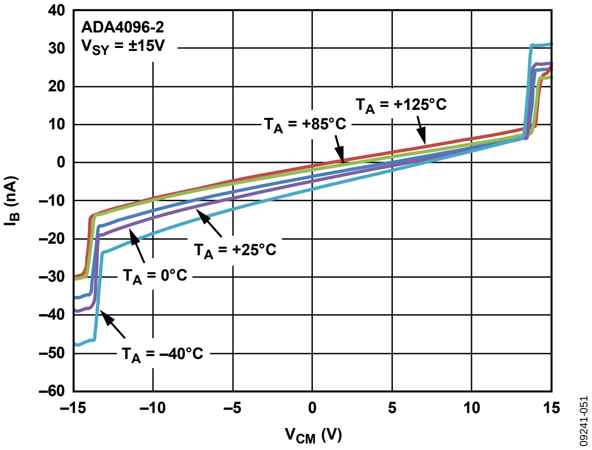


Figure 29. Input Bias Current vs. V_{CM} and Temperature

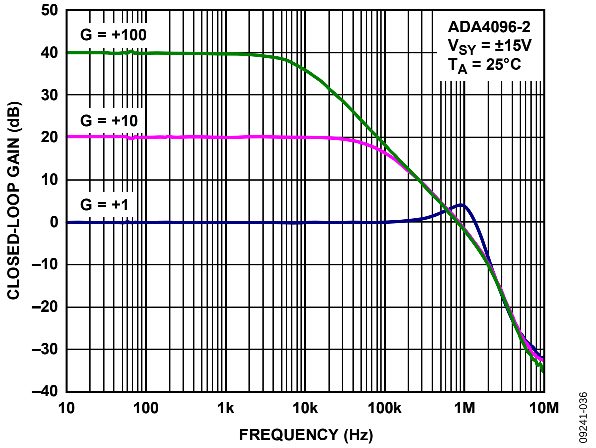


Figure 32. Closed-Loop Gain vs. Frequency

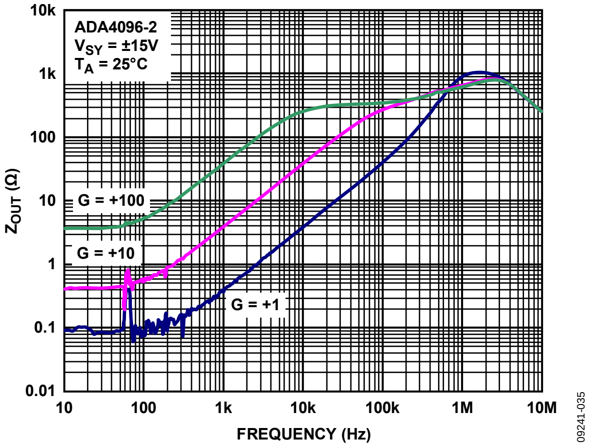


Figure 33. Output Impedance vs. Frequency

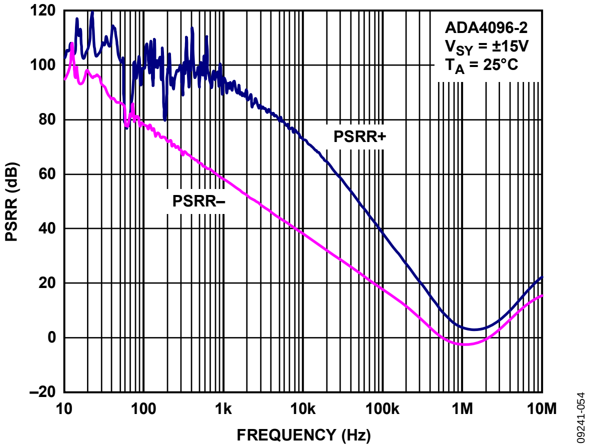


Figure 34. PSRR vs. Frequency

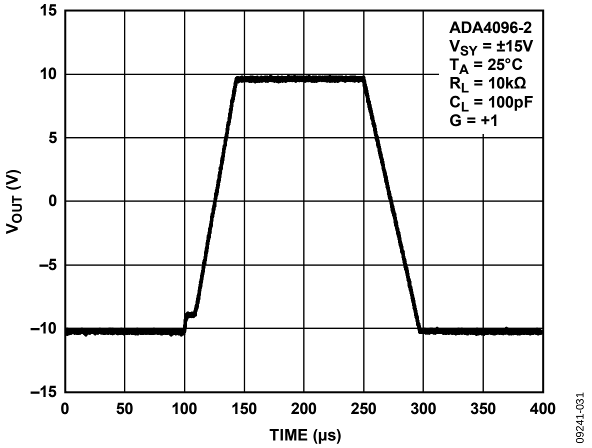


Figure 35. Large Signal Transient Response

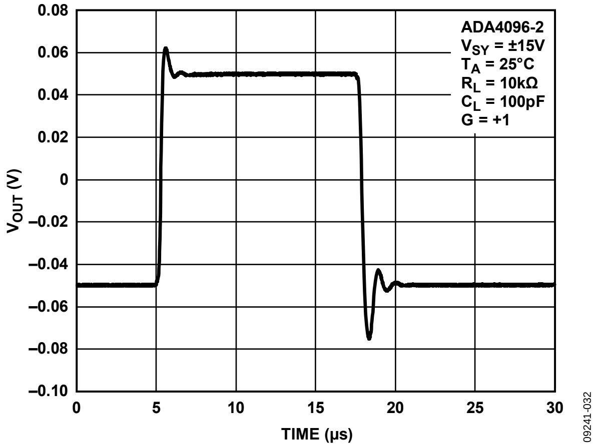


Figure 36. Small Signal Transient Response

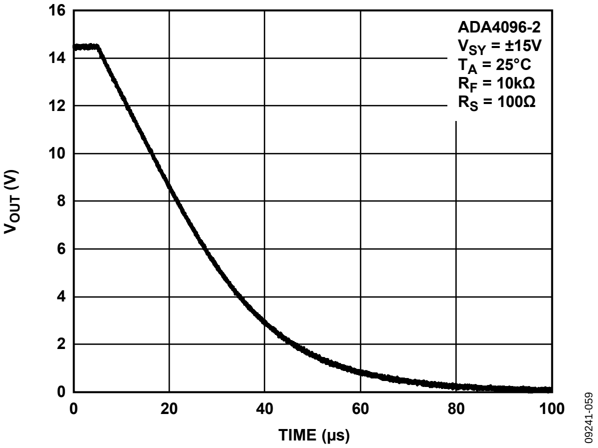


Figure 37. Positive Overload Recovery

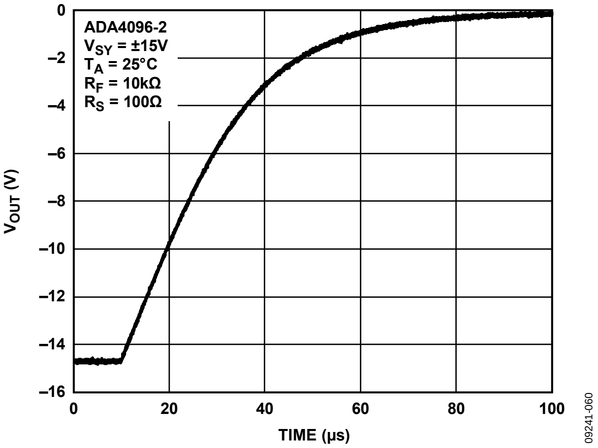


Figure 38. Negative Overload Recovery

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPHS

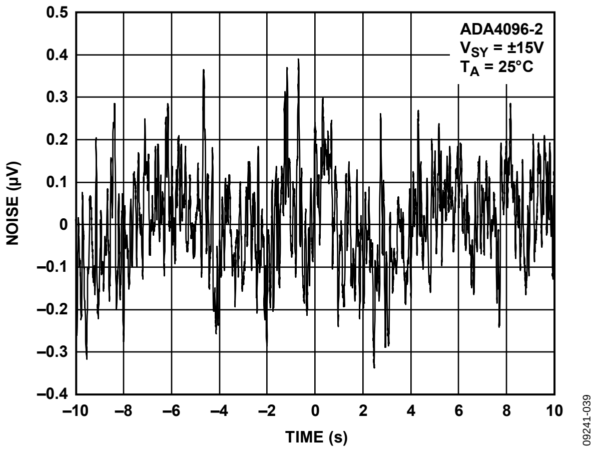


Figure 39. Input Voltage Noise, 0.1 Hz to 10 Hz Bandwidth

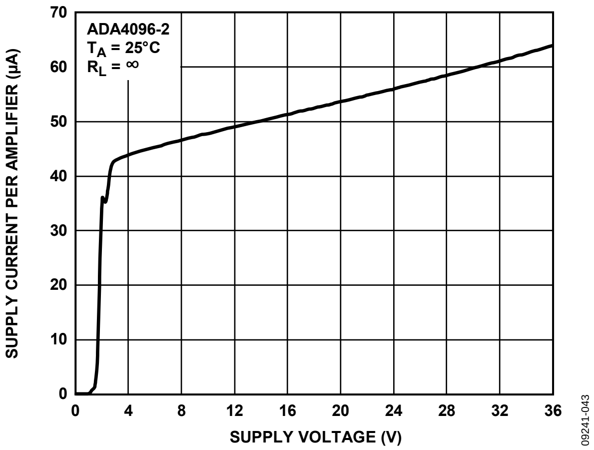


Figure 42. Supply Current vs. Supply Voltage

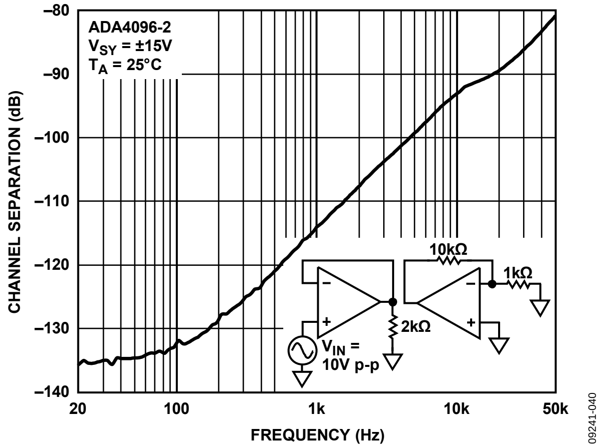


Figure 40. Channel Separation vs. Frequency

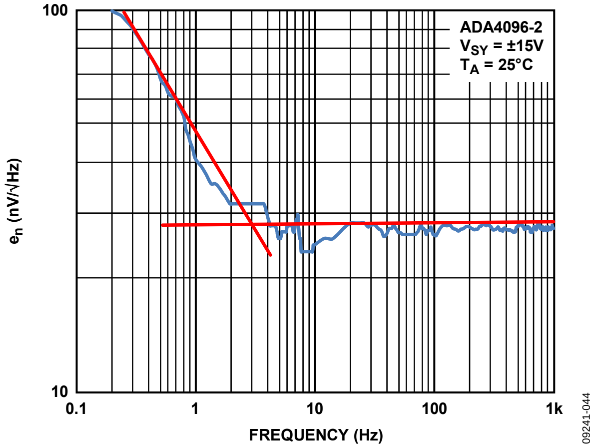


Figure 43. Voltage Noise Density

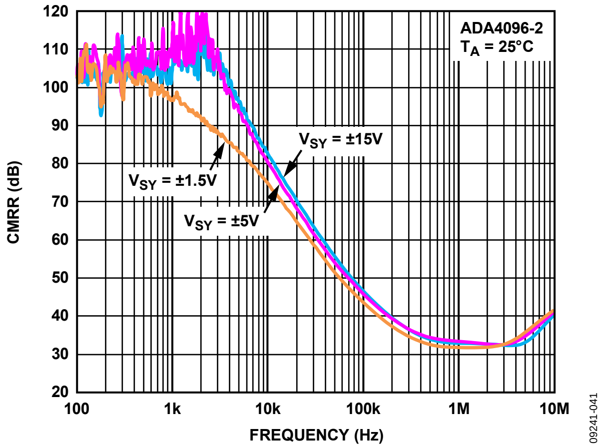


Figure 41. CMRR vs. Frequency

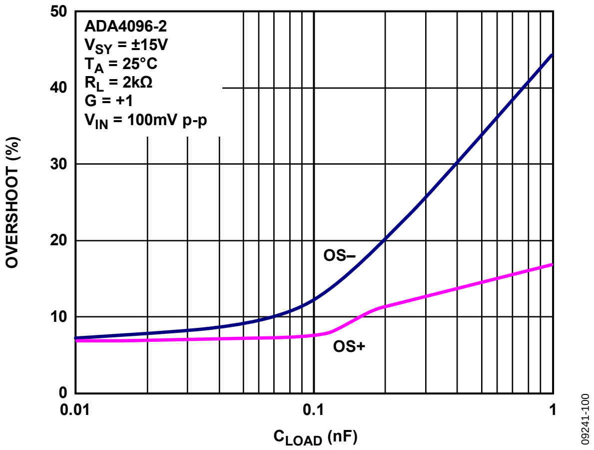


Figure 44. Overshoot vs. Load Capacitance

THEORY OF OPERATION

INPUT STAGE

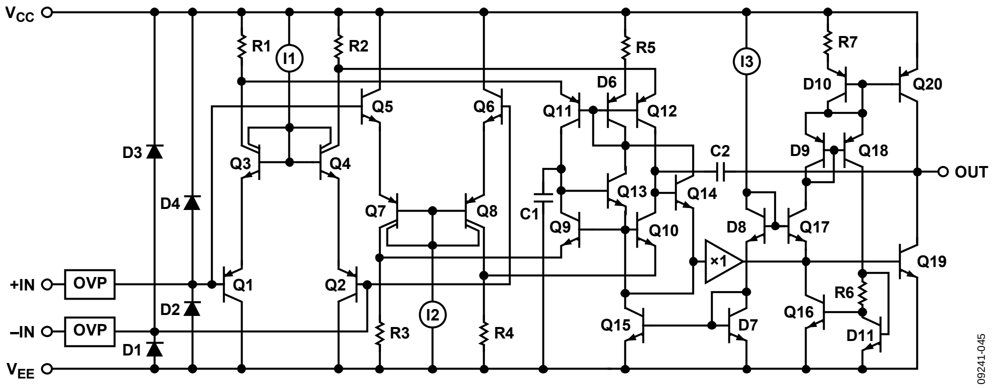


Figure 45. Simplified Schematic

Figure 45 shows a simplified schematic of the ADA4096-2. The input stage comprises two differential pairs (Q1 to Q4 and Q5 to Q8) operating in parallel. When the input common-mode voltage approaches V_{CC} – 1.5 V, Q1 to Q4 shut down as I1 reaches its minimum voltage compliance. Conversely, when the input common-mode voltage approaches V_{EE} + 1.5 V, Q5 to Q8 shut down as I2 reaches its minimum voltage compliance. This topology allows for maximum input dynamic range because the amplifier can function with its inputs at 200 mV outside the rail (at room temperature).

As with any rail-to-rail input amplifier, V_{OS} mismatch between the two input pairs determines the CMRR of the amplifier. If the input common-mode voltage range is kept within 1.5 V of each rail, transitions between the input pairs are avoided, thus improving the CMRR by approximately 10 dB (see Table 3 and Table 4).

PHASE INVERSION

Some single-supply amplifiers exhibit phase inversion when the input signal extends beyond the common-mode voltage range of the amplifier. When the input devices become saturated, the inverting and noninverting inputs exchange functions, causing the output to move in the opposing direction.

Although phase inversion persists for only as long as the inputs are saturated, it can be detrimental to applications where the amplifier is part of a closed-loop system. The ADA4096-2 is free from phase inversion over the entire common-mode voltage range, as well as the overvoltage protected range stated in the Absolute Maximum Ratings section, Table 5. Figure 46 shows the ADA4096-2 in a unity-gain configuration with the input signal at ±40 V and the amplifier supplies at ±10 V.

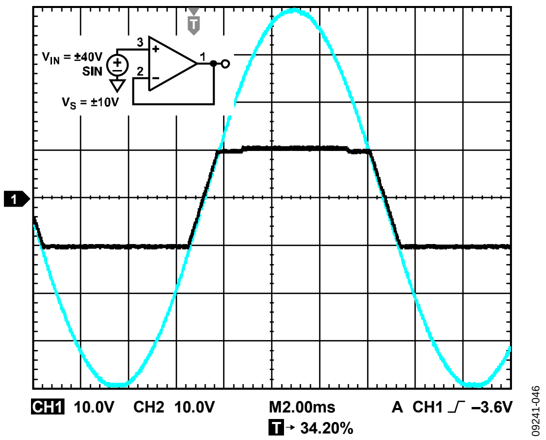


Figure 46. No Phase Reversal

INPUT OVERVOLTAGE PROTECTION

The ADA4096-2 inputs are protected from input voltage excursions up to 32 V outside each rail. This feature is of particular importance in applications with power supply sequencing issues that could cause the signal source to be active before the supplies to the amplifier.

Figure 47 shows the input current limiting capability of the ADA4096-2 (green curves) compared to using a 5 kΩ series resistor (red curves).

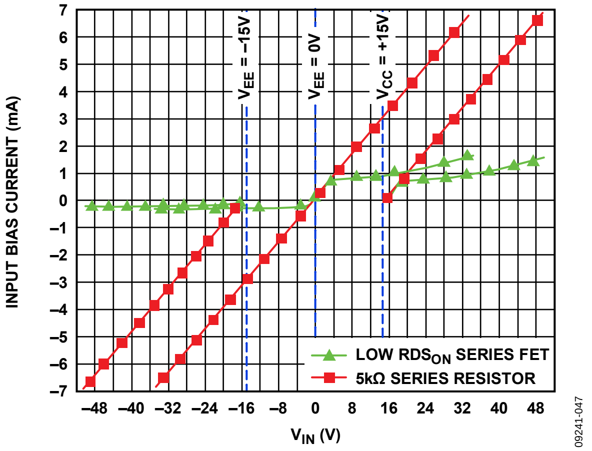


Figure 47. Input Current Limiting Capability

Figure 47 was generated with the ADA4096-2 in a buffer configuration with the supplies connected to GND (or ±15 V) and the positive input swept until it exceeds the supplies by 32 V. In general, input current is limited to 1 mA during positive overvoltage conditions and 200 μA during negative undervoltage conditions. For example, at an overvoltage of 20 V, the ADA4096-2 input current is limited to 1 mA, providing a current limit equivalent to a series 20 kΩ resistor. Figure 47 also shows that the current limiting circuitry is active whether the amplifier is powered or not.

Note that Figure 47 represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2 to Table 4.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be pressed into service as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop, but it cannot, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 48).

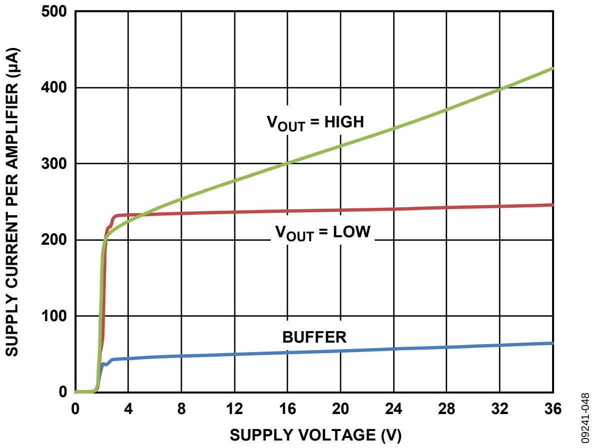
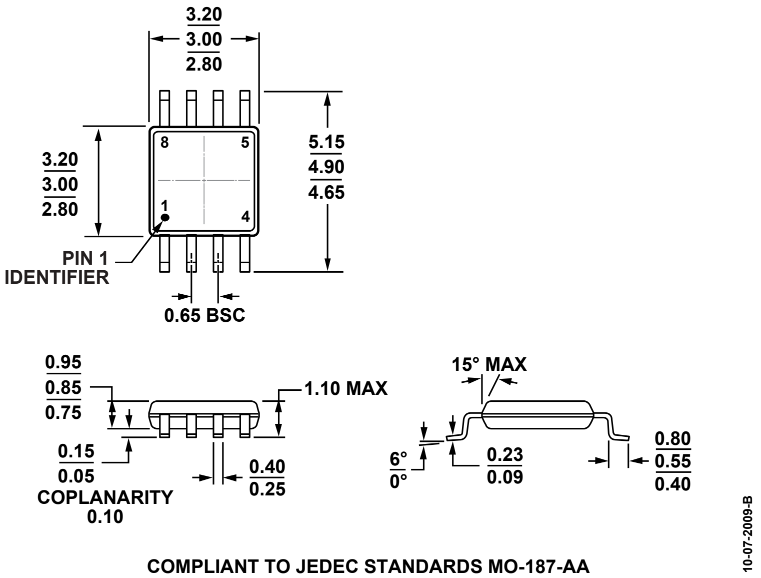


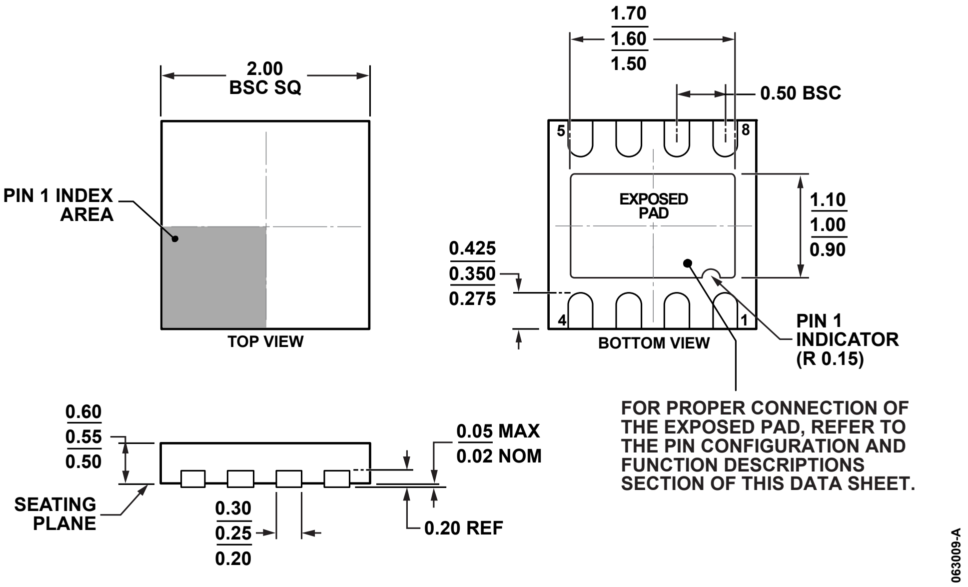
Figure 48. Comparator Supply Current

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 49. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Figure 50. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2 mm × 2 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Branding
ADA4096-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2ACPZ-R7	−40°C to +125°C	8-Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	A4
ADA4096-2ACPZ-RL	−40°C to +125°C	8-Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	A4
ADA4096-2WARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T
ADA4096-2WARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2T

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADA4096-2W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

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