Data Sheet

LM358, LM324

Low Power, 3V to 36V, Single/Dual/Quad Amplifiers

FEATURES

- Unity gain stable
- 100dB voltage gain
- 550kHz unity gain bandwidth
- 0.5mA supply current
- 20nA input bias current
- 2mV input offset voltage
- 3V to 36V single supply voltage range
- ±1.5V to ±18V dual supply voltage range
- Input common mode voltage range includes ground
- 0V to V_S-1.5V output voltage swing
- Improved replacements for industry standard LM358 and LM324
- LM358: Pb-free SOIC-8
- LM324: Pb-free SOIC-14

APPLICATIONS

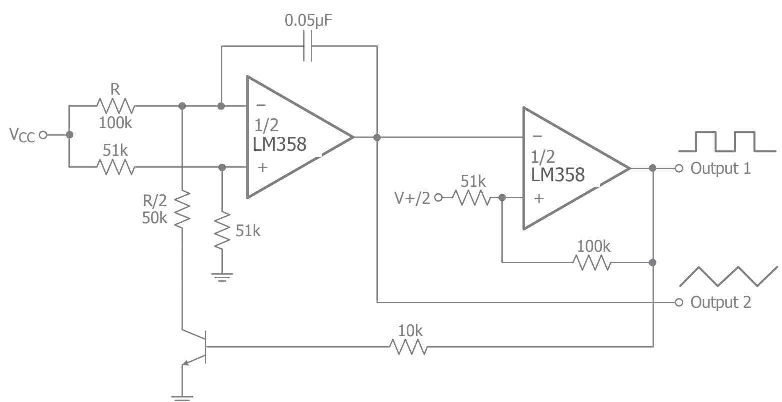
- Battery Charger
- Active Filters
- Transducer amplifiers
- General purpose controllers
- General purpose instruments

General Description

The LM358 (dual), and LM324 (quad) are voltage feedback amplifiers that are internally frequency compensated to provide unity gain stability. At unity gain (G=1), these amplifiers offer 550kHz of bandwidth. They consume only 0.5mA of supply current over the entire power supply operating range. The LM358, and LM324 are specifically designed to operate from single or dual supply voltages.

The LM358, and LM324 offer a common mode voltage range that includes ground and a wide output voltage swing. The combination of low-power, high supply voltage range, and low supply current make these amplifiers well suited for many general purpose applications and as alternatives to several industry standard amplifiers on the market today.

Typical Application - Voltage Controlled Oscillator (VCO)

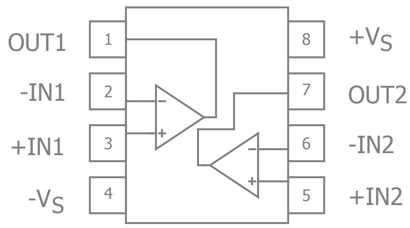


Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
LM358ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
LM324ISO14X	SOIC-14	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

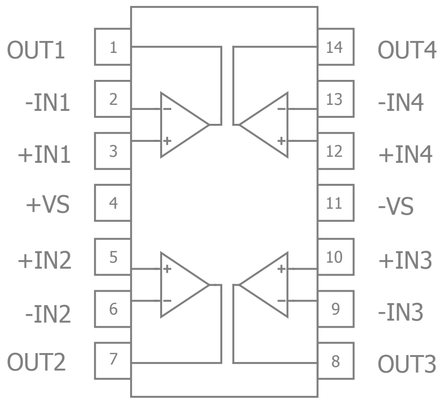
LM358 Pin Configuration



LM358 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

LM324 Pin Configuration



LM324 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	40	V
Differential Input Voltage		40	V
Input Voltage	-0.3	40	V
Power Dissipation (T_A = 25°C) - SOIC-8		550	mW
Power Dissipation (T_A = 25°C) - SOIC-14		800	mW

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
SOIC-8		100		°C/W
SOIC-14		88		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	3 (±1.5)		36 (±18)	V

Electrical Characteristics

T_A = 25°C (if **bold**, T_A = -40 to +85°C), V_s = +5V, -V_s = GND, R_f = R_g =2kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, V_S = 5V		330		kHz
		G = +1, V_{OUT} = 0.2V_{pp}, V_S = 30V		550		kHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}, V_S = 5V		300		kHz
		G = +1, V_{OUT} = 0.2V_{pp}, V_S = 30V		422		kHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 1V_{pp}, V_S = 5V		107		kHz
		G = +2, V_{OUT} = 2V_{pp}, V_S = 30V		76		kHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%), V_S = 5V		4		μs
		V_{OUT} = 2V step; (10% to 90%), V_S = 30V		5.6		μs
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	1V step, V_S = 5V		200		V/ms
		4V step, V_S = 30V		285		V/ms
Distortion/Noise Response						
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, f = 1kHz, G = 20dB, C_L = 100pF, V_S = 30V		0.015		%
e_n	Input Voltage Noise	> 10kHz, V_S = 5V		45		nV/√Hz
		> 10kHz, V_S = 30V		40		nV/√Hz
X_{TALK}	Crosstalk	Channel-to-channel, 1kHz to 20kHz		120		dB
DC Performance						
V_{IO}	Input Offset Voltage (1)	V_{OUT} = 1.4V, R_S = 0Ω, V_S = 5V to 30V		2	5	mV
					7	mV
dV_{IO}	Average Drift			7		μV/°C
I_b	Input Bias Current (1)	V_{CM} = 0V		20	100	nA
					200	nA
I_{OS}	Input Offset Current (1)	V_{CM} = 0V		5	30	nA
					100	nA
PSRR	Power Supply Rejection Ratio (1)	DC, V_S = 5V to 30V	70	100		dB
			60			dB
A_{OL}	Open-Loop Gain (1)	+V_S = 15V, R_L = ≥2kΩ, V_{OUT} = 1V to 11V	85	100		dB
			80			dB
	Supply Current, LM358 (1)	R_L = ∞, V_S = 30V		**0.7**	**2.0**	mA
		R_L = ∞, V_S = 5V		**0.5**	**1.2**	mA
	Supply Current, LM324 (1)	R_L = ∞, V_S = 30V		**1.0**	**3.0**	mA
		R_L = ∞, V_S = 5V		**0.7**	**1.2**	mA
Input Characteristics						
CMIR	Common Mode Input Range (1,3)	+V_S = 30V	0		+V_S - 1.5	V
CMRR	Common Mode Rejection Ratio (1)	DC, V_{CM} = 0V to (+V_S - 1.5V)	60	70		dB
			60			dB
Output Characteristics						
V_{OH}	Output Voltage Swing, High (1)	+V_S = 30V, R_L = 2kΩ	26			V
			26			V
		+V_S = 30V, R_L = 10kΩ	27	28		V
			27			V
V_{OL}	Output Voltage Swing, Low (1)	+V_S = 5V, R_L = 10kΩ		5	20	mV
					30	mV

Electrical Characteristics continued

T_A = 25°C (if **bold**, T_A = -40 to +85°C), V_s = +5V, $-V_s$ = GND, R_f = R_g =2kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{SOURCE}	Output Current, Sourcing (1)	V_{IN+} = 1V, V_{IN-} = 0V, $+V_S$ = 15V, V_{OUT} = 2V	20	40		mA
			20			
I_{SINK}	Output Current, Sinking (1)	V_{IN+} = 0V, V_{IN-} = 1V, $+V_S$ = 15V, V_{OUT} = 2V	10	15		mA
			5			
		V_{IN+} = 0V, V_{IN-} = 1V, $+V_S$ = 15V, V_{OUT} = 0.2V	12	50		μA
I_{SC}	Short Circuit Output Current (1)	$+V_S$ = 15V		40	60	mA

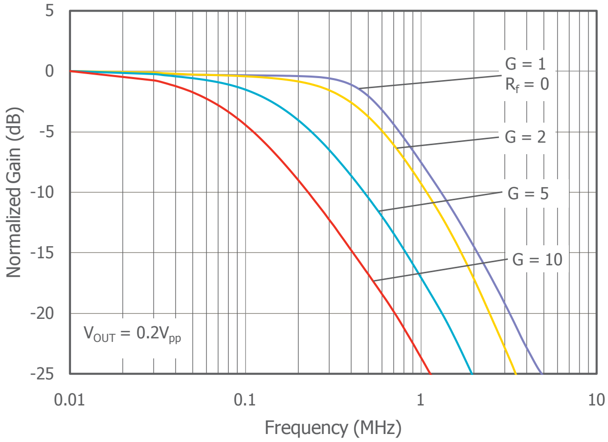
Notes:

1. 100% tested at 25°C. (Limits over the full temperature range are guaranteed by design.)
2. The input common mode voltage of either input signal voltage should be kept > 0.3V at 25°C. The upper end of the common-mode voltage range is $+V_S$ - 1.5V at 25°C, but either or both inputs can go to +36V without damages, independent of the magnitude of V_S.

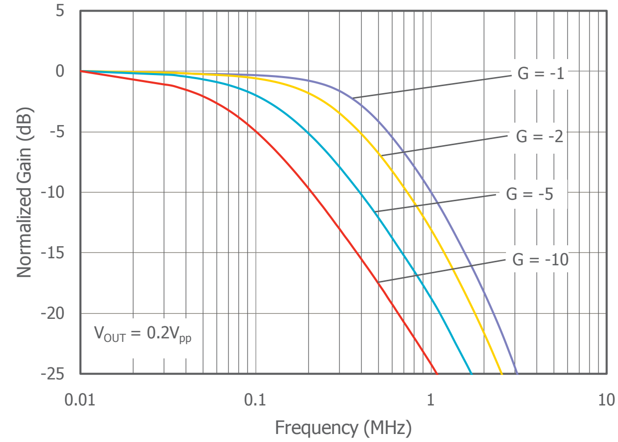
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = 30V, $-V_S$ = GND, R_f = R_g =2kΩ, R_L = 2kΩ, G = 2; unless otherwise noted.

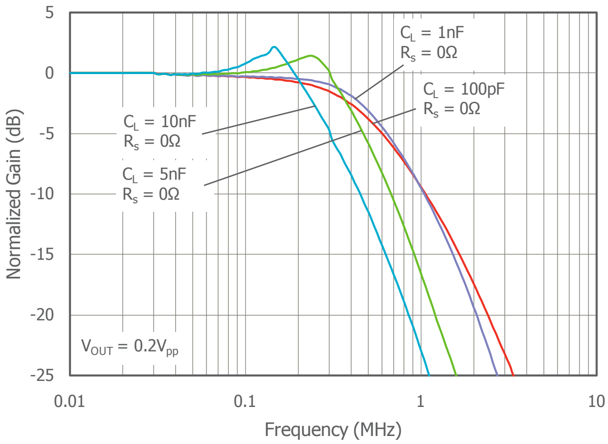
Non-Inverting Frequency Response



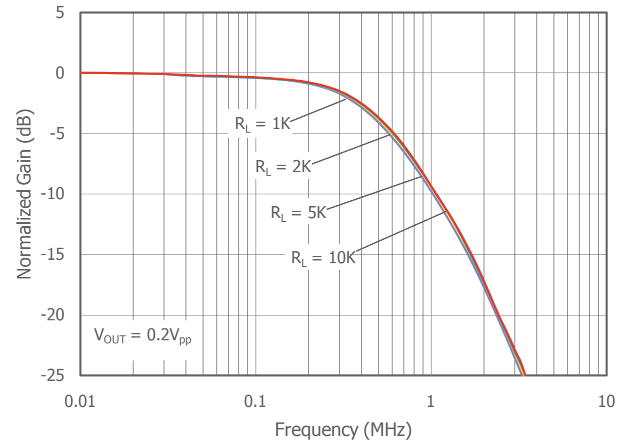
Inverting Frequency Response



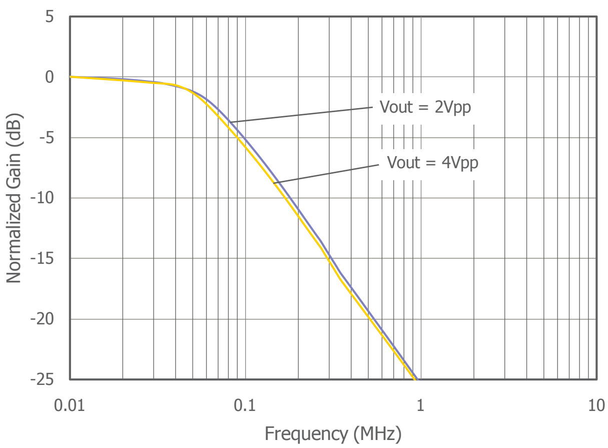
Frequency Response vs. C_L



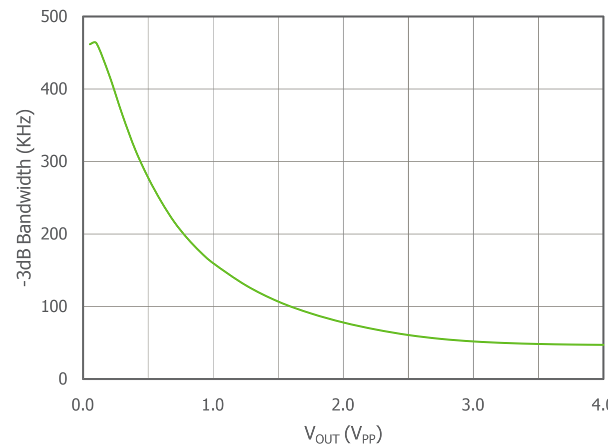
Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



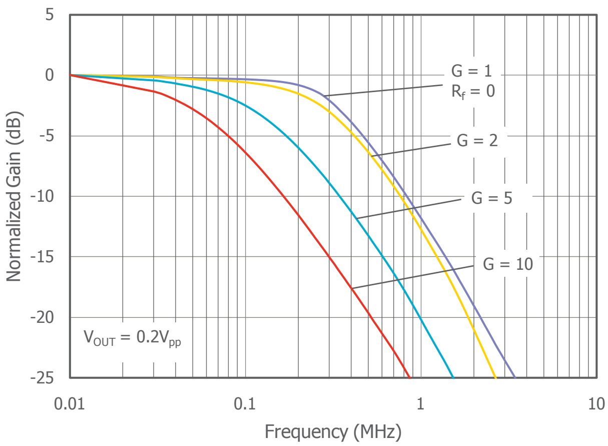
-3dB Bandwidth vs. V_{OUT}



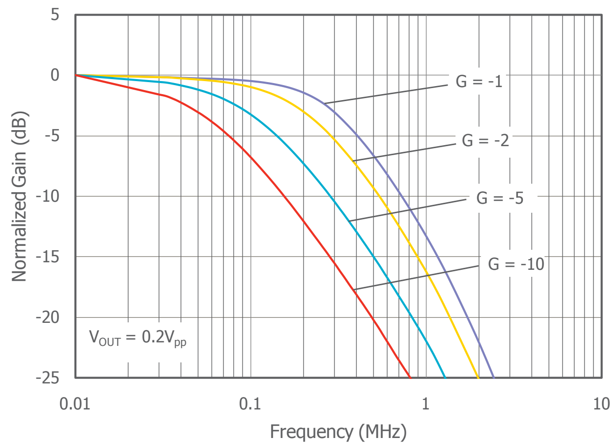
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = 30V, $-V_S$ = GND, $R_f = R_g$ =2kΩ, R_L = 2kΩ, G = 2; unless otherwise noted.

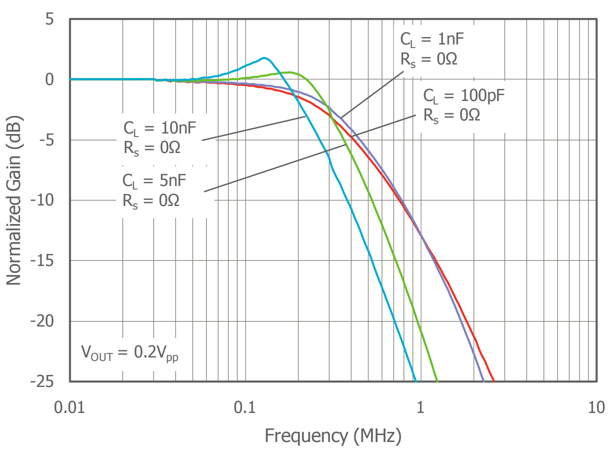
Non-Inverting Frequency Response at V_S = 5V



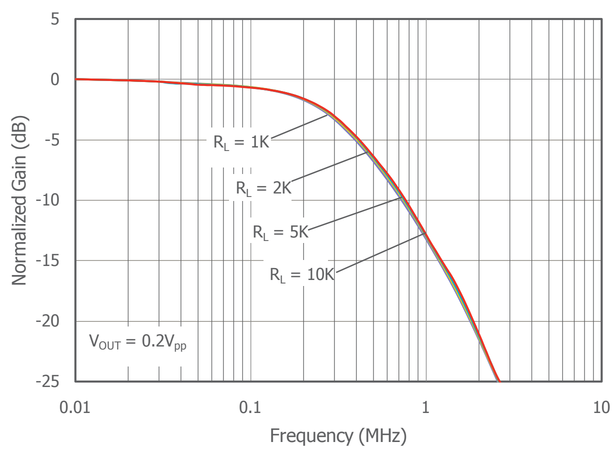
Inverting Frequency Response at V_S = 5V



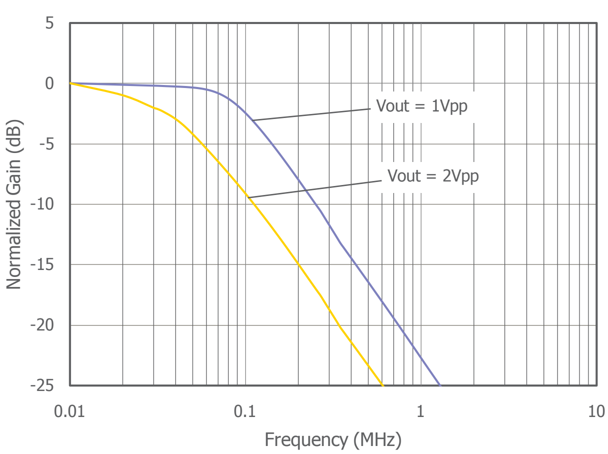
Frequency Response vs. C_L at V_S = 5V



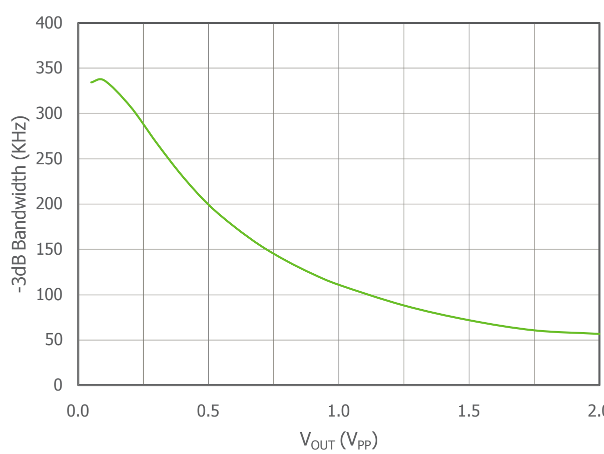
Frequency Response vs. R_L at V_S = 5V



Frequency Response vs. V_{OUT} at V_S = 5V



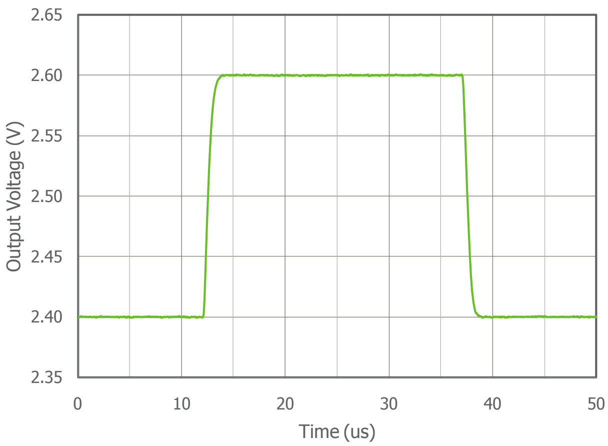
-3dB Bandwidth vs. V_{OUT} at V_S = 5V



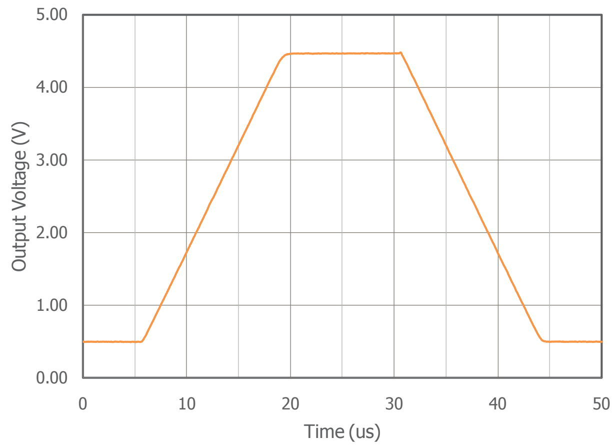
Typical Performance Characteristics - Continued

T_A = 25°C, $+V_S$ = 30V, $-V_S$ = GND, R_f = R_g =2kΩ, R_L = 2kΩ, G = 2; unless otherwise noted.

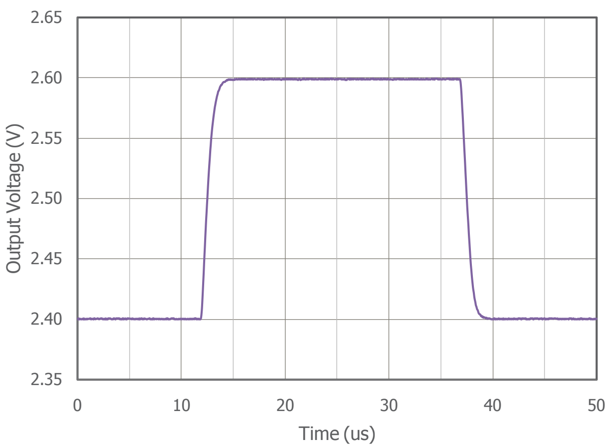
Small Signal Pulse Response



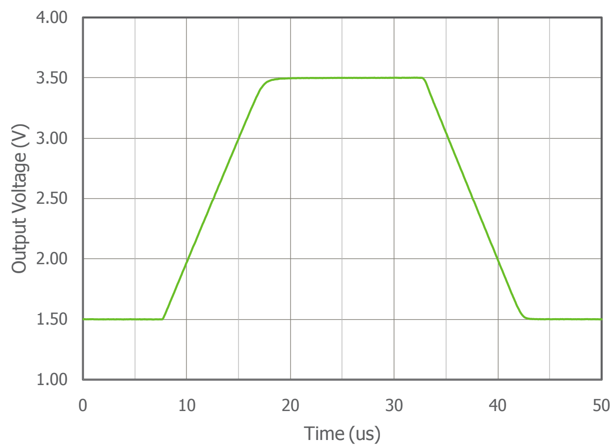
Large Signal Pulse Response



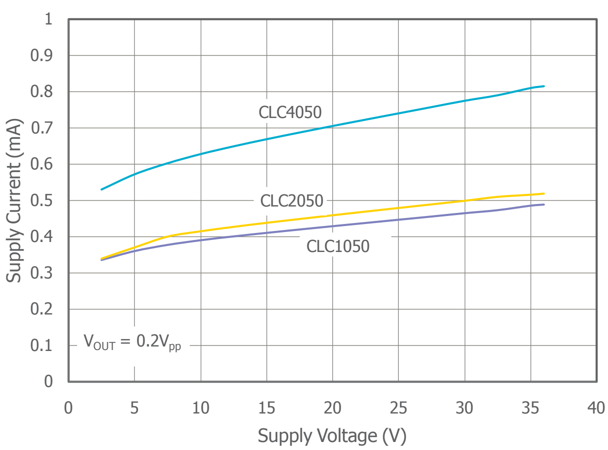
Small Signal Pulse Response at V_S = 5V



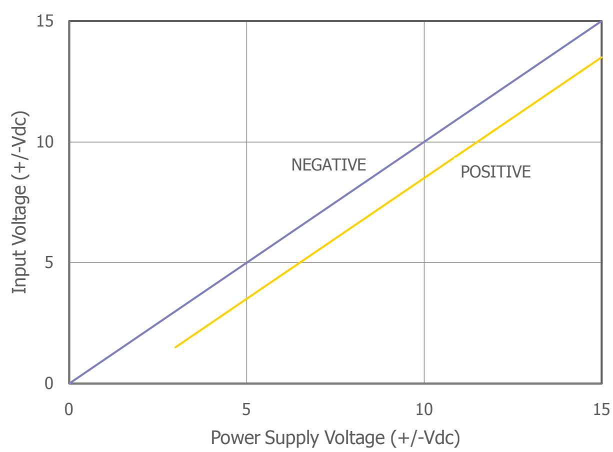
Large Signal Pulse Response at V_S = 5V



Supply Current vs. Supply Voltage



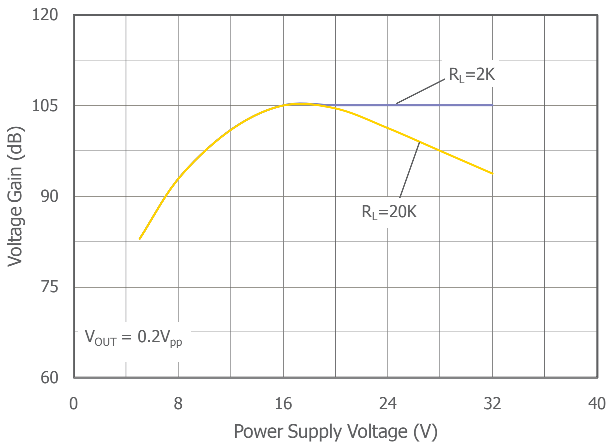
Input Voltage Range vs. Power Supply



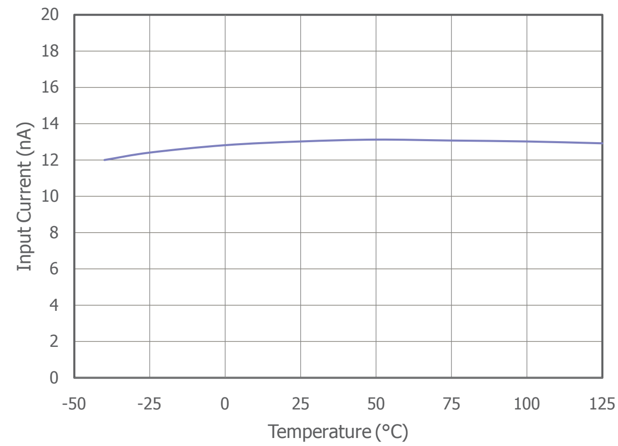
Typical Performance Characteristics - Continued

T_A = 25°C, $+V_S$ = 30V, $-V_S$ = GND, R_f = R_g =2kΩ, R_L = 2kΩ, G = 2; unless otherwise noted.

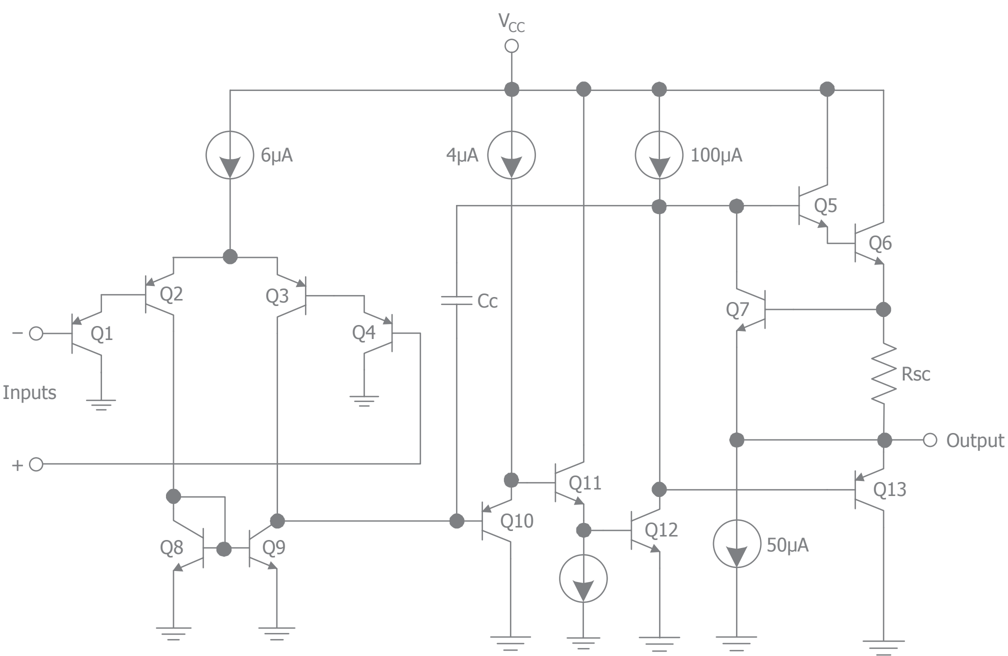
Voltage Gain vs. Supply Voltage



Input Current vs. Temperature



Functional Block Diagram



Application Information

Basic Operation

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

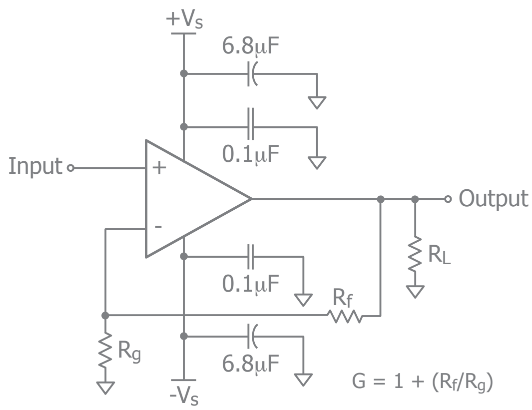


Figure 1. Typical Non-Inverting Gain Circuit

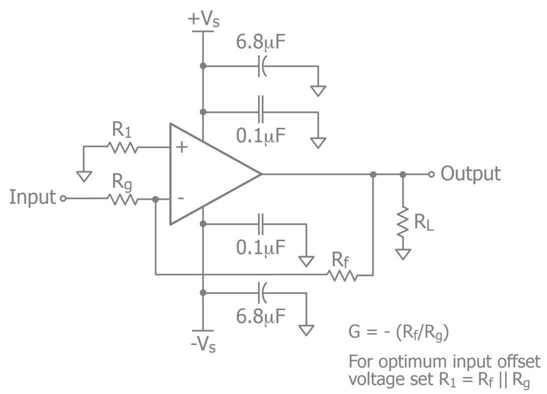


Figure 2. Typical Inverting Gain Circuit

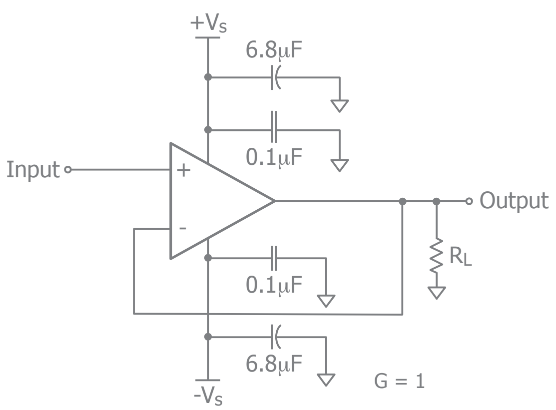


Figure 3. Unity Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2k ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value Theta$_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$P_D = P_{supply} - P_{load}$

Supply power is calculated by the standard power equation.

$P_{supply} = V_{supply} \times I_{RMS\ supply}$

$V_{supply} = V_{S+} - V_{S-}$

Power delivered to a purely resistive load is:

$P_{load} = ((V_{LOAD})_{RMS}{}^2)/Rload_{eff}$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 3 would be calculated as:

$R_L \mid\mid (R_f + R_g)$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$

$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

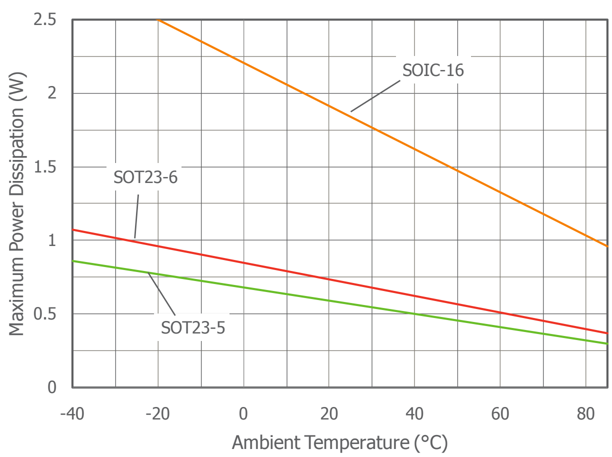


Figure 4. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

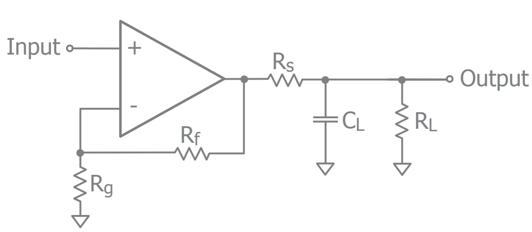


Figure 5. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in <=1dB peaking in the frequency response. The Frequency Response vs. C_L plot, on page 6, illustrates the response of the LM358/LM324.

C_L (pF)	R_S (Ω)	-3dB BW (kHz)
1nF	0	485
5nF	0	390
10nF	0	260
100	0	440

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The LM358/LM324 will typically recover in less than 30ns from an overdrive condition. Figure 6 shows the LM358 in an overdriven condition.

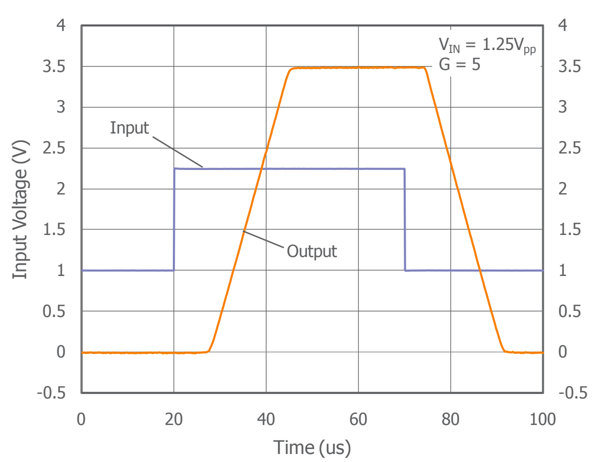


Figure 6. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	LM358
CEB018	LM324

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-12. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

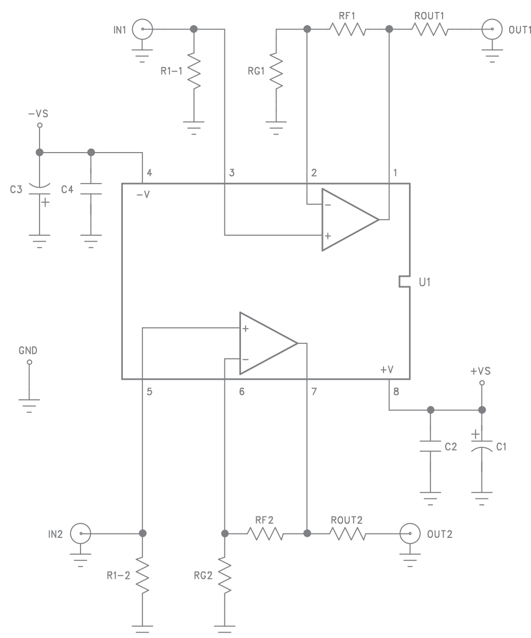


Figure 7. CEB006 Schematic

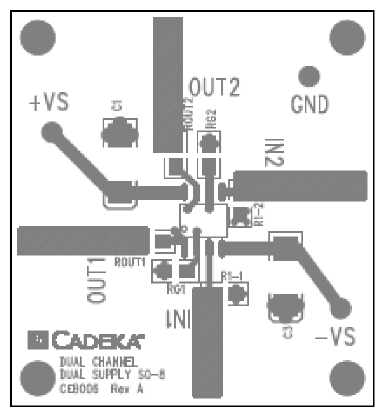


Figure 8. CEB006 Top View

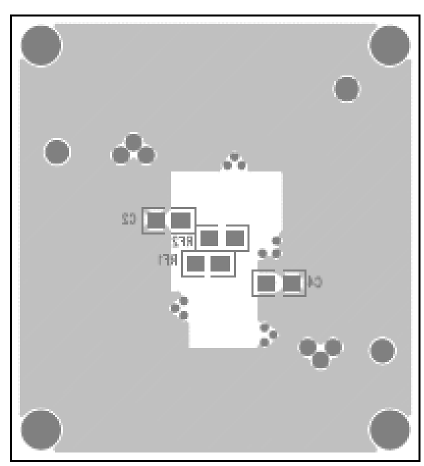


Figure 9. CEB006 Bottom View

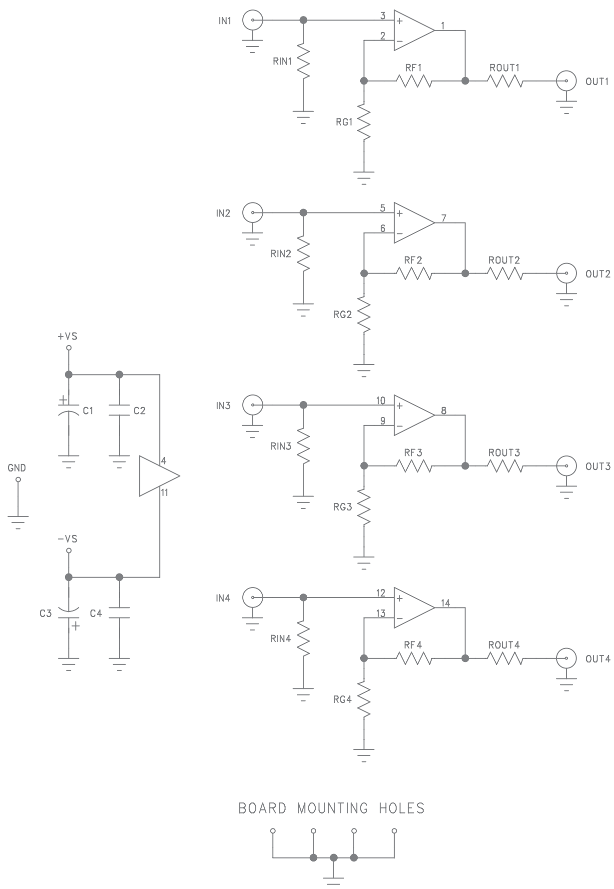


Figure 10. CEB018 Schematic

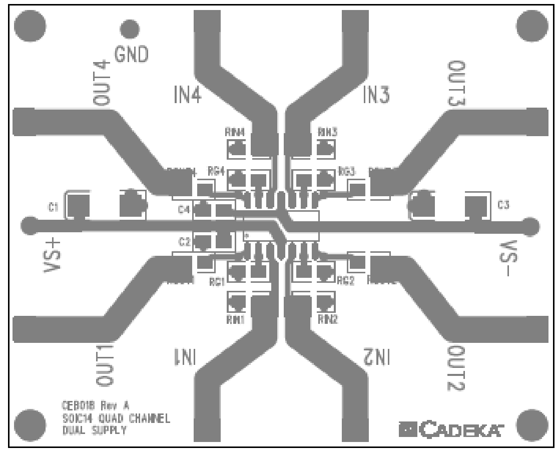


Figure 11 CEB018 Top View

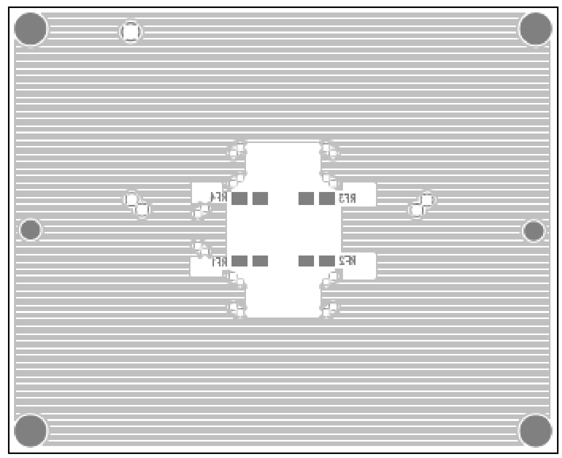


Figure 12. CEB018 Bottom View

Typical Applications

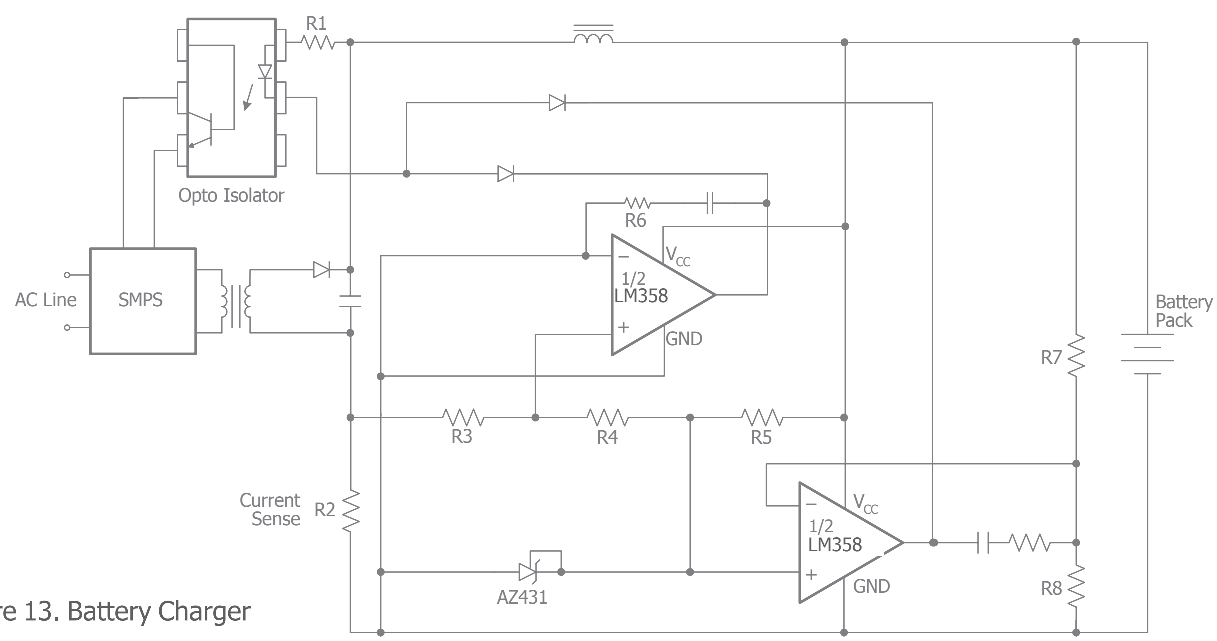


Figure 13. Battery Charger

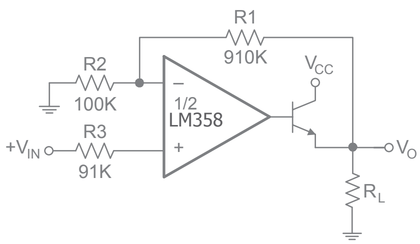


Figure 14. Power Amplifier

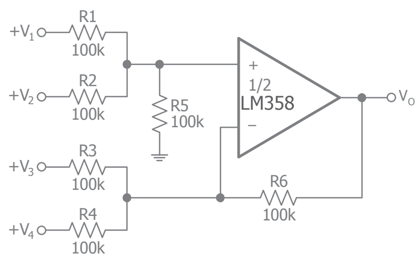


Figure 15. DC Summing Amplifier

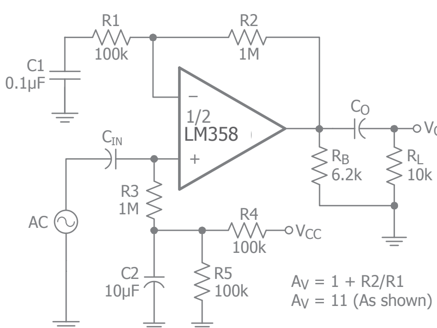


Figure 16. AC-Coupled Non-Inverting Amplifier

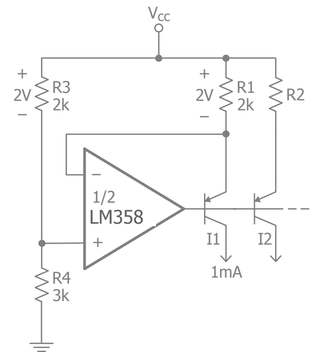


Figure 17. Fixed Current Sources

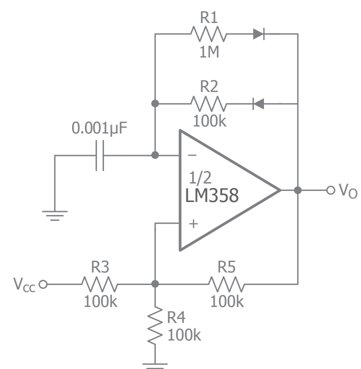


Figure 18. Pulse Generator

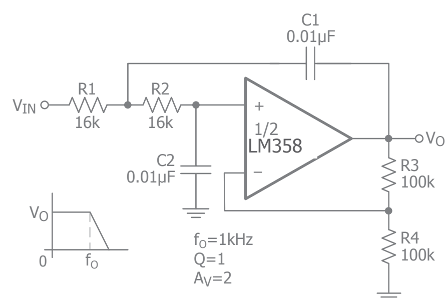
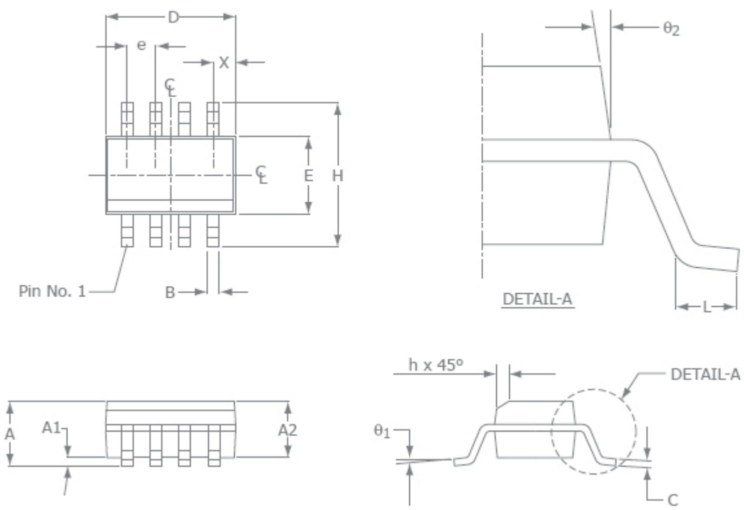


Figure 19. DC-Coupled Low-Pass Active Filter

Mechanical Dimensions

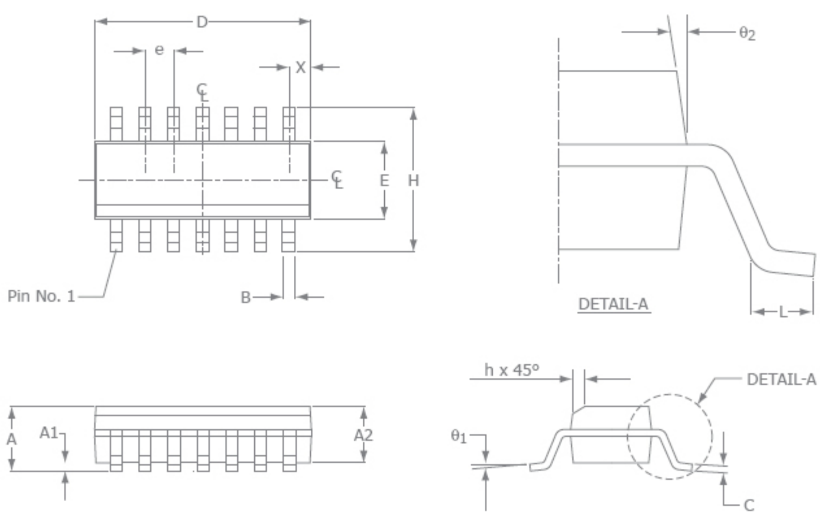
SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:
1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

SOIC-14 Package



SOIC-14		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	8.56	8.74
E	3.84	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.51 ref	
θ_2	7° BSC	

NOTE:
1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") ma
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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