

FAN7171_F085

High-Current High-Side Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- 4A/4A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input Signal
- Under- Voltage Lockout for V_{BS}
- 25V Shunt Regulator on V_{DD} and V_{BS}
- 8-Lead Small Outline Package (SOP)
- Qualified to AEC Q100

Applications

- High-Speed Gate Driver
- High-Power Buck Converter
- Motor Drive Inverter

Description

The FAN7171_F085 is a monolithic high-side gate drive IC, which can drive high-speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to $V_S = -9.8V$ (typical) for $V_{BS} = 15V$.


The UVLO circuit prevents malfunction when V_{BS} is lower than the specified threshold voltage.

The high-current and low-output voltage drop feature makes this device suitable for sustaine switch driver and energy recovery switch driver in the Plasma Display Panel application, motor drive inverter, switching power supply, and high-power DC-DC converter applications.

8-SOP



Ordering Information

| Part Number | Package | Operating Temperature Range |  Eco Status | Packing Method |
|--------------------------|---------|-----------------------------|---|----------------|
| FAN7171M ⁽¹⁾ | 8-SOP | -40°C ~ 125°C | RoHS | Tube |
| FAN7171MX ⁽¹⁾ | | | | Tape & Reel |

Note:

1. These devices passed wave soldering test by JESD22A-111.



For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Diagrams

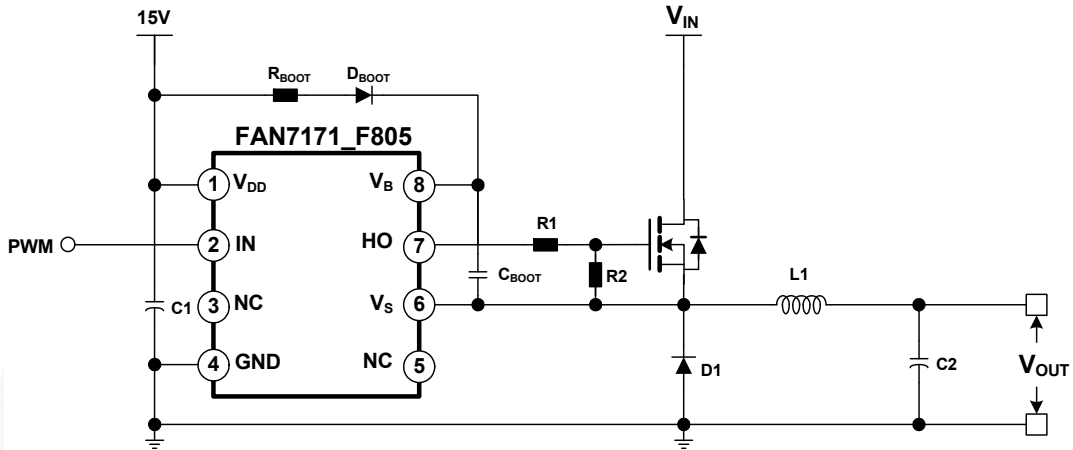


Figure 1. Application Circuit for Step-Down (Buck) DC-DC Converter

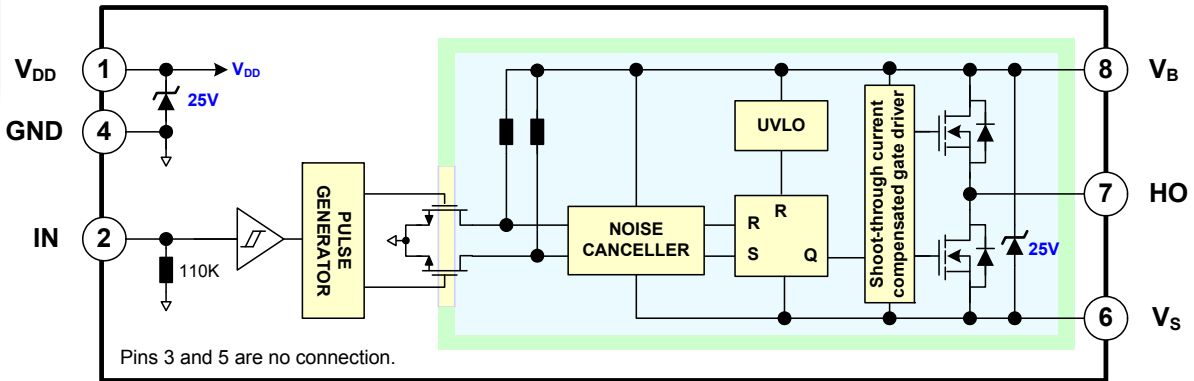


Figure 2. Functional Block Diagram

Pin Configuration

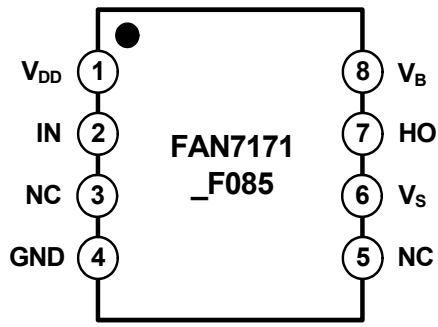


Figure 3. Pin Assignments(Top View)

Pin Definitions

| Pin # | Name | Description |
|-------|-----------------|--|
| 1 | V _{DD} | Supply Voltage |
| 2 | IN | Logic Input for High-Side Gate Driver Output |
| 3 | NC | No Connection |
| 4 | GND | Ground |
| 5 | NC | No Connection |
| 6 | V _S | High-Voltage Floating Supply Return |
| 7 | HO | High-Side Driver Output |
| 8 | V _B | High-Side Floating Supply |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Characteristics | Min. | Max. | Unit |
|---------------|--|-------------------|----------------|-----------------------------|
| V_S | High-Side Floating Offset Voltage | $V_B - V_{SHUNT}$ | $V_B + 0.3$ | V |
| V_B | High-Side Floating Supply Voltage ⁽²⁾ | -0.3 | 625.0 | V |
| V_{HO} | High-Side Floating Output Voltage | $V_S - 0.3$ | $V_B + 0.3$ | V |
| V_{DD} | Low-Side and Logic Supply Voltage ⁽²⁾ | -0.3 | V_{SHUNT} | V |
| V_{IN} | Logic Input Voltage | -0.3 | $V_{DD} + 0.3$ | V |
| dV_S/dt | Allowable Offset Voltage Slew Rate | | ± 50 | V/ns |
| P_D | Power Dissipation ^(3, 4, 5) | | 0.625 | W |
| θ_{JA} | Thermal Resistance | | 200 | $^{\circ}\text{C}/\text{W}$ |
| T_J | Junction Temperature | -55 | 150 | $^{\circ}\text{C}$ |
| T_{STG} | Storage Temperature | -55 | 150 | $^{\circ}\text{C}$ |
| T_A | Operating Ambient Temperature | -40 | 125 | $^{\circ}\text{C}$ |
| V_{ESD} | Human Body Model(HBM) | | 1500 | V |
| V_{CDM} | Charge Device Model | | 500 | V |

Notes:

- This IC contains a shunt regulator on VDD and VBS with a normal breakdown voltage of 25V. Please note that this supply pin should not be driven by a low-impedance voltage source greater than the VSHUNT specified in the Electrical Characteristics section
- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
JESD51-2: Integral circuits thermal test method environmental conditions, natural convection, and
JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
- Do not exceed power dissipation (P_D) under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|----------|---|-----------------------|------------|------|
| V_{BS} | High-Side Floating Supply Voltage | $V_S + 10$ | $V_S + 20$ | V |
| V_S | High-Side Floating Supply Offset Voltage(DC) | $6 - V_{DD}$ | 600 | V |
| V_S | High-Side Floating Supply Offset Voltage(Transient) | -15(~170) -7(~400) | 600 | V |
| V_{HO} | High-Side Output Voltage | V_S | V_B | V |
| V_{IN} | Logic Input Voltage | GND | V_{DD} | V |
| V_{DD} | Supply Voltage | 10 | 20 | V |

Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})=15.0V$, $-40^{\circ}C \leq T_A \leq 125^{\circ}C$, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are relative to V_S and are applicable to the respective output HO.

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---------------------------------------|--|--|------|------|------|-----------|
| POWER SUPPLY SECTION | | | | | | |
| I_{QDD} | Quiescent V_{DD} Supply Current | $V_{IN}=0V$ or $5V$ | | 25 | 70 | μA |
| I_{PDD} | Operating V_{DD} Supply Current | $f_{IN}=20KHz$, No Load | | 35 | 100 | μA |
| BOOTSTRAPPED SUPPLY SECTION | | | | | | |
| V_{BSUV+} | V_{BS} Supply Under-Voltage Positive Going Threshold Voltage | $V_{BS}=\text{Sweep}$ | 8.2 | 9.2 | 10.2 | V |
| V_{BSUV-} | V_{BS} Supply Under-Voltage Negative Going Threshold Voltage | $V_{BS}=\text{Sweep}$ | 7.5 | 8.5 | 9.5 | V |
| V_{BSHYS} | V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage | $V_{BS}=\text{Sweep}$ | | 0.6 | | V |
| I_{LK} | Offset Supply Leakage Current | $V_B=V_S=600V$ | | | 50 | μA |
| I_{QBS} | Quiescent V_{BS} Supply Current | $V_{IN}=0V$ or $5V$ | | 60 | 120 | μA |
| I_{PBS} | Operating V_{BS} Supply Current | $C_{LOAD}=1nF$, $f_{IN}=20KHz$, rms value | | 0.73 | 2.8 | mA |
| SHUNT REGULATOR SECTION | | | | | | |
| V_{SHUNT} | V_{DD} and V_{BS} Shunt Regulator Clamping Voltage | $I_{SHUNT}=5mA$ | 23 | 25 | | V |
| INPUT LOGIC SECTION(IN) | | | | | | |
| V_{IH} | Logic "1" Input Voltage | | 2.5 | | | V |
| V_{IL} | Logic "0" Input Voltage | | | | 0.8 | V |
| I_{IN+} | Logic Input High Bias Current | $V_{IN}=5V$ | | 45 | 125 | μA |
| I_{IN-} | Logic Input Low Bias Current | $V_{IN}=0V$ | | | 2 | μA |
| R_{IN} | Input Pull-down Resistance | | 40 | 110 | | $K\Omega$ |
| GATE DRIVER OUTPUT SECTION(HO) | | | | | | |
| V_{OH} | High Level Output Voltage ($V_{BIAS} - V_O$) | No Load | | | 1.5 | V |
| V_{OL} | Low Level Output Voltage | No Load | | | 35 | mV |
| I_{O+} | Output High, Short-Circuit Pulsed Current ⁽⁵⁾ | $V_{HO}=0V$, $V_{IN}=5V$, $PW \leq 10\mu s$ | 3.0 | 4.0 | | A |
| I_{O-} | Output Low, Short-Circuit Pulsed Current ⁽⁵⁾ | $V_{HO}=15V$, $V_{IN}=0V$, $PW \leq 10\mu s$ | 3.0 | 4.0 | | A |
| V_S | Allowable Negative V_S pin Voltage for IN Signal Propagation to HO | | | -9.8 | -7.0 | V |

Note:

5 These parameters guaranteed by design.

Dynamic Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})=15V$, $V_S=GND=0V$, $C_L=1000pF$, and $-40^{\circ}C \leq T_A \leq 125^{\circ}C$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------|------------|------|------|------|------|
| t_{on} | Turn-on Propagation Delay Time | $V_S=0V$ | | 150 | 210 | ns |
| t_{off} | Turn-off Propagation Delay Time | $V_S=0V$ | | 150 | 210 | ns |
| t_r | Turn-on Rise Time | | | 25 | 50 | ns |
| t_f | Turn-off Fall Time | | | 15 | 45 | ns |

Typical Characteristics

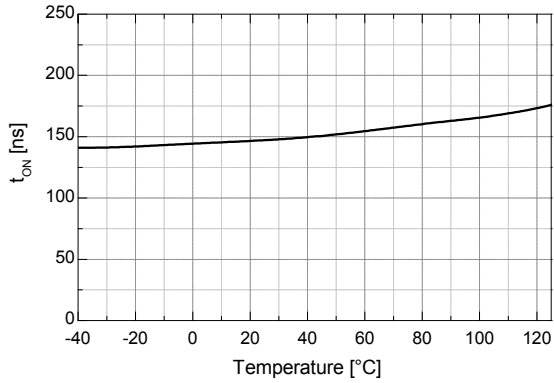


Figure 4. Turn-on Propagation Delay vs. Temperature

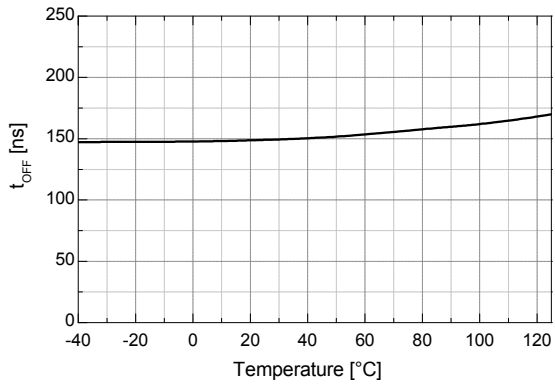


Figure 5. Turn-off Propagation Delay vs. Temperature

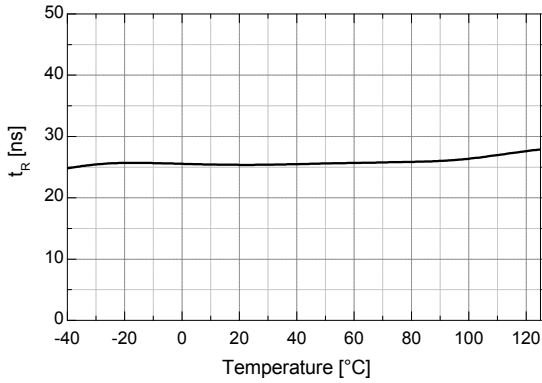


Figure 6. Turn-on Rise Time vs. Temperature

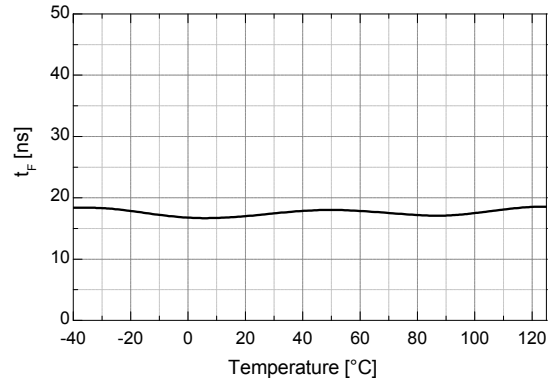


Figure 7. Turn-off Fall Time vs. Temperature

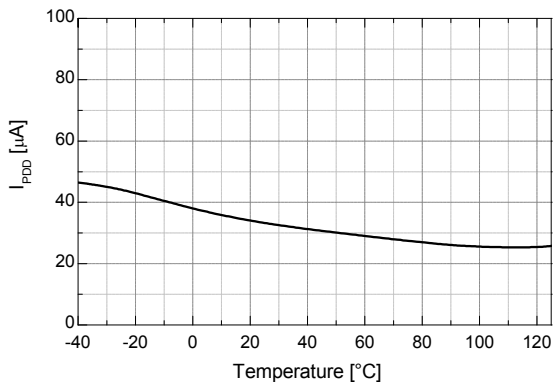


Figure 8. Operating V_{DD} Supply Current vs. Temperature

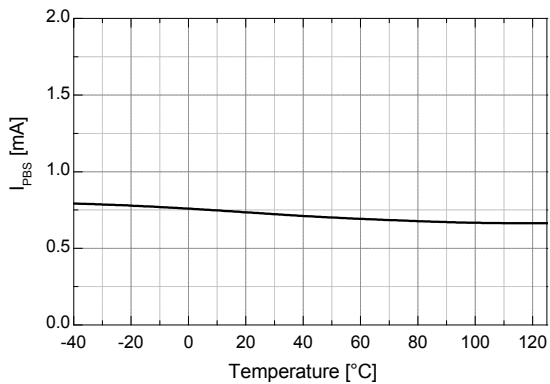


Figure 9. Operating V_{BS} Supply Current vs. Temperature

Typical Characteristics (Continued)

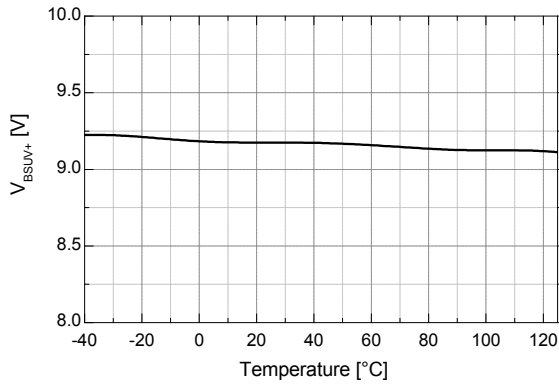


Figure 10. $V_{BS\ UVLO+}$ vs. Temperature

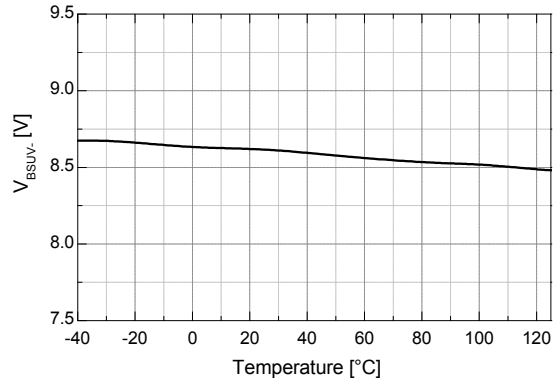


Figure 11. $V_{BS\ UVLO-}$ vs. Temperature

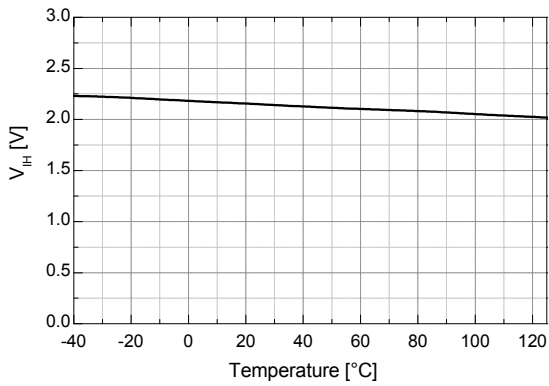


Figure 12. Logic High Input Voltage vs. Temperature

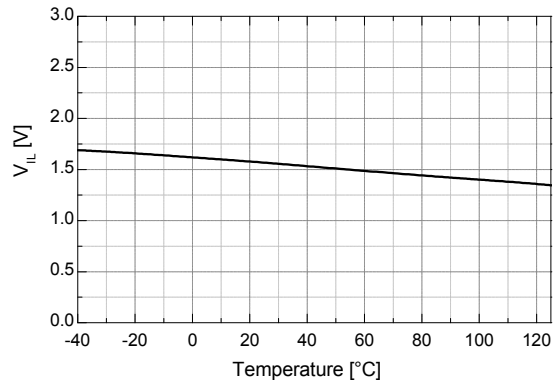


Figure 13. Logic Low Input Voltage vs. Temperature

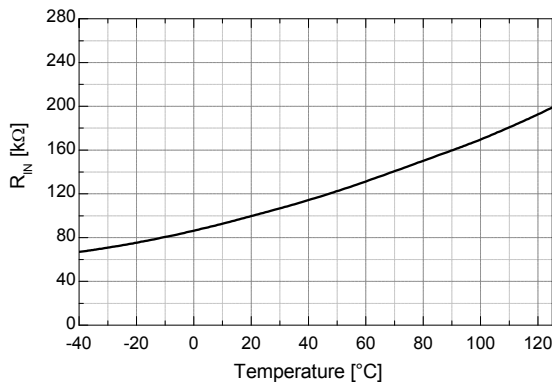


Figure 14. Input Pull-down Resistance vs. Temperature.

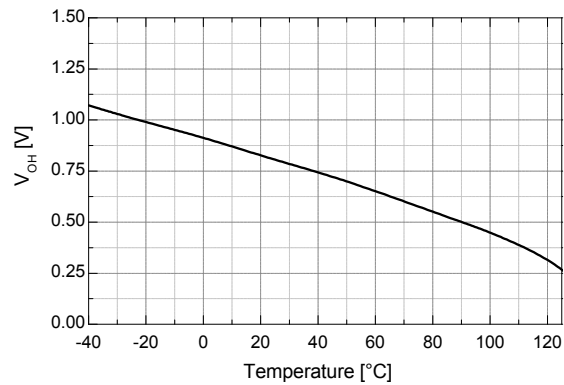


Figure 15. High-Level Output Voltage vs. Temperature

Typical Characteristics (Continued)

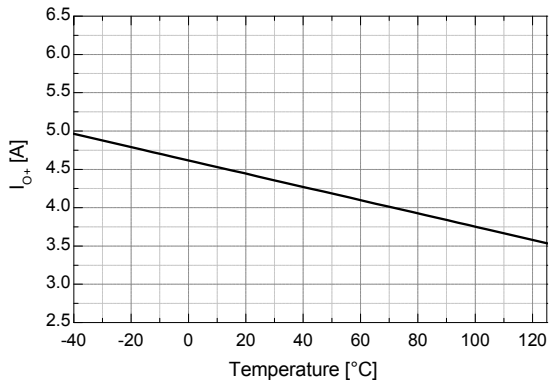


Figure 16. Output High, Short-Circuit Pulsed Current vs. Temperature

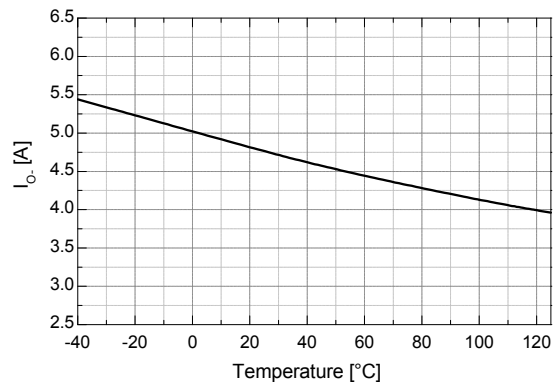


Figure 17. Output Low, Short-Circuit Pulsed Current vs. Temperature

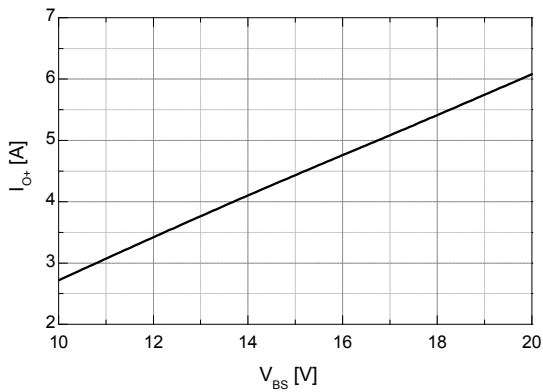


Figure 18. Output High, Short-Circuit Pulsed Current vs. Supply Voltage

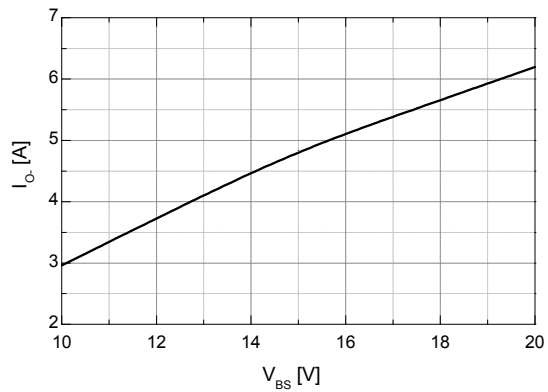


Figure 19. Output Low, Short-Circuit Pulsed Current vs. Supply Voltage

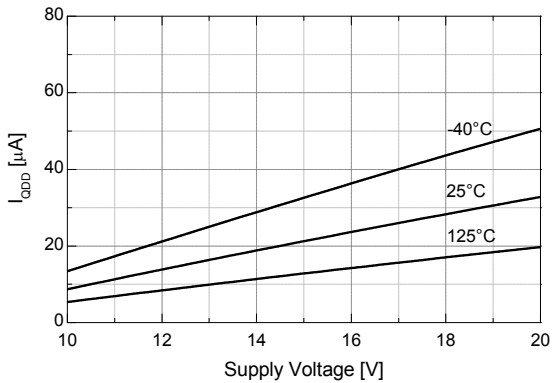


Figure 20. Quiescent V_{DD} Supply Current vs. Supply Voltage

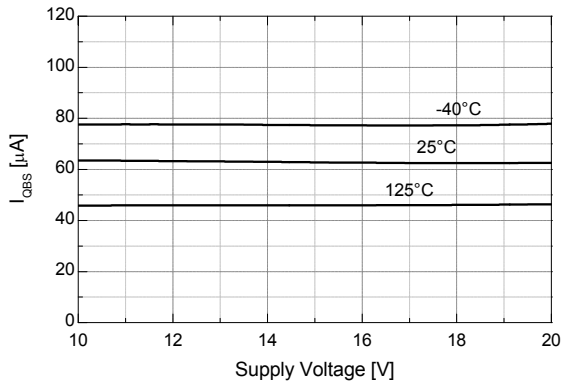


Figure 21. Quiescent V_{BS} Supply Current vs. Supply Voltage

Switching Time Definitions

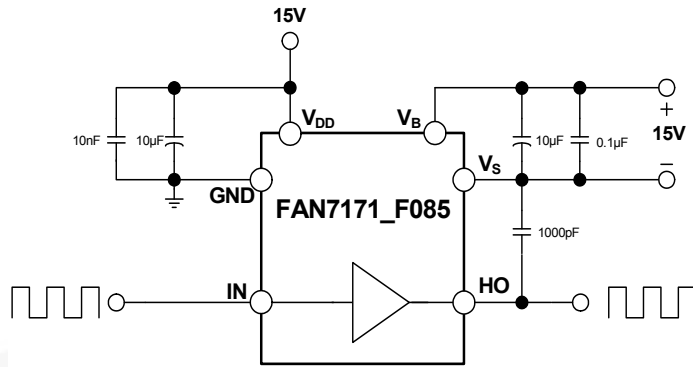


Figure 22. Switching Time Test Circuit (Referenced 8-SOP)

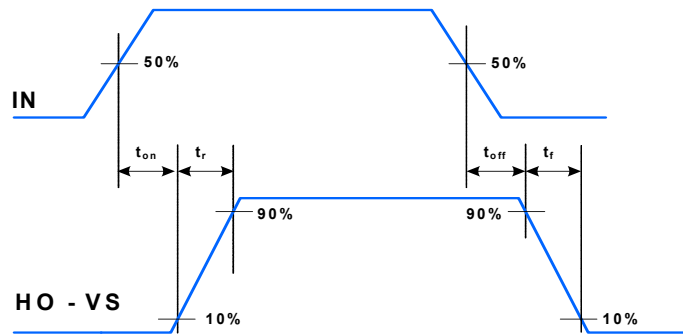


Figure 23. Switching Time Waveform Definitions

Physical Dimensions

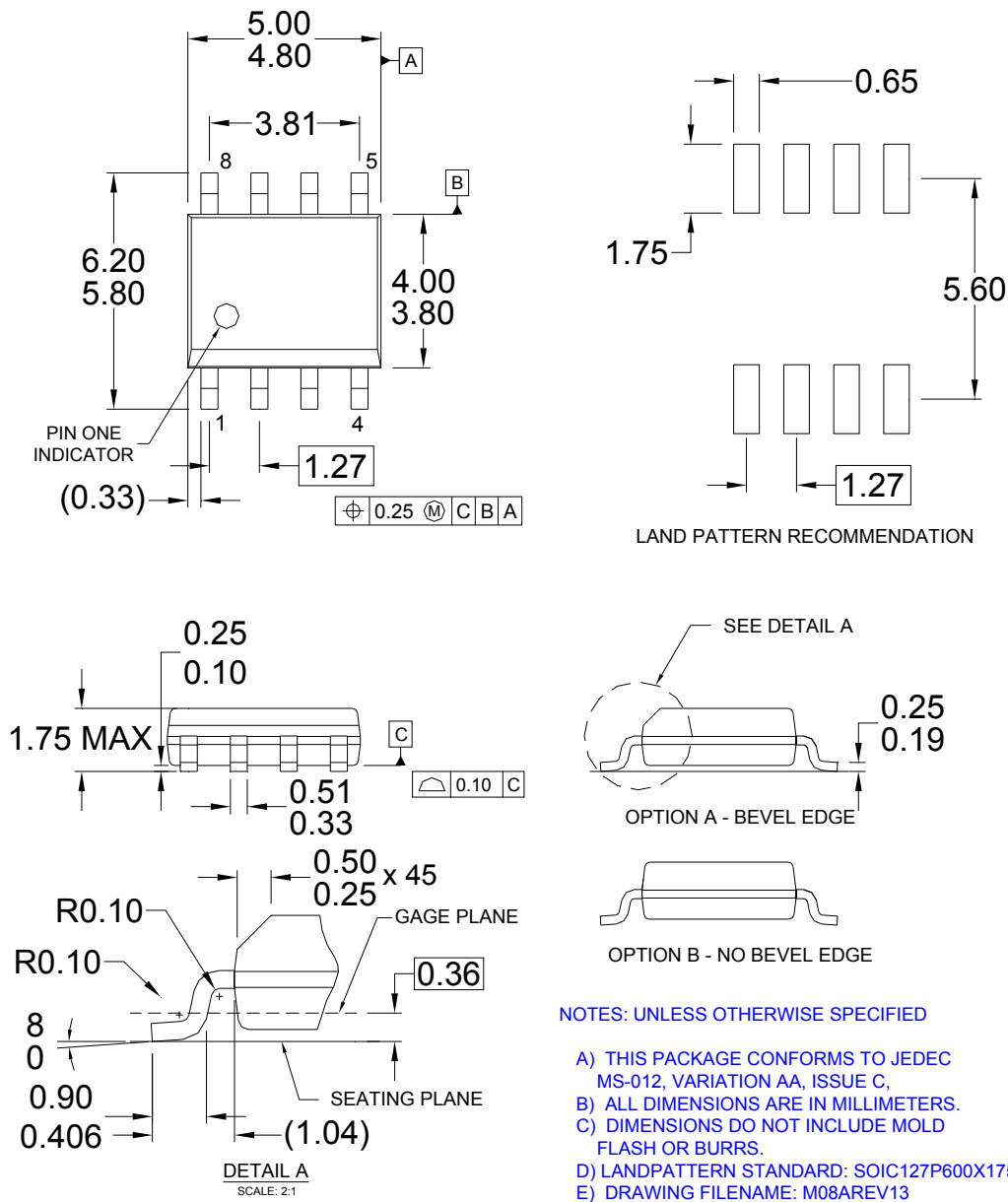


Figure 24. 8-Lead Small Outline Package (SOP)

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