March 2009

FAN7080_F085
Half Bridge Gate Driver

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- VS-pin dv/dt immune.
- Gate drive supply range from 5.5V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- High side output in phase with input
- IN input is 3.3V/5V logic compatible and available on 15V input
- Matched propagation delay for both channels
- Dead time adjustable

Typical Applications

- Junction Box
- Half and full bridge application in the motor drive system

Description

The FAN7080_F085_F085 is a half-bridge gate drive IC with reset input and adjustable dead time control. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to VS=-5V (typical) at VBS=15V. Logic input is compatible with standard CMOS outputs. The UVLO circuits for both channels prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. Combined pin function for dead time adjustment and reset shutdown make this IC packaged with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 500mA respectively, which is suitable for junction box application and half and full bridge application in the motor drive system.

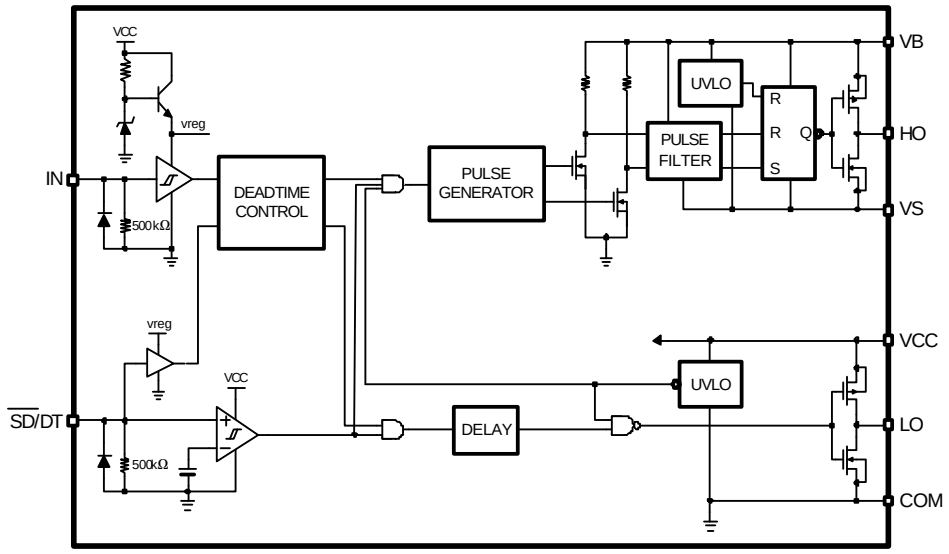
SOIC-8

Ordering Information

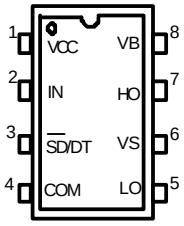
Device	Package	Operating Temp.
FAN7080CM	SOIC-8	-40 °C ~ 125 °C
FAN7080CMX	SOIC-8	-40 °C ~ 125 °C

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

Pine Number	Pin Name	I/O	Pin Function Description
1	VCC	P	Driver supply voltage
2	IN	I	Logic input for high and low side gate drive output
3	$\overline{SD}$/DT	I	Shut down input and dead time setting
4	COM	P	Ground
5	LO	A	Low side gate drive output for MOSFET Gate connection
6	VS	A	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	VB	P	Driver output stage supply

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply offset voltage	V_S	V_B-25	V_B+0.3	V
High side floating supply voltage	V_B	-0.3	625	V
High side floating output voltage	V_{HO}	Vs-0.3	V_B+0.3	V
Low side output voltage	V_{LO}	-0.3	V_{CC} + 0.3	V
Supply voltage	V_{CC}	-0.3	25	V
Input voltage for $\overline{IN}$	VIN	-0.3	Vcc+0.3	V
Input injection current. Full function, no latch up;(Guaranteed by design). Test at 10V and 17V on Eng.Samples	I_{IN}	-	+1	mA
Power Dissipation	Pd		0.625	W
Thermal resistance, junction to ambient	Rthja		200	°C/W
Electrostatic discharge voltage (Human Body Model)	V_{ESD}	1K		V
Charge device model	V_{CDM}	500		V
Junction Temperature	Tj		150	℃
Storage Temperature	T_S	-55	150	℃

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural convection(StillAir)

JESD51-3 : Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply voltage(DC) Transient:-10V@ 0.1 us	VB [1)]	V_S + 6	V_S + 20	V
High side floating supply offset voltage(DC) Transient: -25V(max) @0.1us @VBS<25V	V_S	-5	600	V
High side floating output voltage	V_{HO}	Vs	V_B	V
Low side output voltage	V_{LO}	0	V_{CC}	V
Allowable offset voltage Slew Rate [2)]	dv/dt	-	50	V/ns
Supply voltage for logic part	V_{CC}	5.5	20	V
Logic input voltage	V_{IN}	0	Vcc	V
Switching Frequency [3)]	F_S		200	KHz
Ambient Temperature	Ta	-40	125	℃

Note: 1) The Vs offset is tested with all supplies biased at 15V differential.

2) Guaranteed by design.

3) When VDT= 1.2V.

Statics Electrical Characteristics

Unless otherwise specified, -40°C <= Ta <= 125°C, V_{CC} = 15V, V_{BS} = 15V, V_S = 0V, C_L = 1nF.

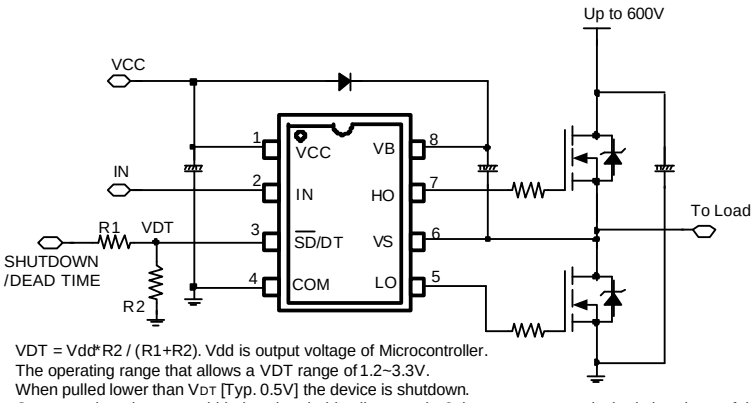
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vcc and VBS supply Characteristics						
V_{CC} and V_{BS} supply under voltage positive going threshold	V_{CCUV+} V_{BSUV+}	-	-	4.2	5.5	V
V_{CC} and V_{BS} supply under voltage negative going threshold	V_{CCUV-} V_{BSUV-}	-	2.8	3.6	-	V
V_{CC} and V_{BS} supply under voltage hysteresis	V_{CCUVH} V_{BSUVH}	-	0.2	0.6	-	V
Under voltage lockout response time	tduvcc tduvbs	VCC: 6V-->2.5V or 2.5V-->6V VBS: 6V-->2.5V or 2.5V-->6V	0.5 0.5	- -	20 20	us us
Offset supply leakage current	I_{LK}	V_B=V_S=600V	-	20	50	uA
Quiescent V_{BS} supply current	I_{QBS}	V_{IN}=0 OR 5V, V_{SDT} = 1.2V	20	75	150	uA
Quiescent Vcc supply current	I_{QCC}	V_{IN}=0 OR 5, V_{SDT} = 1.2V	-	350	1000	uA
Input Characteristics						
High logic level input voltage	V_{IH}		2.7	-	-	V
Low logic level input voltage	V_{IL}		-	-	0.8	V
High logic level input bias current for IN	I_{IN+}	V_{IN}=5V	-	10	50	uA
Low logic level input bias current for IN	I_{IN-}	V_{IN}=0V	-	0	2	uA
VSDT dead time setting range	V_{DT}		1.2	-	5	V
VSDT shutdown threshold voltage	V_{SD}		-	0.8	1.2	V
High logic level resistance for $\overline{SD}$/DT	R_{SDT}	V_{SDT}=5V	100	500	1100	KΩ
Low logic level input bias current for $\overline{SD}$/DT	I_{SDT-}	V_{SDT}=0V	-	1	2	uA
Output characteristics						
High level output voltage, V_{CC}-V_{HO}	$V_{OH(HO)}$	I_O=0	-	-	0.1	V
Low level output voltage, V_{HO}	$V_{OL(HO)}$	I_O=0	-	-	0.1	V
Output high short circuit pulse current	$I_{O+(HO)}$		250	300	-	mA
Output low short circuit pulse current	$I_{O-(HO)}$		500	600	-	mA
Equivalent output resistance	$R_{OP(HO)}$		-	-	60	Ω
	$R_{ON(HO)}$		-	-	30	Ω
High level output voltage, V_B-V_{LO}	$V_{OH(LO)}$	I_O=0	-	-	0.1	V
Low level output voltage, V_{LO}	$V_{OL(LO)}$	I_O=0	-	-	0.1	V
Output high short circuit pulse current	$I_{O+(LO)}$		250	-	-	mA
Output low short circuit pulse current	$I_{O-(LO)}$		500	-	-	mA
Equivalent output resistance	$R_{OP(LO)}$		-	-	60	Ω
	$R_{ON(LO)}$		-	-	30	Ω

Dynamic Electrical Characteristics

Unless otherwise specified, -40°C <= Ta <= 125°C, V_{CC} = 15V, V_{BS} = 15V, V_S = 0V, C_L = 1nF.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	ton	V_S=0V	-	750	1500	ns
Turn-off propagation delay	toff	V_S=0V	-	130	250	ns
Turn -on rising time	tr	-	-	40	150	ns
Turn -off falling time	tf	-	-	25	400	ns
Dead time, LS turn-off to HS turn-on and HS turn-on to LS turn-off	DT	V_{IN}=0 or 5V@ VDT=1.2V V_{IN}=0 or 5V@ VDT=3.3V	250 1600	650 2100	1200 2600	ns
Dead time matching time	MDT	DT1 -DT2@ VDT=1.2V DT1 -DT2@ VDT=3.3V	-	35 -	110 300	ns
Delay Matching, HS and LS turn-on	MTON	VDT=1.2V	-	25	110	ns
Delay Matching, HS and LS turn-off	MTOFF	VDT=1.2V		15	60	ns
Shutdown propagation delay	Tsd		-	180	330	ns
Switching Frequency	Fs1	V_{CC}=V_{BS}=20V	-	-	200	KHz
	Fs2	V_{CC}=V_{BS}=5.5V	-	-	200	KHZ

Typical Application Circuit



VDT = Vdd*R2 / (R1+R2). Vdd is output voltage of Microcontroller.
The operating range that allows a VDT range of 1.2~3.3V.
When pulled lower than V_{DT} [Typ. 0.5V] the device is shutdown.
Care must be taken to avoid below threshold spikes on pin 3 that can cause undesired shut down of the IC. For this reason the connection of the components between pin 3 and ground has to be as short as possible. And a capacitor (Typ 0.02uF)between pin3 and COM can prevent this spike. This pin can not be left floating for the same reason.

Typical Waveforms

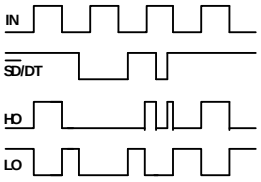


Figure 1. Input/output Timing Diagram

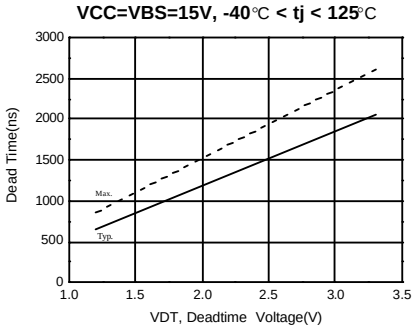


Figure 2. Dead Time VS V_{DT}

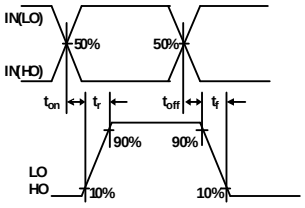


Figure 3. Switching Time Waveform Definitions

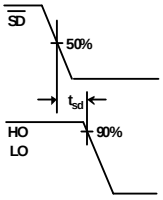


Figure 4. Shutdown Waveform Definitions

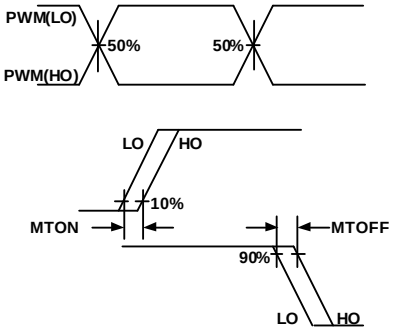


Figure 5. Delay Matching Waveform Definitions

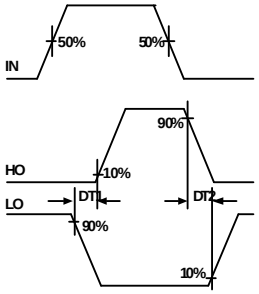


Figure 6. Dead Time Waveform Definitions

Performance Graphs(This performance graphs based on ambient temperature -40°C ~125°C)

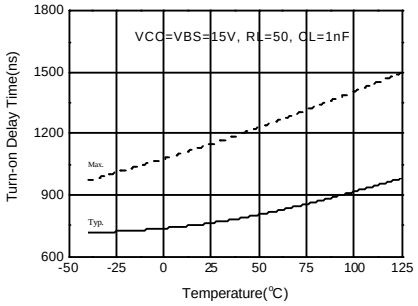


Figure 7a. Turn-On Delay Time of HO vs VBS Temperature

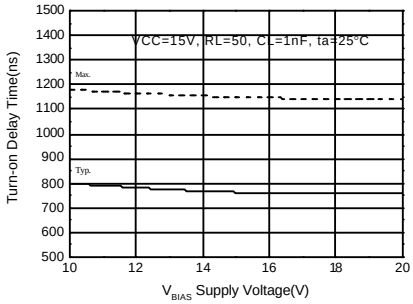


Figure 7b. Turn-On Delay Time of HO vs VBS Supply Voltage

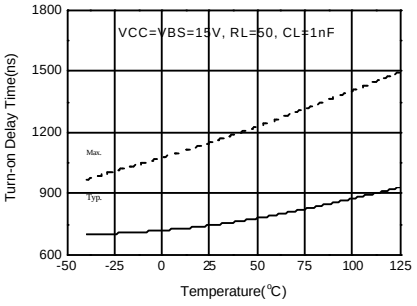


Figure 8a. Turn-On Delay Time of LO vs Temperature

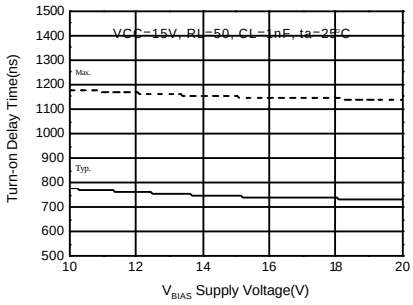


Figure 8b. Turn-On Delay Time vs of LO VBS Supply Voltage

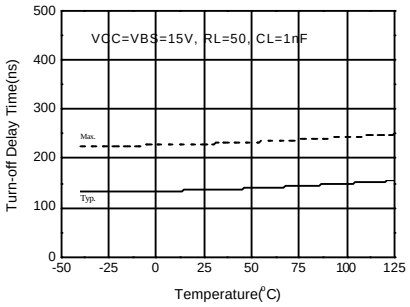


Figure 9a. Turn-Off Delay Time of HO vs Temperature

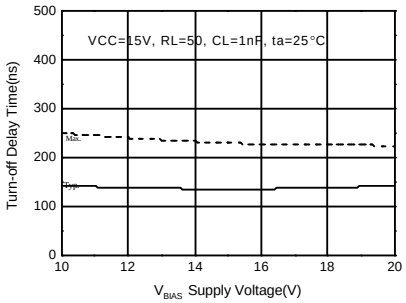


Figure 9b. Turn-Off Delay Time of HO vs VBS Supply Voltage

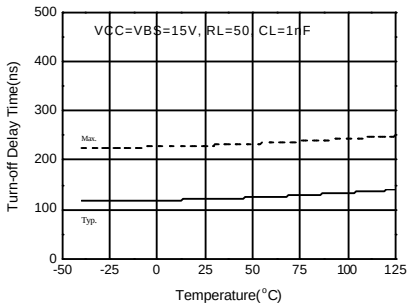


Figure 10a. Turn-Off Delay Time of LO vs Temperature

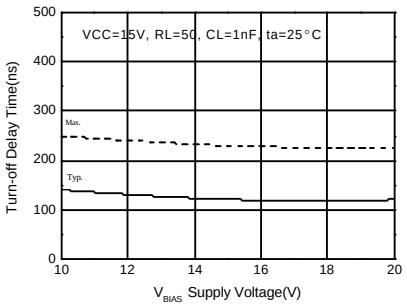


Figure 10b. Turn-Off Delay Time of LO vs VBS Supply Voltage

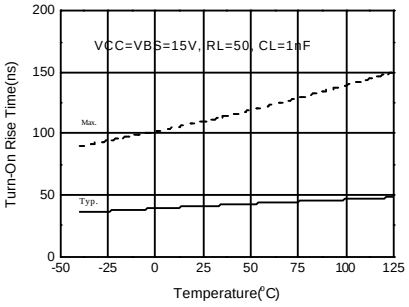


Figure 11a. Turn-On Rise Time of HO vs Temperature

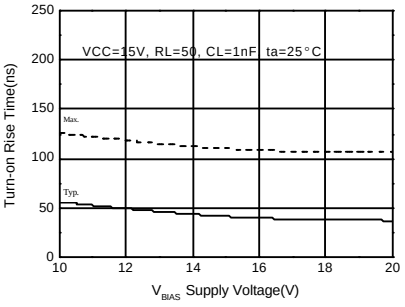


Figure 11b. Turn-On Rise Time vs of HO VBS Supply Voltage

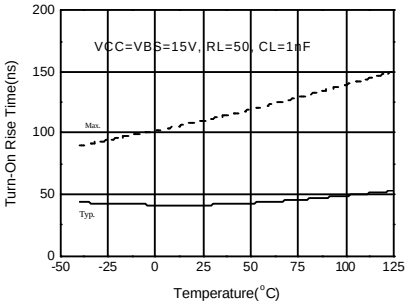


Figure 12a. Turn-On Rise Time of LO vs Temperature

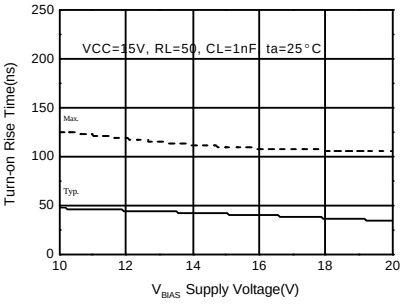


Figure 12b. Turn-On Rise Time of LO vs VBS Supply Voltage

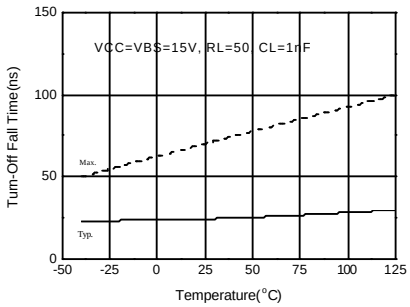


Figure 13a. Turn-Off Fall Time of HO vs Temperature

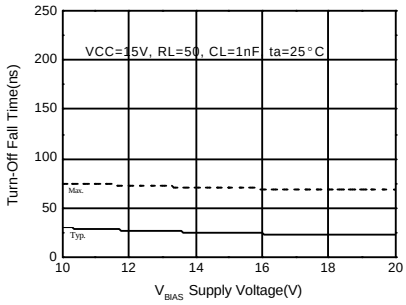


Figure 13b. Turn-Off Fall Time of HO vs VBS Supply Voltage

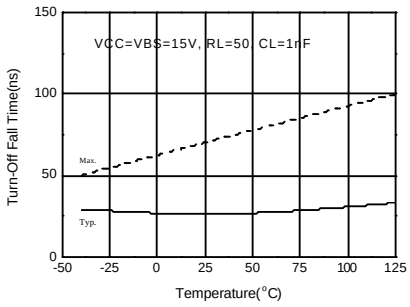


Figure 14a. Turn-Off Fall Time of LO vs Temperature

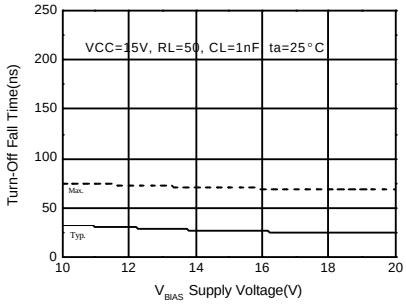


Figure 14b. Turn-Off Fall Time of LO vs BS Supply Voltage

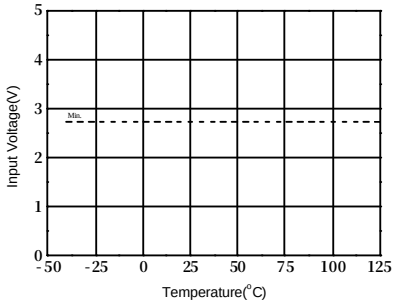


Figure 15a. Logic 0 Input Voltage vs Temperature

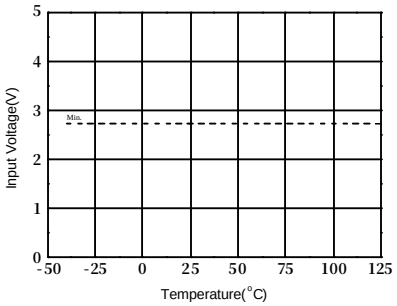


Figure 15b. Logic 1 Input Voltage vs Temperature

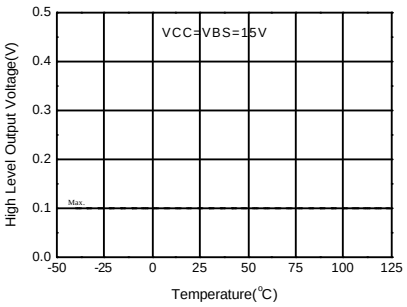


Figure 16a. High Level Output of HO vs Temperature

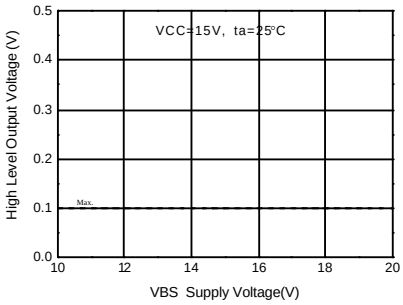


Figure 16b. High Level Output of HO vs VBS Supply Voltage

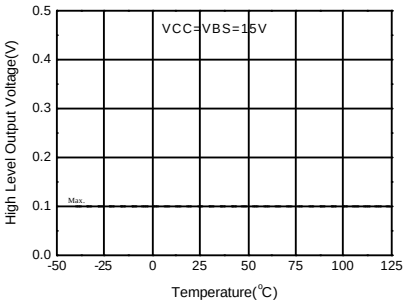


Figure 17a. High Level Output of LO vs Temperature

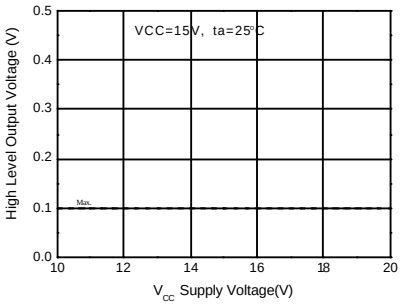


Figure 17b. High Level Output of LO vs VCC Supply Voltage

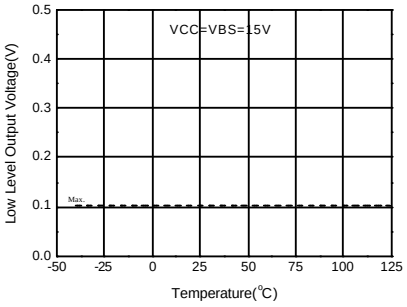


Figure 18a. Low Level Output of HO vs Temperature

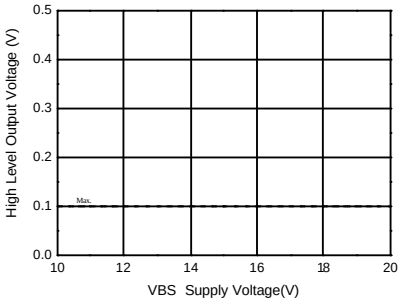


Figure 18b. Low Level Output of HO vs VBS Supply Voltage

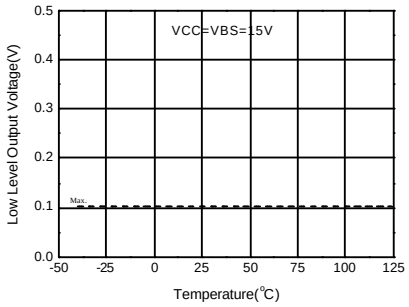


Figure 19a. Low Level Output of LO vs Temperature

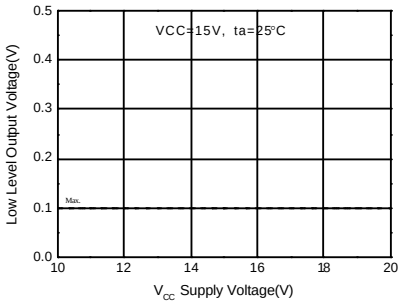


Figure 19b. Low Level Output of LO vs VCC Supply Voltage

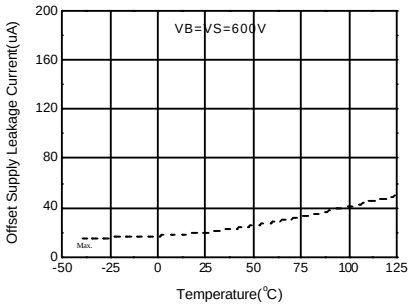


Figure 20a. Offset Supply leakage Current vs Temperature

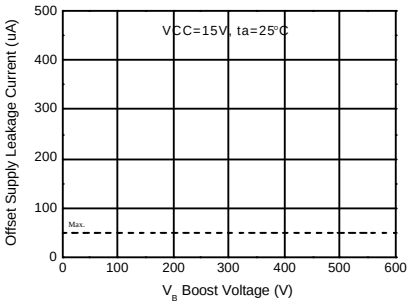


Figure 20b. Offset Supply leakage Current vs VB Boost Voltage

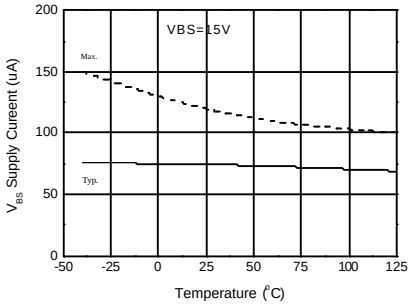


Figure 21. VBS Supply Current vs Temperature

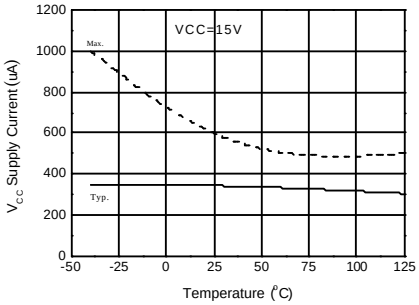


Figure 22. VCC Supply Current vs Temperature

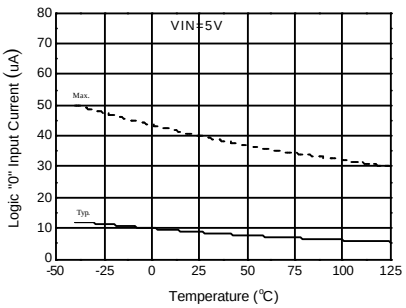


Figure 23a. Logic 1 Input Current vs Temperature

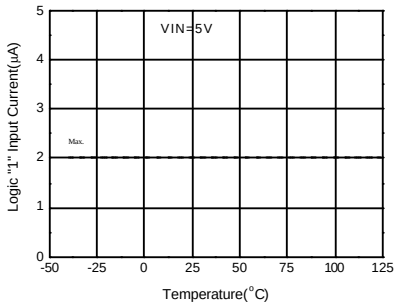


Figure 23b. Logic 0 Input Current vs Temperature

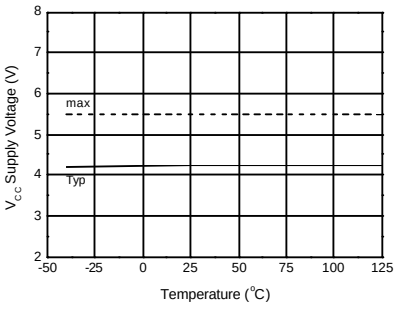


Figure 24a. VCC UnderVoltage Threshold (+) vs Temperature

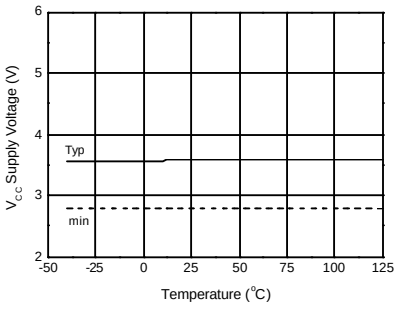


Figure 24b. VCC UnderVoltage Threshold(-) vs Temperature

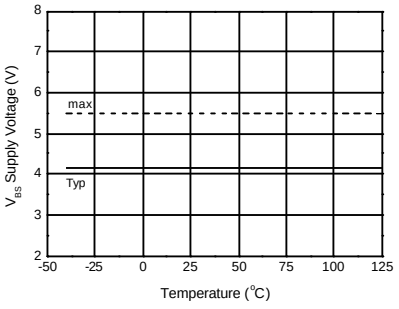


Figure 25a. VBS UnderVoltage Threshold (+) vs Temperature

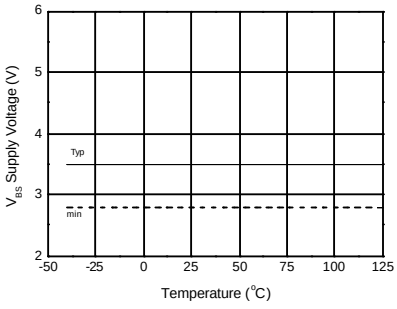


Figure 25b.VBS UnderVoltage Threshold(-) vs Temperature

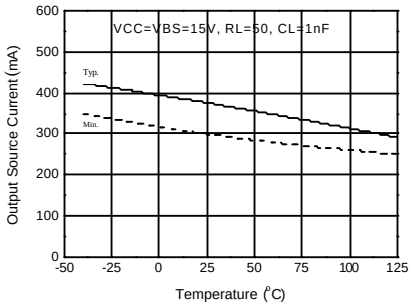


Figure 26a. Output Source Current of HO vs Temperature

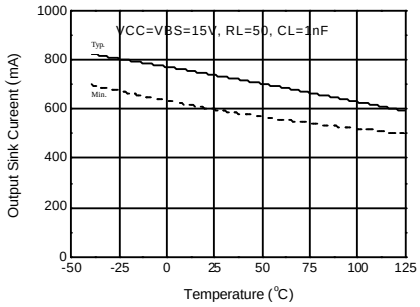


Figure 26b. Output Sink Current of HO vs Temperature

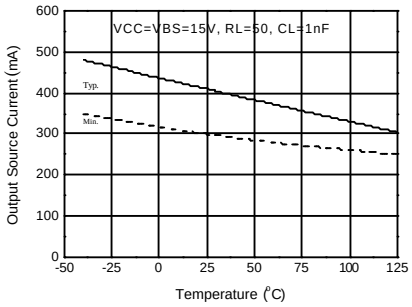


Figure 27a. Output Source Current of LO vs Temperature

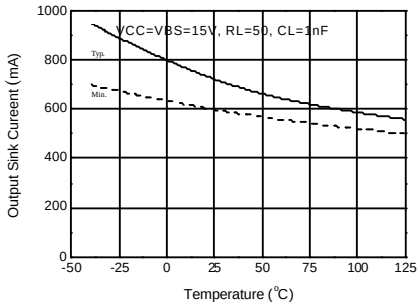


Figure 27b. Output Sink Current of LO vs Temperature

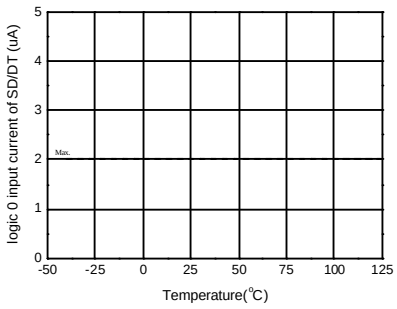


Figure 28. Logic 0 Input Current of SD/DT vs Temperature

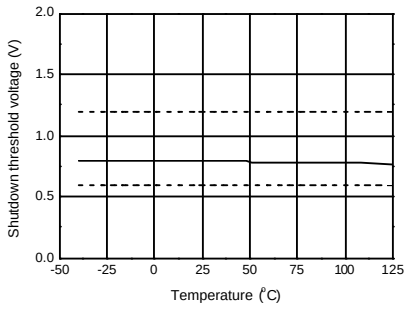


Figure 29.Shutdown Threshold of vs Temperature

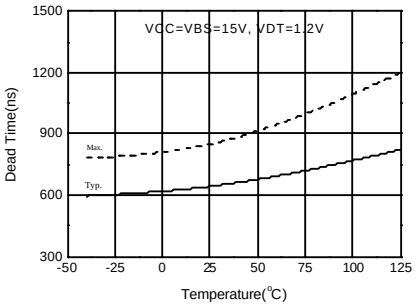


Figure 30. Deadtime vs Temperature

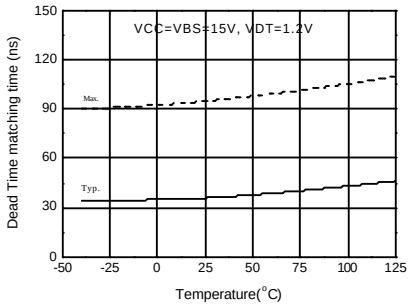


Figure 31. Deadtime Matching Time vs Temperature

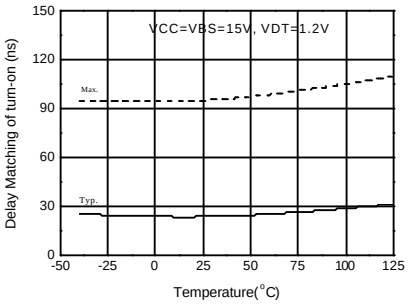


Figure 32. Turn-On Delay Matching vs Temperature

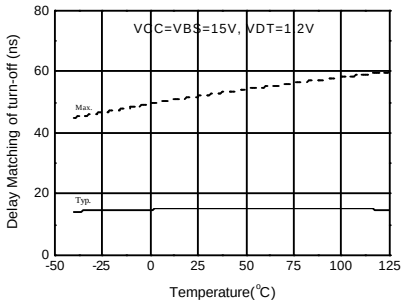


Figure 33. Turn_Off Delay Matching vs Temperature

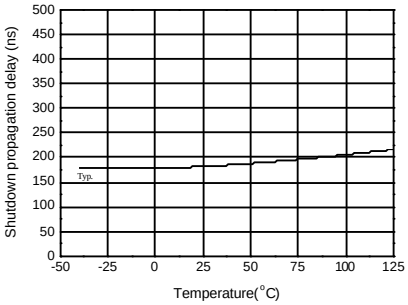


Figure 34. Shutdown Propagation Delay vs Temperature

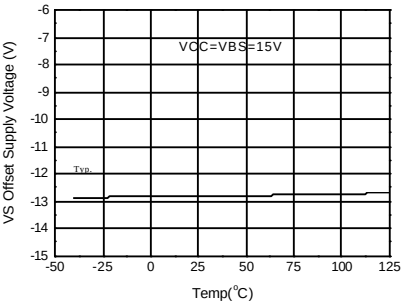


Figure35. Maximum VS Negtive Offset of vs Temperature

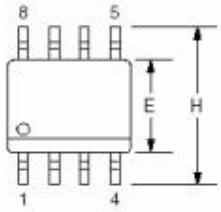
Package Dimensions

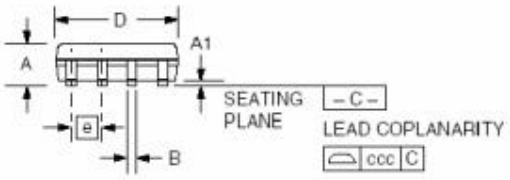
8-SOP

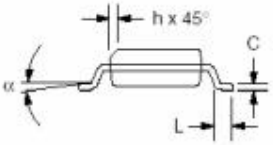
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







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