TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCXR162500FT

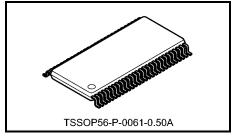
Low-Voltage 18-Bit Universal Bus Transceiver with 3.6-V Tolerant Inputs and Outputs

The TC74VCXR162500FT is a high-performance CMOS 18-bit universal bus transceiver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to $3.6~\mathrm{V}.$

Data flow in each direction is controlled by output-enable (OEAB and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (\overline{CKAB} and \overline{CKBA}) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CKAB}}$ is held at a high or low logic level. If LEAB is



Weight: 0.25 g (typ.)

low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of CKAB.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CKBA}}$.

When the $\overline{\text{OE}}$ input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The $26 \cdot \Omega$ series resistor helps reducing output overshoot and undershoot without external resistor. All inputs are equipped with protection circuits against static discharge.

Features (Note)

- 26-Ω series resistors on outputs
- Low-voltage operation: VCC = 1.8 to 3.6 V
- High-speed operation: $t_{pd} = 3.8 \text{ ns (max) (VCC} = 3.0 \text{ to } 3.6 \text{ V)}$

 $t_{rd} = 4.9 \text{ ns (max) (VCC} = 2.3 \text{ to } 2.7 \text{ V)}$

 $: t_{pd} = 9.8 \text{ ns (max) (V}_{CC} = 1.8 \text{ V})$

• Output current: $I_{OH}/I_{OL} = \pm 12 \text{ mA (min)} (V_{CC} = 3.0 \text{ V})$

 $: I_{OH}/I_{OL} = \pm 8 \text{ mA (min) (V}_{CC} = 2.3 \text{ V)}$

: $IOH/IOL = \pm 4 \text{ mA (min) (VCC} = 1.8 \text{ V)}$

- Latch-up performance: -300 mA
- ESD performance: Machine model $\geq \pm 200 \text{ V}$

Human body model ≥ ±2000 V

- Package: TSSOP
- Bidirectional interface between 2.5 V and 3.3 V signals.
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

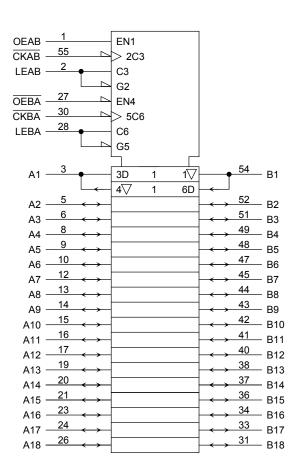
All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

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Pin Assignment (top view)

OEAB 56 GND LEAB 2 CKAB Α1 3 54 B1 GND 4 GND 53 A2 5 52 B2 А3 6 51 B3 7 Vcc 50 Vcc 8 A4 49 B4 Α5 9 B5 A6 10 B6 GND 11 46 **GND** A7 12 45 B7 A8 13 B8 В9 Α9 14 43 A10 15 42 B10 A11 16 B11 41 B12 A12 17 GND 18 GND A13 19 38 B13 A14 20 B14 37 A15 21 36 B15 V_{CC} 22 35 V_{CC} A16 23 B16 A17 24 B17 33 GND 25 **GND** A18 26 31 B18 OEBA 27 CKBA LEBA 28 GND 29

IEC Logic Symbol



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Truth Table (A bus \rightarrow B bus)

	Inputs					
OEAB	LEAB	CKAB	Α	В		
L	Х	Х	Х	Z		
Н	Н	Х	L	L		
Н	Н	Х	Н	Н		
Н	L	\neg	L	L		
Н	L	\rightarrow	Н	Н		
Н		Н	Х	В0		
П	L	П	^	(Note)		
Н			Х	В0		
П	L	ı	^	(Note)		

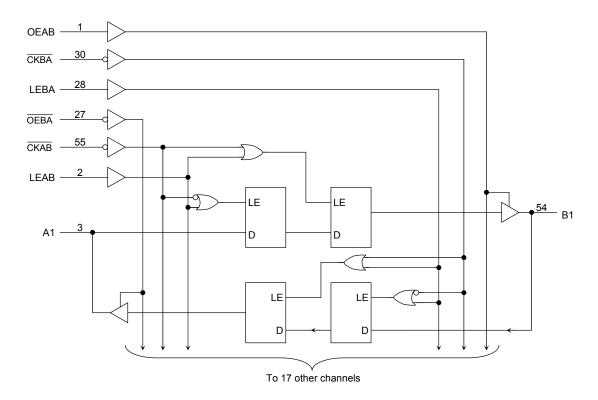
Note: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CKAB}}$ was low or high before LEAB went low.

Truth Table (B bus \rightarrow A bus)

	Inputs					
OEBA	LEBA	CKBA	В	Α		
Н	Х	Х	Х	Z		
L	Н	Х	L	L		
L	Н	Х	Н	Н		
L	L	\neg	L	L		
L	L	\neg	Н	Н		
	1	Н	Х	A0		
L	L	П	^	(Note)		
	1		Х	A0		
_	Ĺ	L	^	(Note)		

Note: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CKBA}}$ was low or high before LEBA went low.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	−0.5 to 4.6	V
DC input voltage (OEAB, OEBA, LEAB, LEBA, CKAB, CKBA)	VIN	-0.5 to 4.6	V
		-0.5 to 4.6 (Note 2)	
DC bus I/O voltage	V _{I/O}	-0.5 to V_{CC} + 0.5	V
		(Note 3)	
Input diode current	I _{IK}	-50	mA
Output diode current	lok	±50 (Note 4)	mA
DC output current	lout	±50	mA
Power dissipation	PD	400	mW
DC V _{CC} /ground current per supply pin	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

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Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND, V_{OUT} > V_{CC}$



Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.8 to 3.6	V
rower supply voltage	vcc vcc	1.2 to 3.6 (Note 2)	V
Input voltage (OEAB, OEBA, LEAB, LEBA, CKAB, CKBA)	V _{IN}	-0.3 to 3.6	٧
Bus I/O voltage	Vivo	0 to 3.6 (Note 3)	V
Bus I/O voltage	V _{I/O}	0 to V _{CC} (Note 4)	V
		±12 (Note 5)	
Output current	I _{OH} /I _{OL}	±8 (Note 6)	mA
		±4 (Note 7)	
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: OFF state

Note 4: High or low state

Note 5: $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$

Note 6: $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$

Note 7: $V_{CC} = 1.8 \text{ V}$

Note 8: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V



Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C, 2.7 V < $V_{CC} \le 3.6$ V)

Characteri	stics	Symbol	Test C	Test Condition		Min	Max	Unit
lanut valtaga	H-level	V _{IH}		_	2.7 to 3.6	2.0	_	V
Input voltage	L-level	V _{IL}		_	2.7 to 3.6		0.8	V
				I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	_	
	H-level	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6 \text{ mA}$	2.7	2.2	_	
				$I_{OH} = -8 \text{ mA}$	3.0	2.4	_	
Output voltage				$I_{OH} = -12 \text{ mA}$	3.0	2.2	_	V
				$I_{OL} = 100 \ \mu A$	2.7 to 3.6	_	0.2	
	L-level	VOI		I _{OL} = 6 mA	2.7	_	0.4	
	L-level	VOL		I _{OL} = 8 mA	3.0	_	0.55	
				I _{OL} = 12 mA	3.0	_	0.8	
Input leakage curre	nt	I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	1	±5.0	μΑ
3 state output OEE	state current	loz	$V_{IN} = V_{IH}$ or V_{IL}		2.7 to 3.6		±10.0	^
3-State output OFF	3-state output OFF state current		V _{OUT} = 0 to 3.6 V		2.7 10 3.0		±10.0	μА
Power-off leakage	current	I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	_	10.0	μΑ
Quiescent supply current		laa	V _{IN} = V _{CC} or GND		2.7 to 3.6	_	20.0	
Quiescent supply C	uncil	icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6 \text{ V}$		2.7 to 3.6	_	±20.0	μΑ
Increase in I _{CC} per	input	Δlcc	V _{IH} = V _{CC} - 0.6 V		2.7 to 3.6	_	750	

DC Characteristics (Ta = -40 to 85°C, 2.3 V \leq V_{CC} \leq 2.7 V)

Character	istics	Symbol	Test C	Test Condition		Min	Max	Unit		
Input voltage	H-level	V _{IH}	-	_	2.3 to 2.7	1.6	_	V		
Input voltage	L-level	V _{IL}	-		2.3 to 2.7	_	0.7	V		
				$I_{OH} = -100 \mu A$	2.3 to 2.7	V _{CC} - 0.2				
	H-level	Voh	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -4 \text{ mA}$	2.3	2.0	_			
			V _{IN} = V _{IH} or V _{IL} I _O			$I_{OH} = -6 \text{ mA}$	2.3	1.8	_	
Output voltage				$I_{OH} = -8 \text{ mA}$	2.3	1.7		V		
				$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \ \mu A$	2.3 to 2.7	1	0.2		
	L-level	V _{OL}			$I_{OL} = 6 \text{ mA}$	2.3		0.4		
				$I_{OL} = 8 \text{ mA}$	2.3	_	0.6			
Input leakage curre	ent	I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	_	±5.0	μΑ		
3 state output OEE	state current	loz	V _{IN} = V _{IH} or V _{IL}		2.3 to 2.7		±10.0	μА		
3-state output OFF state current		102	$V_{OUT} = 0$ to 3.6 V		2.5 to 2.7		±10.0	μΛ		
Power-off leakage	current	I _{OFF}	V_{IN} , $V_{OUT} = 0$ to 3.6 V		0	_	10.0	μΑ		
Quiescent supply c	urrent	la.	V _{IN} = V _{CC} or GND		2.3 to 2.7	_	20.0	μА		
Quicacent auppry C	unon	Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.0$	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6 \text{ V}$			±20.0	μΑ		



DC Characteristics (Ta = -40 to 85°C, 1.8 V \leq V $_{CC}$ < 2.3 V)

Characteris	stics	Symbol	Test Co	ondition	V _{CC} (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	_	_	1.8 to 2.3	0.7 × V _{CC}	_	V
input voltage	L-level	V _{IL}	_	_	1.8 to 2.3	_	0.2 × V _{CC}	V
	H-level	V _{OH}	V _{IN} = V _{IH} or V _{II}	I _{OH} = -100 μA	1.8	V _{CC} - 0.2	_	
Output voltage		011		I _{OH} = -4 mA	1.8	1.4	_	V
	L-level	VOI	V _{IN} = V _{IH} or V _{II}	I _{OL} = 100 μA	1.8	_	0.2	
	L-level	VOL	VIN = VIH OI VIL	I _{OL} = 4 mA	1.8	_	0.3	
Input leakage currer	nt	I _{IN}	$V_{IN} = 0$ to 3.6 V		1.8		±5.0	μΑ
3-state output OFF	state current	loz	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 0 \text{ to } 3.6 \text{ V}$		1.8	_	±10.0	μА
Power-off leakage c	urrent	l _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	_	10.0	μΑ
Quiescent supply cu	ırrent	loo	V _{IN} = V _{CC} or GND		1.8	_	20.0	μА
Quicocint supply co	III CIII	Icc	$V_{CC} \le (V_{IN}, V_{OUT}) \le 3.6$	6 V	1.8		±20.0	μΛ



AC Characteristics (Ta = –40 to 85°C, input: $t_r = t_f$ = 2.0 ns, C_L = 30 pF, R_L = 500 Ω) (Note 1)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
			1.8	100	_	
Maximum clock frequency	f _{max}	Figure 1, Figure 3	2.5 ± 0.2	200	_	MHz
			3.3 ± 0.3	250	_	
			1.8	1.5	9.8	
Propagation delay time	t _{pLH}	Figure 1, Figure 2	2.5 ± 0.2	0.8	4.9	ns
(An, Bn-Bn, An)	tpHL		3.3 ± 0.3	0.6	3.8	
D	1.		1.8	1.5	9.8	
Propagation delay time (CKAB , CLKBA -Bn, An)	t _{pLH}	Figure 1, Figure 3	2.5 ± 0.2	0.8	6.7	ns
(CRAD, CLRDA-DII, AII)	tpHL		3.3 ± 0.3	0.6	5.1	
Drawagation delay time			1.8	1.5	9.8	
Propagation delay time (LEAB, LEBA-Bn, An)	t _{pLH}	Figure 1, Figure 4	2.5 ± 0.2	8.0	6.3	ns
(LEAD, LEDA-DII, AII)	tpHL		3.3 ± 0.3	0.6	4.7	1
Output analys time	t _{pZL}	Figure 1, Figure 5, Figure 6	1.8	1.5	9.8	
Output enable time (OEAB, OEBA -Bn, An)			2.5 ± 0.2	8.0	5.9	ns
(OEAB, OEBA-BII, AII)			3.3 ± 0.3	0.6	4.3	
Output disable time	+ . –		1.8	1.5	8.8	
(OEAB, OEBA -Bn, An)	t _{pLZ}	Figure 1, Figure 5, Figure 6	2.5 ± 0.2	0.8	4.9	ns
(OEAB, OEBA-BII, AII)	t _{pHZ}		3.3 ± 0.3	0.6	4.3	
	4		1.8	4.0	_	
Minimum pulse width	tw (H)	Figure 1, Figure 3, Figure 4	2.5 ± 0.2	1.5		ns
	t _{W (L)}		3.3 ± 0.3	1.5	_	
			1.8	2.5		
Minimum setup time	ts	Figure 1, Figure 3, Figure 4	2.5 ± 0.2	1.5		ns
			3.3 ± 0.3	1.5		
			1.8	1.0	_	
Minimum hold time	t _h	Figure 1, Figure 3, Figure 4	2.5 ± 0.2	1.0	_	ns
			3.3 ± 0.3	1.0	_	
	t		1.8	_	0.5	
Output to output skew	t _{osLH}	(Note 2)		_	0.5	ns
	USHL		3.3 ± 0.3	_	0.5	

Note 1: For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design. $(t_{OSLH} = |t_{PLHm} - t_{PLHn}|, \, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)$



Dynamic Switching Characteristics

(Ta = 25°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500$ Ω)

Characteristics	Symbol	Test Condition			Unit
Characteristics	Symbol	rest Condition	V _{CC} (V)	Тур.	Offic
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	1.8	0.15	
Quiet output maximum dynamic V _{OL}	V _{OLP}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	2.5	0.25	V
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	3.3	0.35	
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	1.8	-0.15	
Quiet output minimum dynamic V _{OI}	V _{OLV}	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	2.5	-0.25	V
,		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	3.3	-0.35	
		$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	1.8	1.55	
Quiet output minimum dynamic VOH	0	$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	2.5	2.05	V
,		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (Note	3.3	2.65	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Characteristics Symbol Test Condition			Тур.	Unit	
Characteristics				V _{CC} (V)	ιyp.	Ullit
Input capacitance	C _{IN}	_		1.8, 2.5, 3.3	6	pF
Bus I/O capacitance	C _{I/O}	_		1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C _{PD}	$f_{IN} = 10 \text{ MHz}$ (No	ote)	1.8, 2.5, 3.3	20	pF

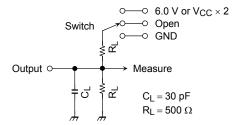
Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18 \text{ (per bit)}$



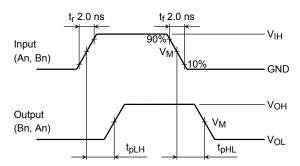
AC Test Circuit



Parameter	Switch			
t _{pLH} , t _{pHL}	Open			
t _P LZ, t _P ZL	6.0 V V _{CC} × 2			
t _{pHZ} , t _{pZH}	GND			

Figure 1

AC Waveform



Symbol	Vcc					
Cymbol	$3.3\pm0.3~\textrm{V}$	$2.5\pm0.2\textrm{V}$	1.8 V			
V _{IH}	2.7 V	V _{CC}	V _{CC}			
V_{M}	1.5 V	V _{CC} /2	V _{CC} /2			
VX	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V			
VY	V _{OH} – 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V			

Figure 2 t_{pLH}, t_{pHL}

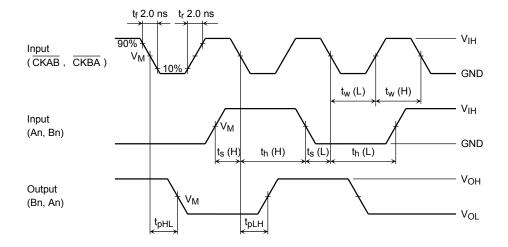


Figure 3 t_{pLH} , t_{pHL} , t_w , t_s , t_h

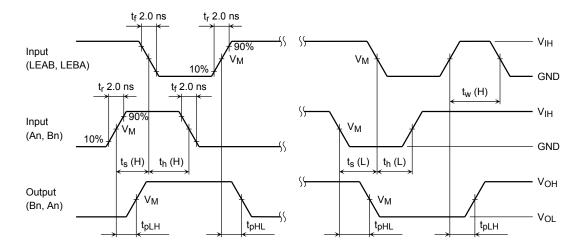


Figure 4 tpLH, tpHL, tw, ts, th

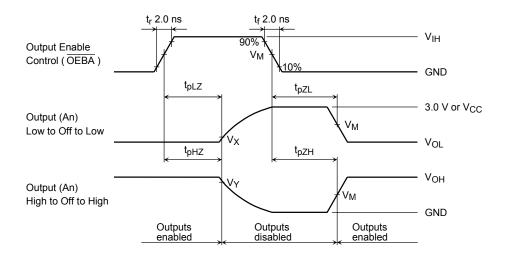


Figure 5 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

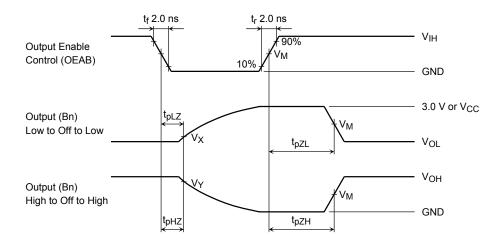
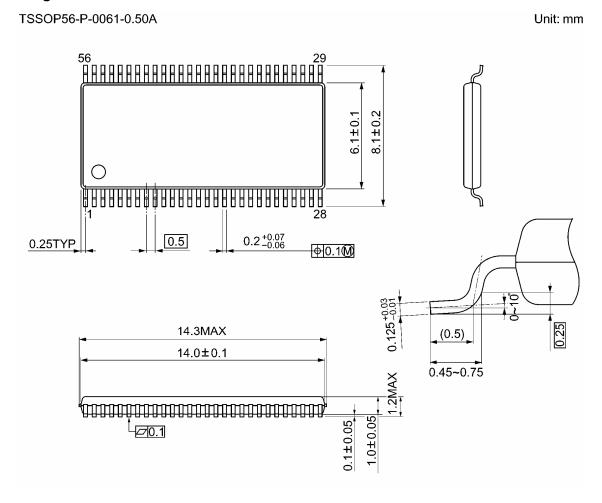


Figure 6 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

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Package Dimensions



Weight: 0.25 g (typ.)

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