TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

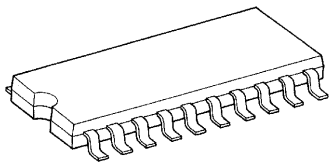
TC74LVX373F, TC74LVX373FW, TC74LVX373FT

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74LVX373 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
This device is suitable for low voltage and battery operated systems.
This 8bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

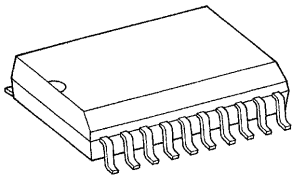
(Note) The JEDEC SOP (FW) is not available in Japan.

TC74LVX373F



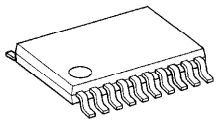
SOP20-P-300-1.27

TC74LVX373FW



SOL20-P-300-1.27

TC74LVX373FT



TSSOP20-P-0044-0.65

Weight
SOP20-P-300-1.27 : 0.22g (Typ.)
SOL20-P-300-1.27 : 0.46g (Typ.)
TSSOP20-P-0044-0.65 : 0.08g (Typ.)

FEATURES

- High speed : $t_{pd} = 5.8ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) ($Ta = 25°C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
  $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \simeq t_{pHL}$
- Low noise : $V_{OLP} = 0.8V$ (Max.)
- Pin and function compatible with 74HC373

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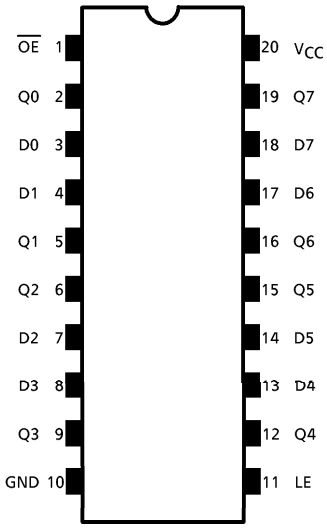
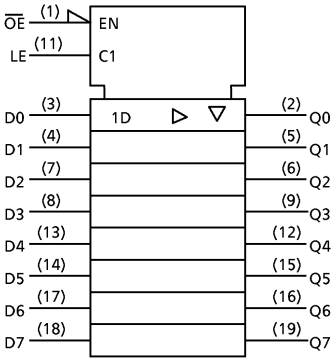
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

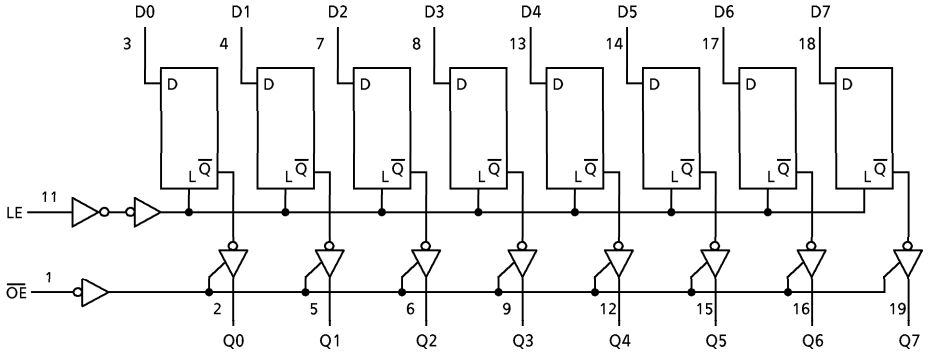


TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
Qn : Q outputs are latched at the time when the LE input is taken to a low logic level.

SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~100	ns / V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
3-state Output Off-state Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current		I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

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TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION		Ta = 25°C	Ta = −40~85°C	UNIT
			V_{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (LE)	t_W (H)		2.7	6.5	7.5	ns
			3.3 ± 0.3	5.0	5.0	
Minimum Set-up Time	t_s		2.7	6.0	6.0	ns
			3.3 ± 0.3	4.0	4.0	
Minimum Hold Time	t_h		2.7	1.0	1.0	ns
			3.3 ± 0.3	1.0	1.0	

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	V_{CC} (V)	C_L (pF)	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40~85°C MIN.	MAX.	UNIT
Propagation Delay Time (LE-Q)	t_{pLH}		2.7	15	—	7.5	14.5	1.0	17.5	ns
				50	—	10.0	18.0	1.0	21.0	
	t_{pHL}		3.3 ± 0.3	15	—	5.8	9.3	1.0	11.0	
				50	—	8.3	12.8	1.0	14.5	
Propagation Delay Time (D-Q)	t_{pLH}		2.7	15	—	7.7	15.0	1.0	18.5	ns
				50	—	10.2	18.5	1.0	22.0	
	t_{pHL}		3.3 ± 0.3	15	—	6.0	9.7	1.0	11.5	
				50	—	8.5	13.2	1.0	15.0	
Output Enable Time	t_{pZL}	$R_L = 1k\Omega$	2.7	15	—	7.7	15.0	1.0	18.5	ns
				50	—	10.2	18.5	1.0	22.0	
	t_{pZH}		3.3 ± 0.3	15	—	6.0	9.7	1.0	11.5	
				50	—	8.5	13.2	1.0	15.0	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	9.8	18.0	1.0	21.0	ns
			3.3 ± 0.3	50	—	8.2	12.8	1.0	14.5	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	27	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :

$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per Latch)

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

$C_{PD}(total) = 14 + 13 \cdot n$

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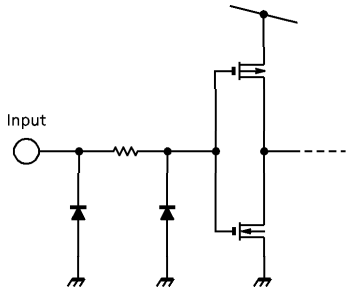
Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



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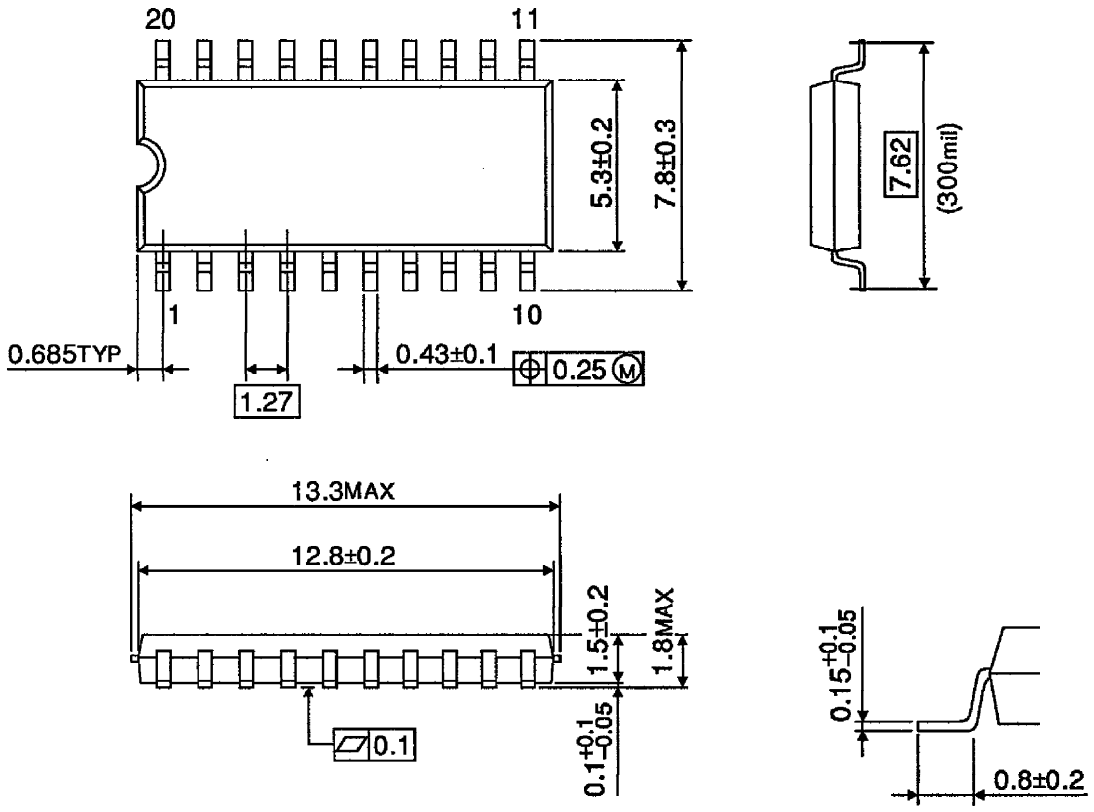
OUTLINE DRAWING

SOP20-P-300-1.27 Unit : mm



Weight : 0.22g (Typ.)

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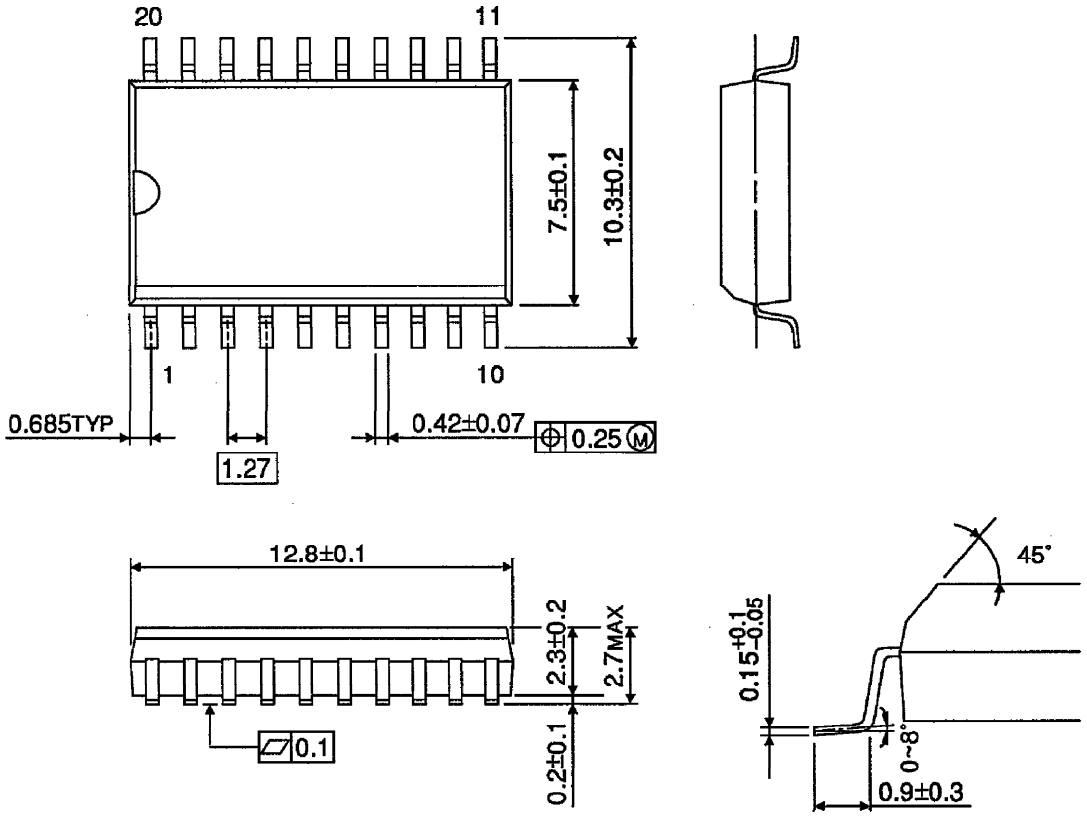
OUTLINE DRAWING

SOL20-P-300-1.27

Unit : mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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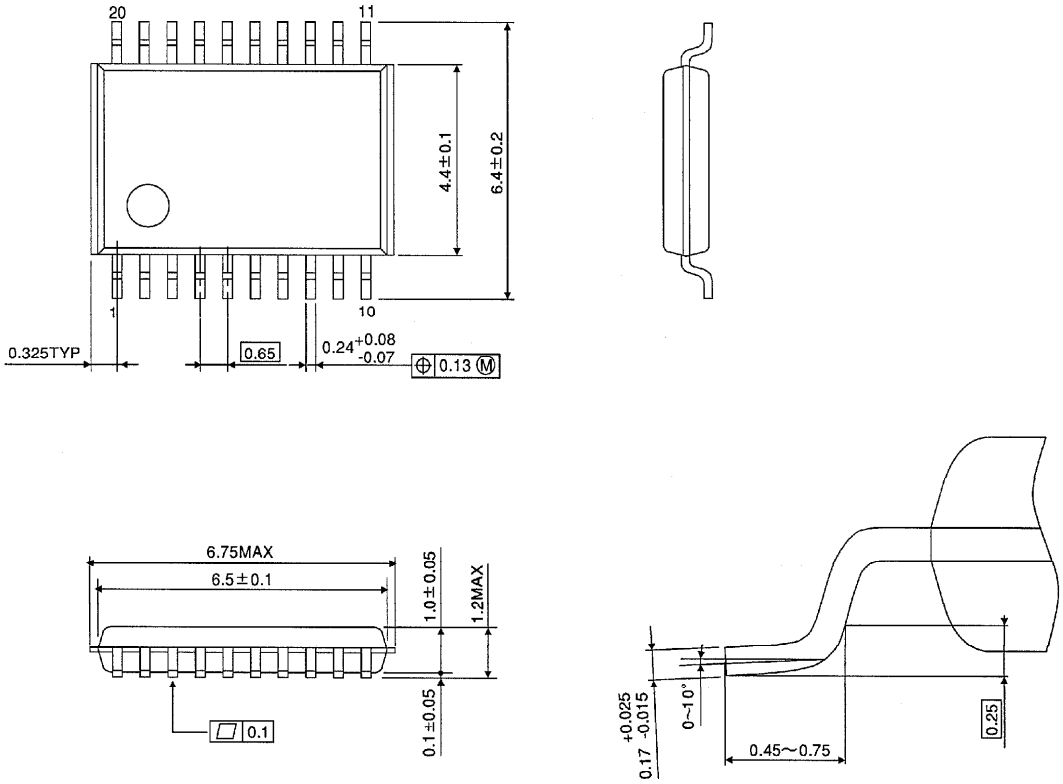
OUTLINE DRAWING

TSSOP20-P-0044-0.65

Unit : mm



Weight : 0.08g (Typ.)

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