TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LVX157F, TC74LVX157FN, TC74LVX157FT

QUAD 2-CHANNEL MULTIPLEXER

The TC74LVX157 is a high speed CMOS QUAD 2-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

This device consist of four 2-input digital multiplexers with common select and strobe inputs.

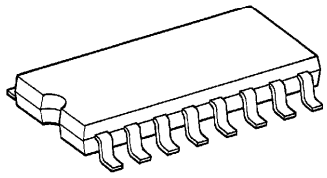
When the $\overline{\text{STROBE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

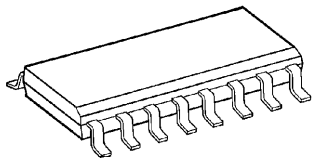
(Note) The JEDEC SOP (FN) is not available in Japan.

TC74LVX157F



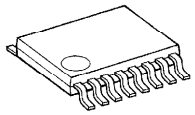
SOP16-P-300-1.27

TC74LVX157FN



SOL16-P-150-1.27

TC74LVX157FT



TSSOP16-P-0044-0.65

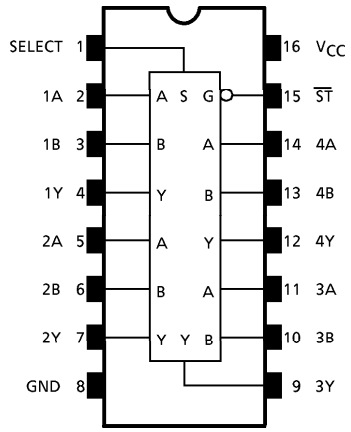
Weight
SOP16-P-300-1.27 : 0.18g (Typ.)
SOL16-P-150-1.27 : 0.12g (Typ.)
TSSOP16-P-0044-0.65 : 0.06g (Typ.)

FEATURES

- High speed : $t_{pd} = 5.1$ns (Typ.) ($V_{CC} = 3.3$V)
- Low power dissipation : $I_{CC} = 4\mu$A (Max.) (Ta = 25°C)
- Input voltage level : $V_{IL} = 0.8$V (Max.) ($V_{CC} = 3$V)
  $V_{IH} = 2.0$V (Min.) ($V_{CC} = 3$V)
- Power down protection is provided on all inputs.
- Balanced propagation delays
  : $t_{pLH} \simeq t_{pHL}$
- Low noise : $V_{OLP} = 0.5$V (Max.)
- Pin and function compatible with 74HC157

961001EBA2

PIN ASSIGNMENT



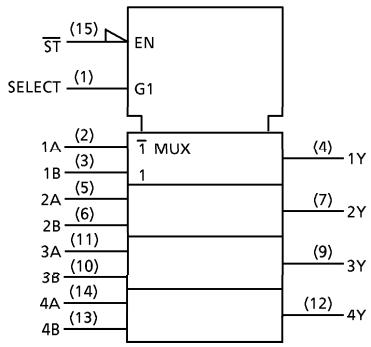
(TOP VIEW)

TRUTHTH TABLE

INPUTS				OUTPUTS
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

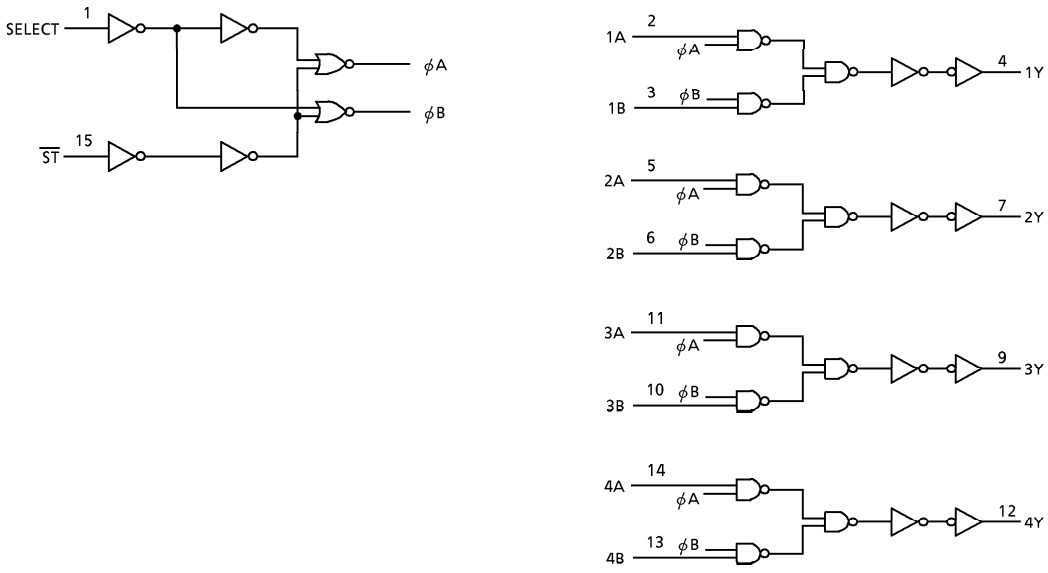
X : Don't Care

IEC LOGIC SYMBOL



961001EBA2'

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current		I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	V_{CC} (V)	C_L (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (A, B-Y)	t_{pLH}		2.7	15	—	6.6	12.5	1.0	15.5	ns
				50	—	9.1	16.0	1.0	19.0	
	t_{pHL}		3.3 ± 0.3	15	—	5.1	7.9	1.0	9.5	
				50	—	7.6	11.4	1.0	13.0	
Propagation Delay Time (SELECT-Y)	t_{pLH}		2.7	15	—	8.9	16.9	1.0	20.5	ns
				50	—	11.4	20.4	1.0	24.0	
	t_{pHL}		3.3 ± 0.3	15	—	7.0	11.0	1.0	13.0	
				50	—	9.5	14.5	1.0	16.5	
Propagation Delay Time ($\overline{ST}$-Y)	t_{pLH}		2.7	15	—	9.1	17.6	1.0	20.5	ns
				50	—	11.6	21.1	1.0	24.0	
	t_{pHL}		3.3 ± 0.3	15	—	7.2	11.5	1.0	13.5	
				50	—	9.7	15.0	1.0	17.0	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	20	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :

$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$ (per bit)

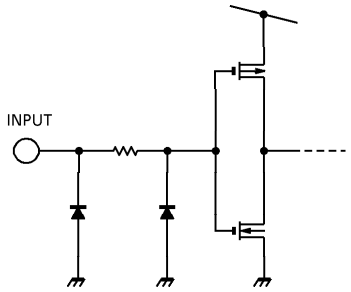
And the total C_{PD} when n pcs. of gate operate can be gained by the following equation :

C_{PD} (total) $= 13 + 7 \cdot n$

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

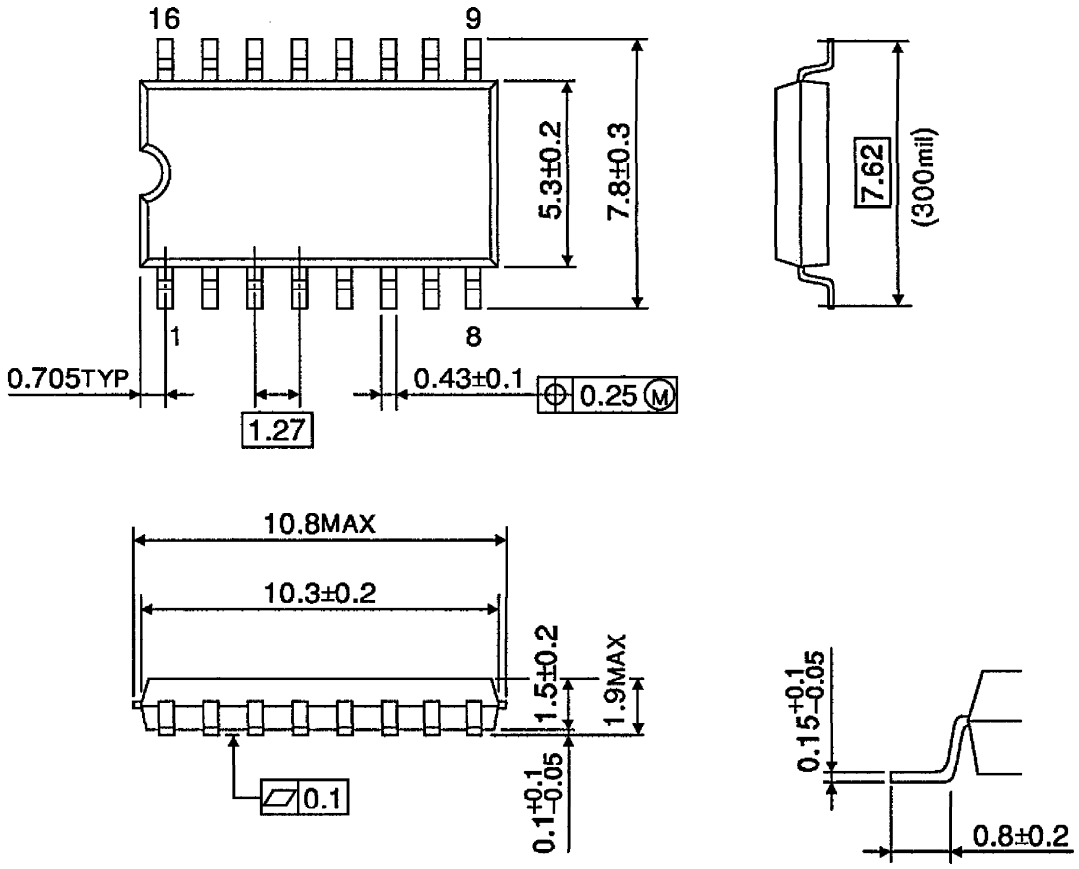
INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING

SOP16-P-300-1.27

Unit : mm



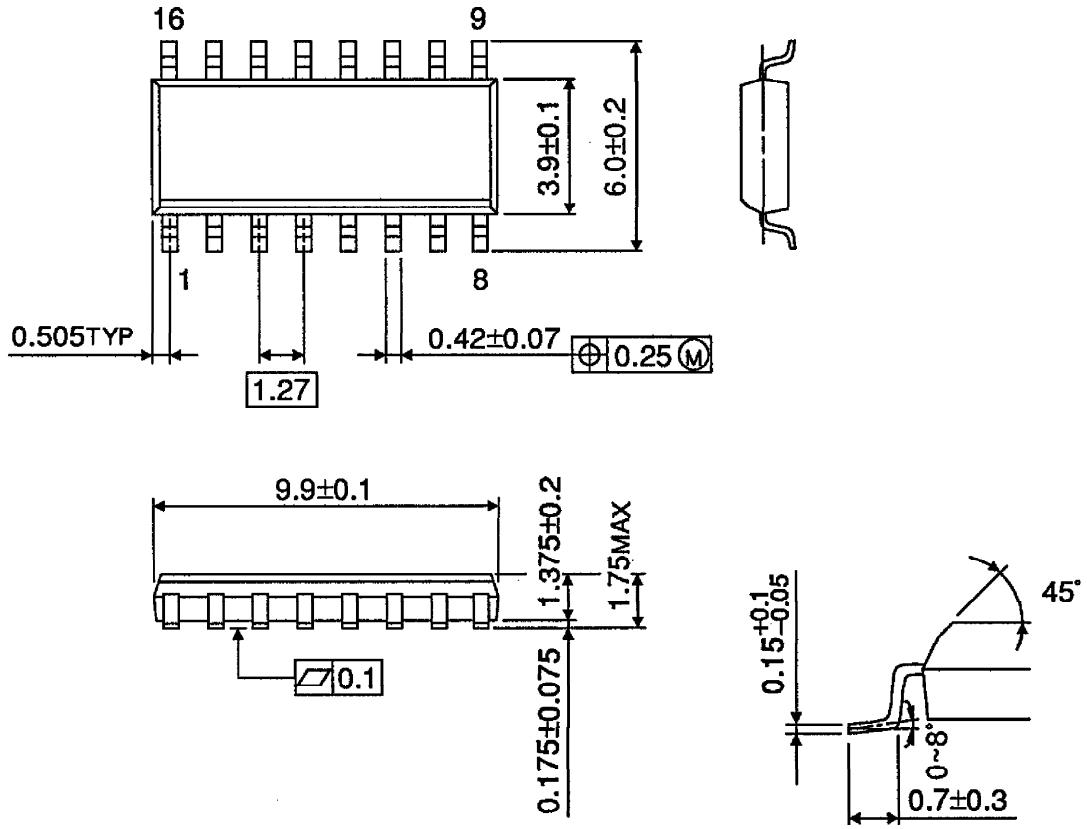
Weight : 0.18g (Typ.)

OUTLINE DRAWING

SOL16-P-150-1.27

Unit : mm

(Note) This package is not available in Japan.

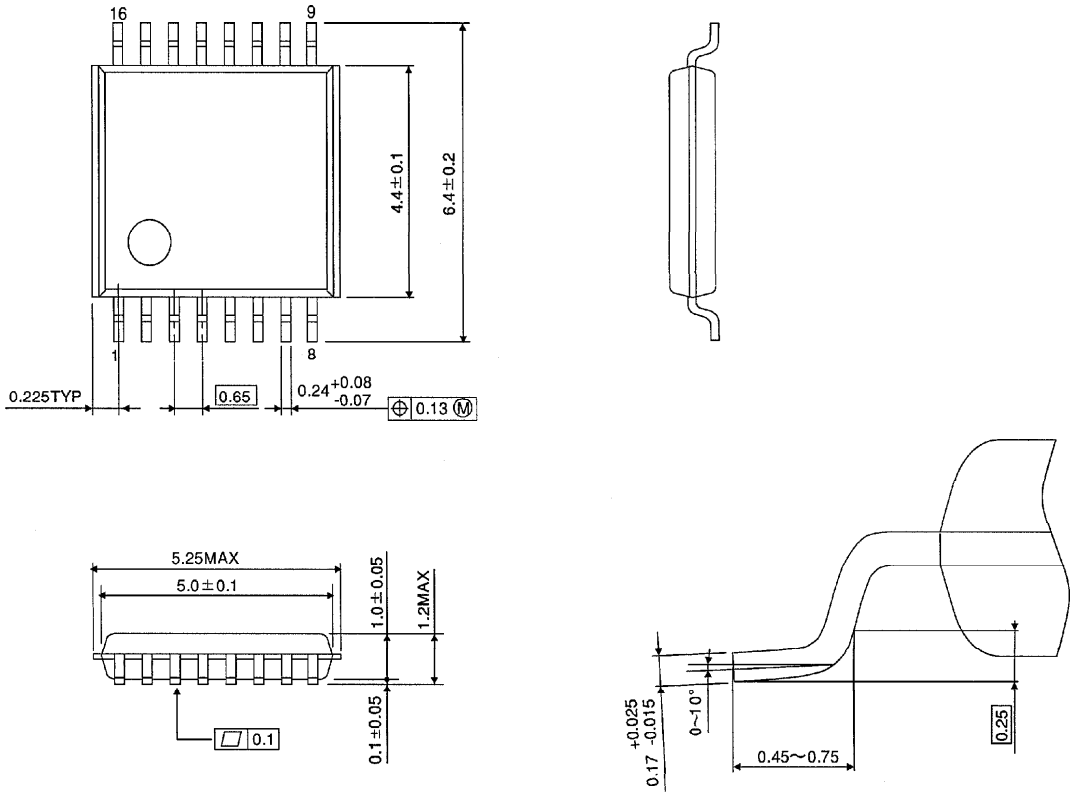


Weight : 0.12g (Typ.)

OUTLINE DRAWING

TSSOP16-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)