HD6345/HD6445

CRTC-II(CRT Controller)

The HD6345/HD6445 CRTC-II provides an interface between MPU and a raster scan CRT display. The HD6345 is upward-compatible with the NMOS CRTC HD6845S in pin and software, and has a 68 system bus interface. The HD6445 has a 80 system bus interface. A power dissipation is lowered by adopting the CMOS process.
The CRTC-II offers a variety of functions under MPU control, such as programmable timing signal outputs for CRT monitor and display screen control operation. It can be widely applied to the various types of CRT display systems.

FEATURES

FLEXIBLE SCREEN FORMAT

- Programmable numbers of characters per screen and rasters per character row
- Programmable horizontal/vertical sync signals and display timing signals
- Up to 16k words refresh memory (14-bit) addressable
- Programmable raster scanning modes: Non-Interlace, Interlace sync, or Interlace sync and video modes
- Up to 256 character rows per field
- High-speed display operation at 4.5 MHz character clock
- Double-size vertical display by raster interpolation

VERSATILE DISPLAY FUNCTIONS

- Screen split (max. 4 screens configurable, horizontally)
- Paging and scrolling for each screen
- Smooth scrolling
- Two cursors with programmable width
- Programmable refresh memoly width

FACILITATED SYSTEM CONFIGURATION

- 68 system bus interface (HD6345)
- 80 system bus interface (HD6445)
- Three-state control of memory address and raster address
- External synchronization in Master-slave or TV syne modes
- Interrupt request by vertical blanking or light pen strobe detection
- Programmable timing signal for dual-port RAM in MPRAM mode

PIN AND SOFTWARE UPWARD-COMPATIBLE WITH HD6845S

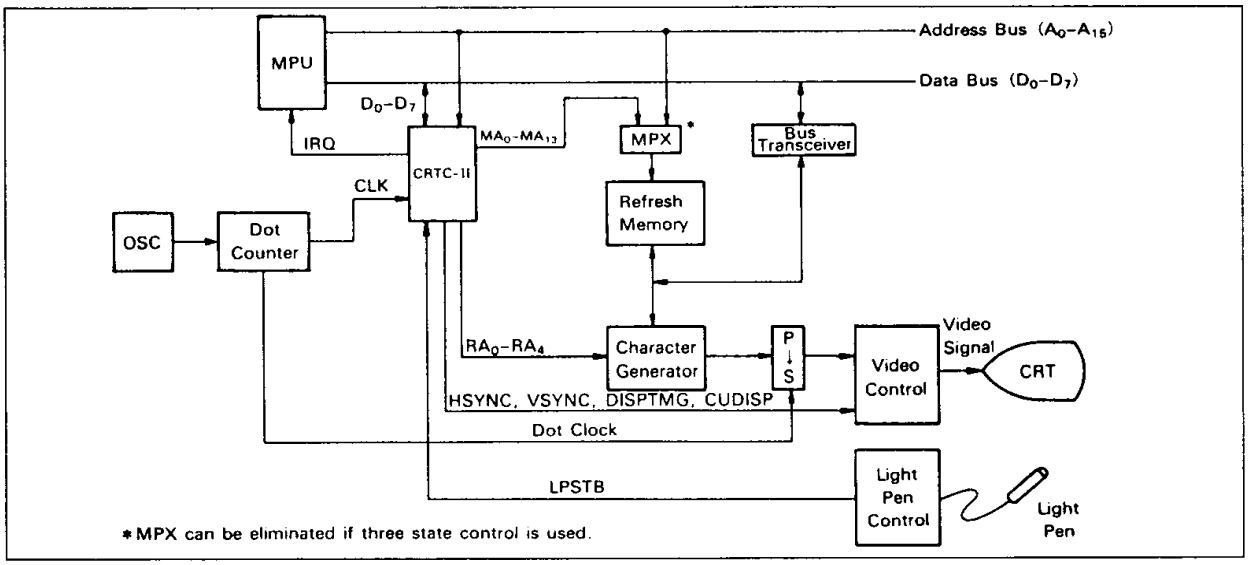
SINGLE +5V POWER SUPPLY

CMOS PROCESS

OPERATING TEMPERATURE SPECIFICATIONS

- Normal -20°C ~ +75°C
- J Version -40°C ~ +85°C

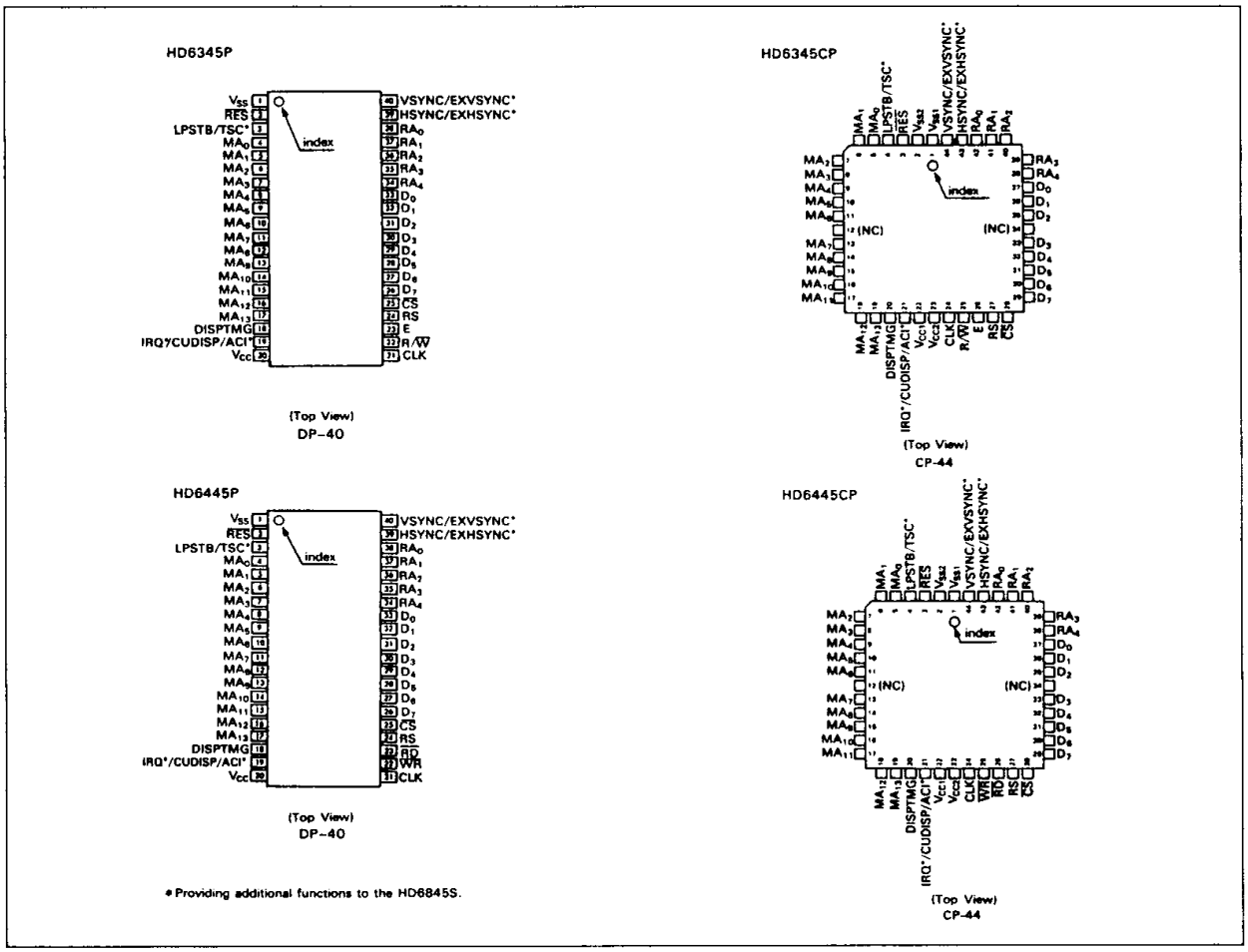
SYSTEM BLOCK DIAGRAM



TYPE OF PRODUCTS

Specification	Bus Interface	Type No.	Bus Timing	Package	CRT Display Timing
Normal	6800 system Bus interface	HD6345P	1.0 MHz	DP-40 (40 pin plastic Dip)	4.5 MHz (max)
		HD63A45P	1.5 MHz		
		HD63B45P	2.0 MHz		
		HD6345CP	1.0 MHz	CP-44 (44 pin PLCC)	
		HD63A45CP	1.5 MHz		
		HD63B45CP	2.0 MHz		
	80 system Bus interface	HD6445P4	4.0 MHz	DP-40	
		HD6445CP4		CP-44	
J version (wide temperature range)	6800 system Bus interface	HD6345CPJ	1.0 MHz	CP-44	4.5 MHz (max)
		HD63A45CPJ	1.5 MHz		
		HD63B45CPJ	2.0 MHz		
	80 system Bus interface	HD6445CP4J	4.0 MHz		

PIN ARRANGEMENT



PIN FUNCTION

Pin No.					
DP-40	CP-44	Symbol	Pin Name	Input/ Output	Functions
1	1, 2	V_{SS} (V_{SS1}, V_{SS2})**	V_{SS}	—	Ground (GND) pin
2	3	$\overline{RES}$	Reset	Input	Performs external reset on CRTC-II $\overline{RES}$ assertion causes CRTC-II: (1) Clear all the internal counters (2) Set all the output signals at "L" (D_0–D_7 are excluded.) (3) Clear registers R30 (Control 1), R31 (Control 2/Status), and R32 (Control 3) (Other registers are not affected at all) $\overline{RES}$ is valid only while LPSTB is "L"
3	4	LPSTB	Light Pen Strobe	Input	Informs light pen strobe pulse detection
		TSC	Three State Control	Input	Performs three-state control on memory and raster addresses
4–17	5–11, 13–19	MA_0–MA_{13}	Memory Address 0–13	Output	Supplies memory address for periodical memory refresh
18	20	DISPTMG	Display Timing	Output	Indicates a screen display period
19	21	CUDISP	Cursor Display	Output	Display cursor on a screen Enabled during DISPTMG is "H"
		ACI	Access Inhibit	Output	Supplies MPRAM access inhibit timing (programmable)
		IRQ	Interrupt Request	Output	Indicates interrupt request to MPU Enabled during DISPTMG is "L"
20	22, 23	V_{CC}(V_{CC1}, V_{CC2})**	V_{CC}	—	Power supply (+5V) pin
21	24	CLK	V_{CC} Character Clock	Input	Receives character clock timing
22	25	R/$\overline{W}$	Read/Write	Input	Controls data transfer direction between MPU and CRTC-II
		$\overline{WR}$*	Write	Input	Inputs write signal from MPU
23	26	E	Enable	Input	Enables register read/write strobe signals from MPU
		$\overline{RD}$*	Read	Input	Inputs read signal from MPU
24	27	RS	Register Select	Input	Selects either of address register or other registers Address reg. selected when at "L", and others at "H" Normally, requested to connect to "A_0" of MPU address bus
25	28	$\overline{CS}$	Chip Select	Input	Performs addressing on CRTC-II MPU Read/ write upon CRTC-II registers enabled when $\overline{CS}$ is "L"
33–26	37–35, 33–29	D_0–D_7	Data Bus 0–7	Input/ Output	Bidirectional bus for data transfer between MPU and CRTC-II
38–34	42–38	RA_0–RA_4	Raster Address 0–4	Output	Supplies raster address for selecting raster on character generator
39	43	HSYNC	Horizontal Sync	Output	Supplies horizontal sync signal
		EXHSYNC	External Horizontal Sync	Input	Receives external horizontal sync signal
40	44	VSYNC	Vertical Sync	Output	Supplies vertical sync signal
		EXVSYNC	External Vertical Sync	Input	Receives external vertical sync signal

*Notes: *Marked pins are of the HD6445.
**Marked pins are of the CP-44

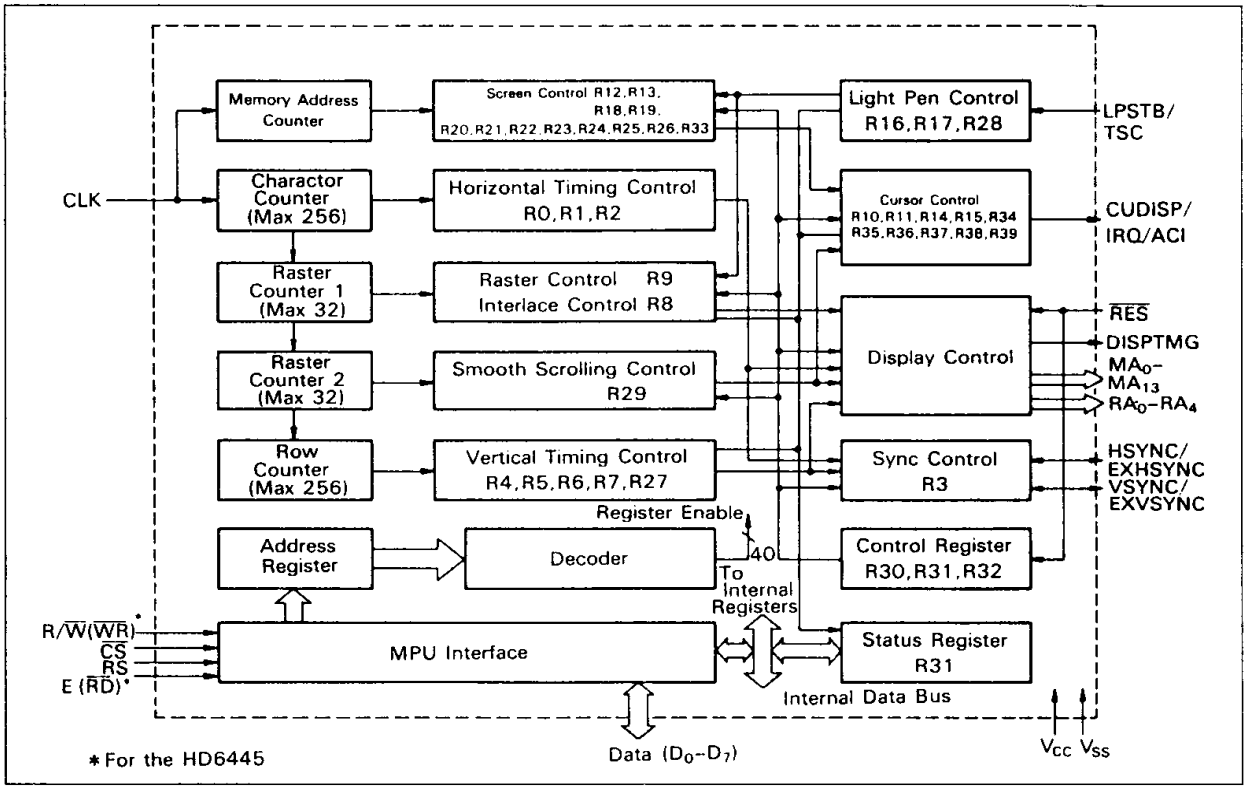
FUNCTION TABLE

Item	Descriptions	Remarks
Programmable Screen Format	Horizontal scan cycle	Programmable by char. clock time
	Vertical scan cycle (by row)	Programmable by char. row time
	Vertical scan cycle (Adjust)	Programmable by raster time
	Number of displayed chars./row	
	Number of char. rows/screen	
	Number of rasters/char. row	
	Horizontal display position	Enabled by programming sync signal output timings
	Vertical display position	
	Vertical sync position (Adjust)	Programmable by raster time
	HSYNC pulse width	
	VSYNC pulse width	
	DISPTMG skew	1 or 2 character skew
Screen Split	4 split-screens start positions programmable	Discretely programmable (Unit: row) 2/3/4 screens format selectable
Cursor Control	Cursor display position	Two 14-bit cursor registers 1 or 2 cursors displayed
	Cursor height	Display start/end rasters programmable within a row
	Cursor width	Programmable by char. clock time
	Cursor blink	1/16 or 1/32 field rate selectable
	Simultaneous output of 2 cursors (Only 1 availble in MPRAM mode)	Discretely programmable
	Cursor display mode	OR/EOR mode selectable
	CUDISP skew	1 or 2 character skew
Raster Scan Mode	Non-Interlace mode Interlace sync mode Interlace sync and video mode	Either one of three modes selectable
Memory Format	Memory width set	Memory width programmable wider than display width (Unit: char.)
Smooth Scrolling	Display start raster address set	Programmable by char. clock time
	Target screen set	Any screen selectable
Raster Interpolation	Double-size vertical display Vertical scan cycle doubled	Same raster address supplied twice
External Synchronization	Synchronization with external sync signals	Superimposed display enhabled on other CRT or TV screens
Interrput Request	Interrupt request signal caused by vertical ratrace period or light pen detection (Disabled in MPRAM mode)	Interrupt reqest mode programmable
Light Pen	14-bit Light pen register Light pen raster register	Light pen raster address detected
Refresh Memory Addressing	14-bit refresh memory address output Four 14-bit screen start address regs. (Display start address programmable for each screen)	Up to 16k words refresh memory accessible Paging and scrolling enabled each screen
Three-State Control	Three-state control on MA and RA	Controlled by TSC pin input
Programmable Timing Output	Programmable timing signal supplied from access inhibit pin	In MPRAM mode

CRTC-II NEWLY ADOPTED FEATURES

1. Screen Partition (horizontally split into 4 screens)
2. Smooth Scrolling
3. External Synchronization
4. Interrupt request
5. Raster Interpolation
6. Sync Position Adjustment
7. Light Pen Raster Address
8. Second Cursor
9. Display Momory Width Setting
10. 256 Rows Max
11. Timing Signal for MPRAM
12. Three-state Control of MA/RA Output

INTERNAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PROGRAMMABLE SCREEN FORMAT

Figure 1 illustrates the screen format example, in Non-Interlace mode, when programming CRTC-II registers as listed in Tabel 1. Figure 2 shows the relation between memory address (MA_0-MA_{13}), raster address (RA_0-RA_4) and the location on the CRT screen.

The timing charts of CRT interface signals are shown in Figure 3, and those details are partially shown in Figure 4 and 5.

Tabel 1 Programmed Values in Each Register

Register No.	Register Name	Programmed Values
R0	HORIZONTAL TOTAL CHARACTERS	Nht
R1	HORIZONTAL DISPLAYED CHARACTERS	Nhd
R2	HORIZONTAL SYNC POSITION	Nhsp
R3	SYNC WIDTH	Nvsw, Nhsw
R4	VERTICAL TOTAL ROWS	Nvt
R5	VERTICAL TOTAL ADJUST	Nadj
R6	VERTICAL DISPLAYED ROWS	Nvd
R7	VERTICAL SYNC POSITION	Nvsp
R9	MAX. RASTER ADDRESS	Nr
R12	SCREEN 1 START ADDRESS (H)	0
R13	SCREEN 1 START ADDRESS (L)	0
R30	CONTROL 1	0
R31	CONTROL 2/STATUS	0
R32	CONTROL 3	0

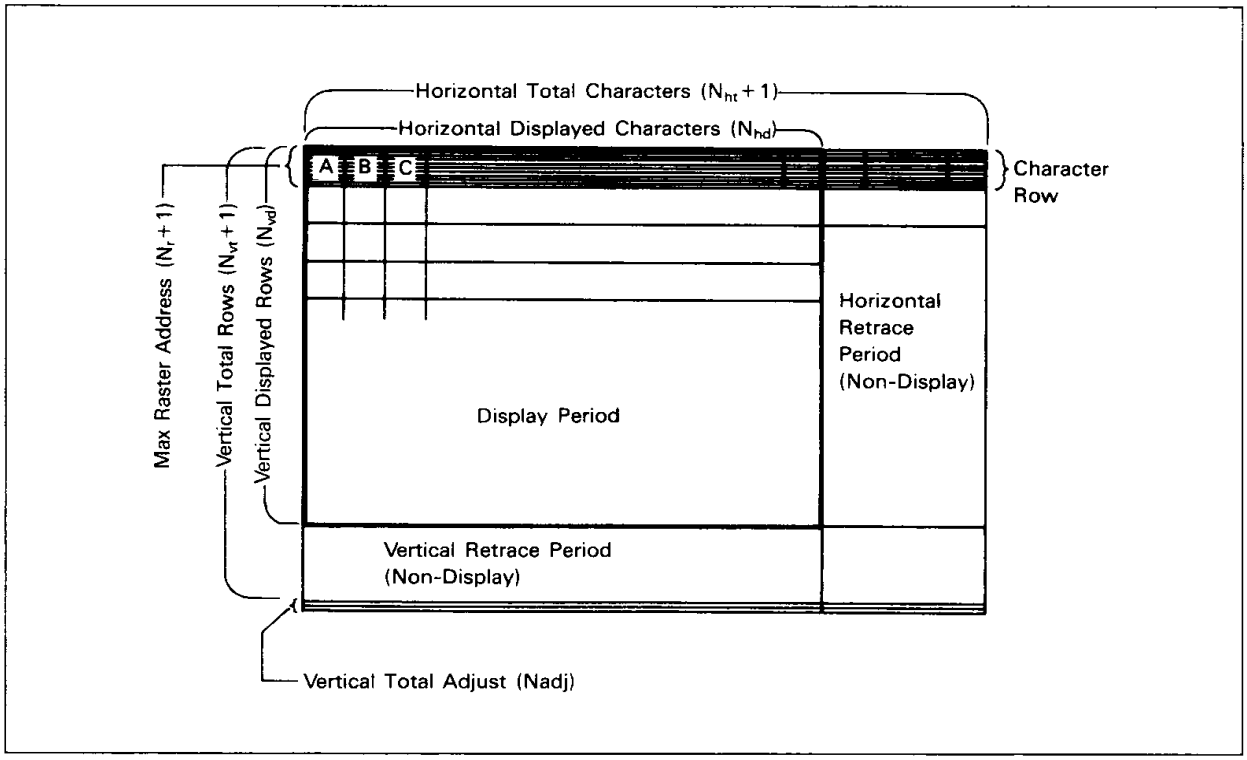
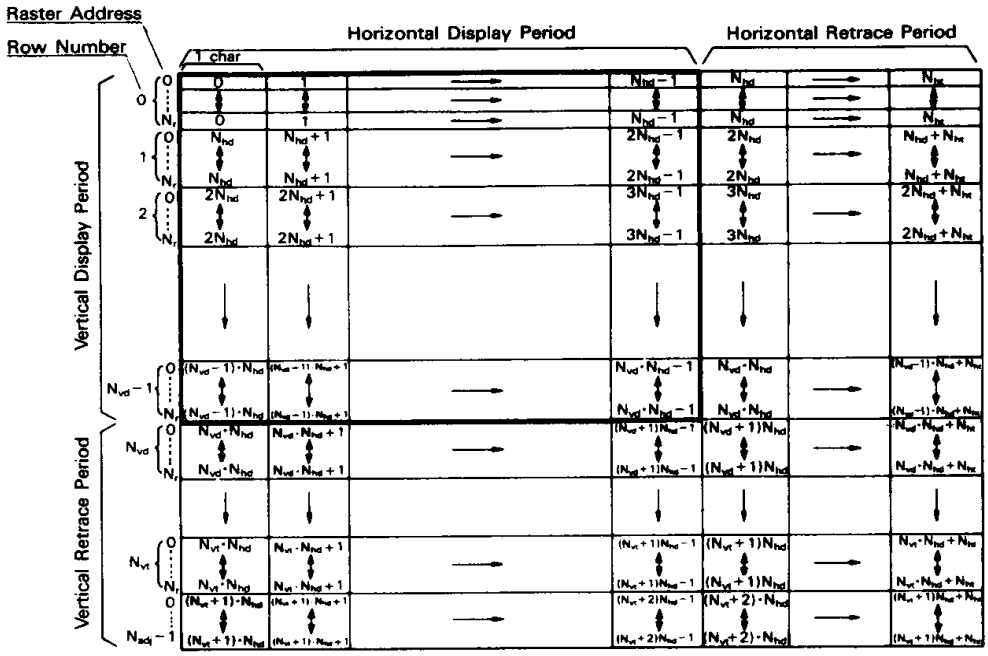


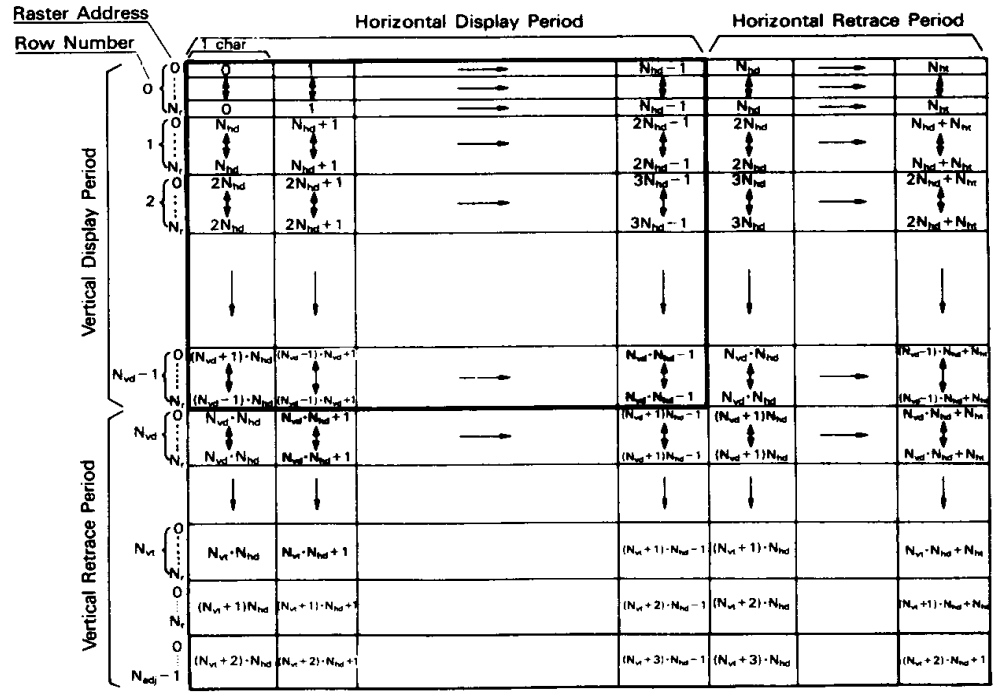
Figure 1 CRT Screen Format

① $N_{adj} - 1 \leqq N_r$



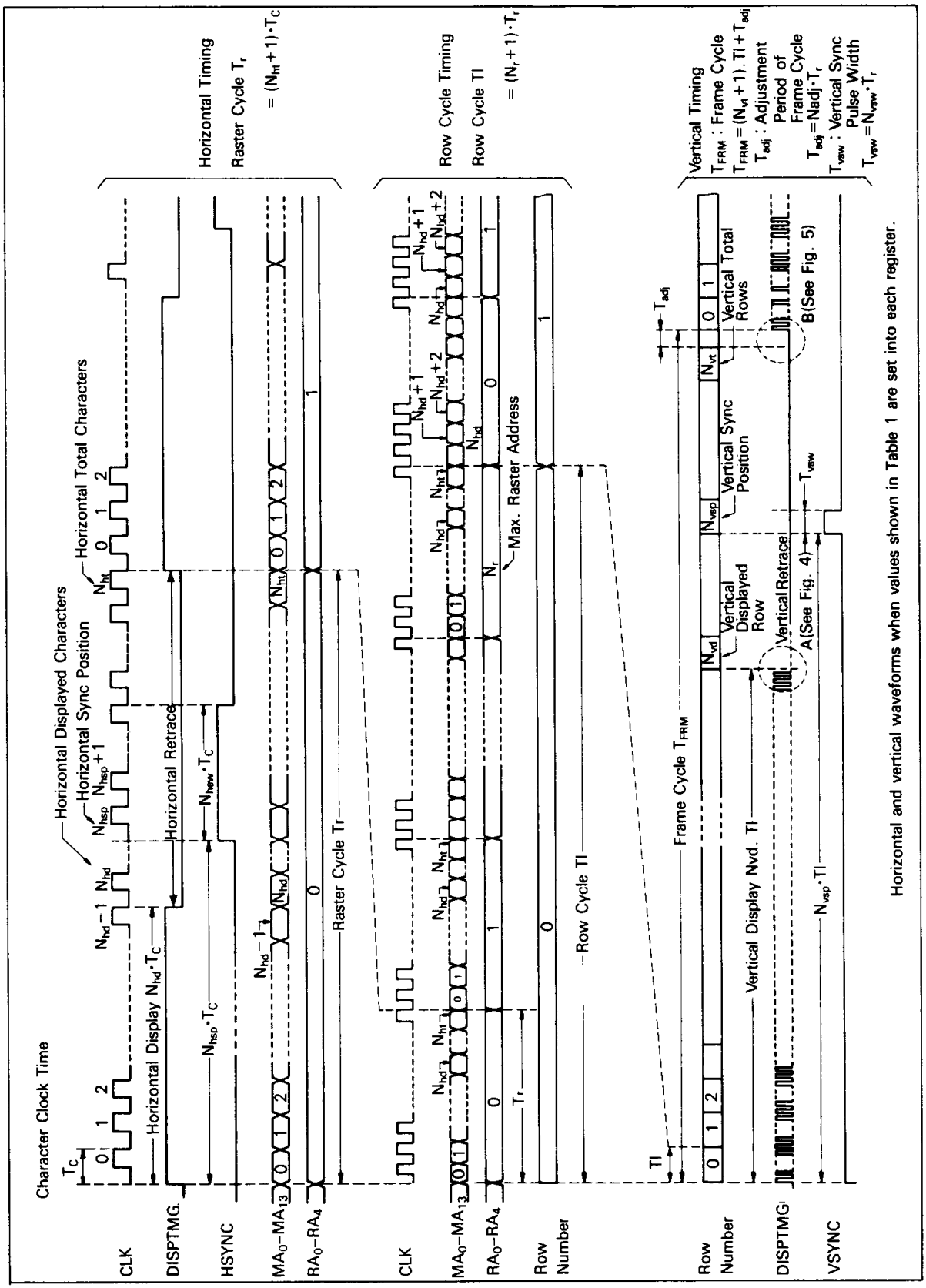
Valid memory addresses [0 thru (N_{vd} -1) or 0 (N_{hd} -1)] are shown within the thick-line square. Memory addresses are provided even during horizontal and vertical retrace period. This is an example in the case where the programmed value of start address register is 0.

② $N_{adj} - 1 > N_r$



Valid memory addresses [0 thru (N_{vd} -1) or 0 (N_{hd} -1)] are shown within the thick-line square. Memory addresses are provided even during horizontal and vertical retrace period. This is an example in the case where the programmed value of start address register is 0.

Figure 2 Memory Address and Raster Address



Horizontal and vertical waveforms when values shown in Table 1 are set into each register.

Figure 3 CRTC-II Timing Chart (Non-Interlace mode)

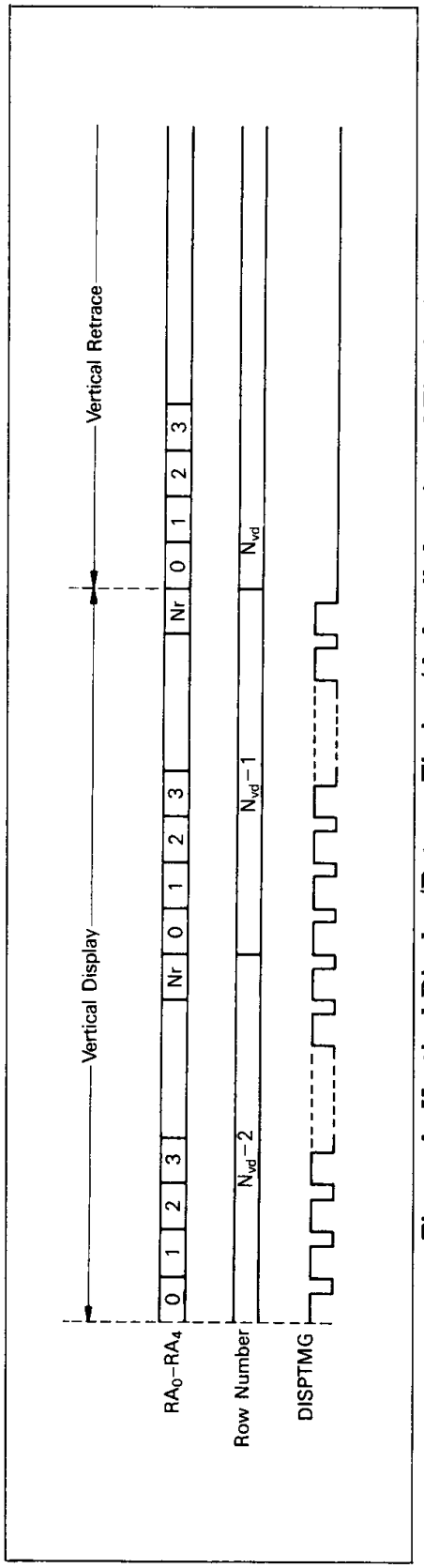


Figure 4 Vertical Display/Retrace Timing (A detail drawing of Fig. 3 A)

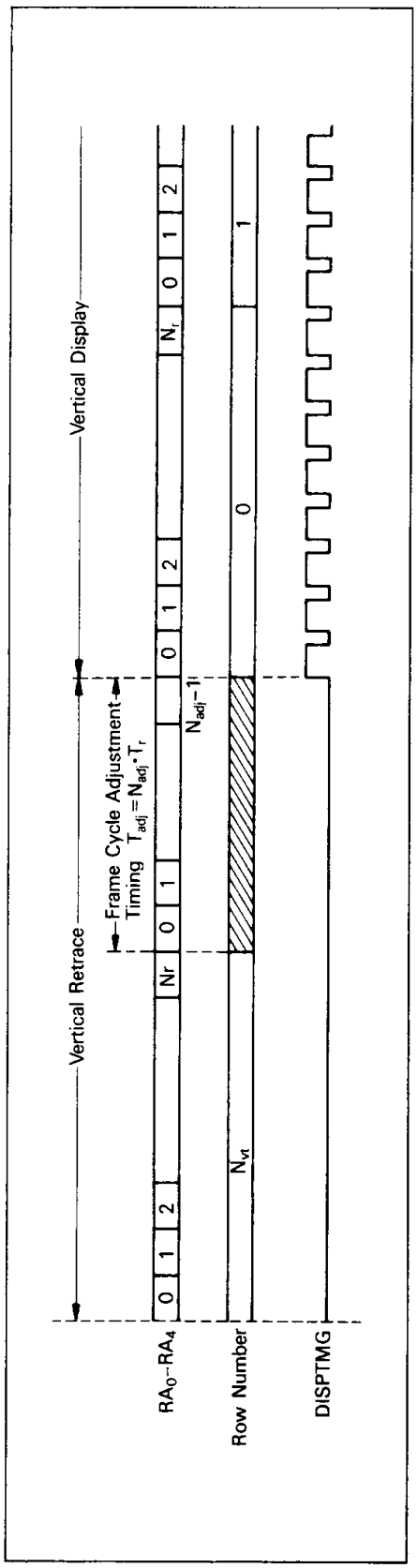


Figure 5 Frame Cycle Adjustment Timing (A detail drawing of Fig. 3 B)

SCREEN SPLIT

A display screen can be divided into up to four parts in the horizontal direction. Divided four parts are defined as split-screen 1, split-screen 2, split-screen 3, and split-screen 4.

The starting positions of each split-screen are determined in the number of character row. Split-screen 1 is the base screen, and always starts at row 0, while the other three split-screens start at any row except row 0. Paging or scrolling (by character) is performed in each split-screen independently.

Screen split is controlled by the SP0 and the Sp1 bits of the control 1 register (R30) and the screen start position registers (R18, R21, R24). If the same value is programmed in more than one screen start position register or a start position which is out of display row is programmed in those registers, the corresponding split-screens will not be displayed.

The following is examples of screen split:

When the same value are programmed into more than one screen start position registers, split-screens corresponding to these registers are not displayed.

Table 2 Screen Split

Control 1 Register		Number of effective screen			
SP1	SP0	1	2	3	4
0	0	○	–	–	–
0	1	○	○	–	–
1	0	○	○	○	–
1	1	○	○	○	○

○ : effective screen
– : invalid screen

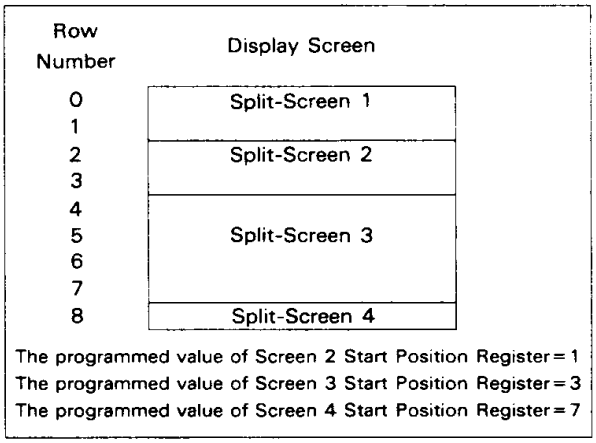


Figure 6-A Screen Split (Example 1)

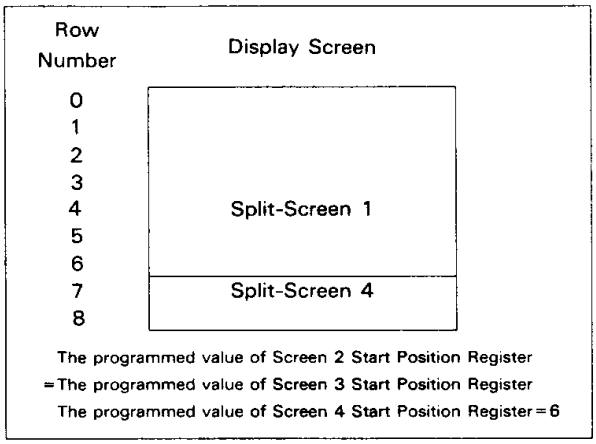


Figure 6-B Screen Split (Example 2)

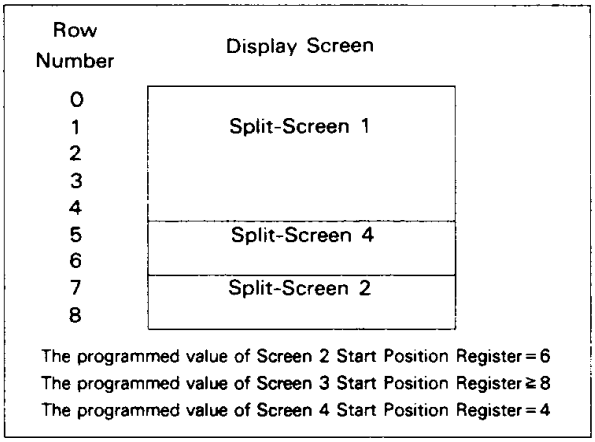


Figure 6-C Screen Split (Example 3)

CURSOR CONTROL

The CRTC-II can display two separate cursors (cursor 1, cursor 2) simultaneously on the screen. These two cursors are controlled independently. The cursor 1 is always valid, while the cursor 2 becomes valid by setting the C_2 bit of the control 3 register (R32).
In the MPRAM mode, the cursor 2 cannot be displayed. The CRTC-II controls cursors as follows:

1) Starting Position
   Starting position is controlled by the cursor 1 address registers (R14, R15), and the cursor 2 address registers (R36, R37).
2) Cursor Heights
   The heights of the cursor 1 and the cursor 2 can be specified independently in units of rasters by the cursor start registers (R10, R34), and the cursor end registers (R11, R35).
3) Cursor Widths
   The widths of the cursor 1 and the cursor 2 can be specified independently in units of characters by the cursor width registers (R38, R39). The R38 register is enabled when 1 is set into the CW1 bit of the control 3 register (R32). The R39 register's enable bit is the CW2.
   If the cursor width extends over the following row, the cursor in the following row will not be displayed.
4) Cursor Blink
   Cursor display, non-display, and blink rate can be controlled by the bits B_1 and P_1 of the cursor 1 start register (R10), and bits the B_2 and P_2 of the cursor 2 start register (R34).
5) Cursor Display Mode
   When the cursor 1 and the cursor 2 are overlapped on the screen, cursor display mode in the overlapped area can be selected by the CM bit of the control 3 register (R32), as shown in Figure 8.

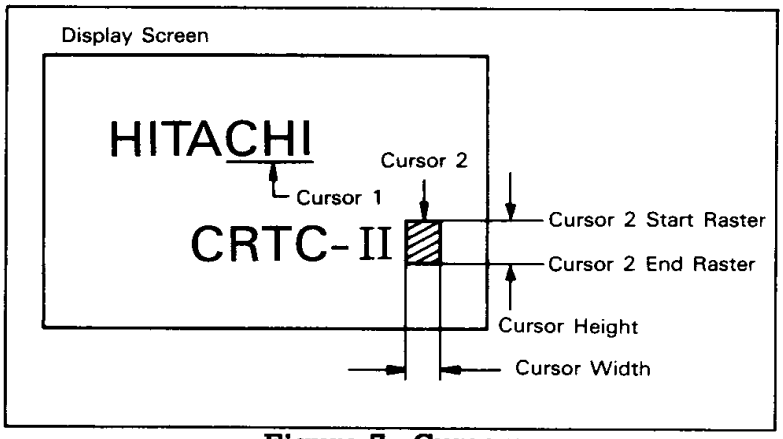


Figure 7 Cursors

Table 3 Cursor Blink Mode

B_1	P_1	Cursor Blink Mode
0	0	No blink
0	1	No cursor
1	0	Blink, 1/16 field rate
1	1	Blink, 1/32 field rate

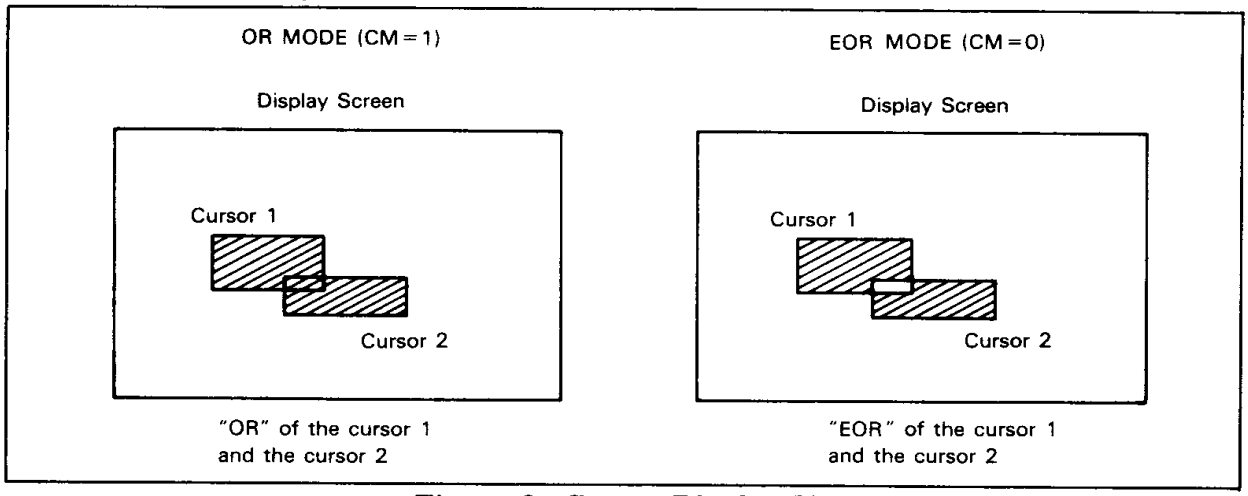


Figure 8 Cursor Display Mode

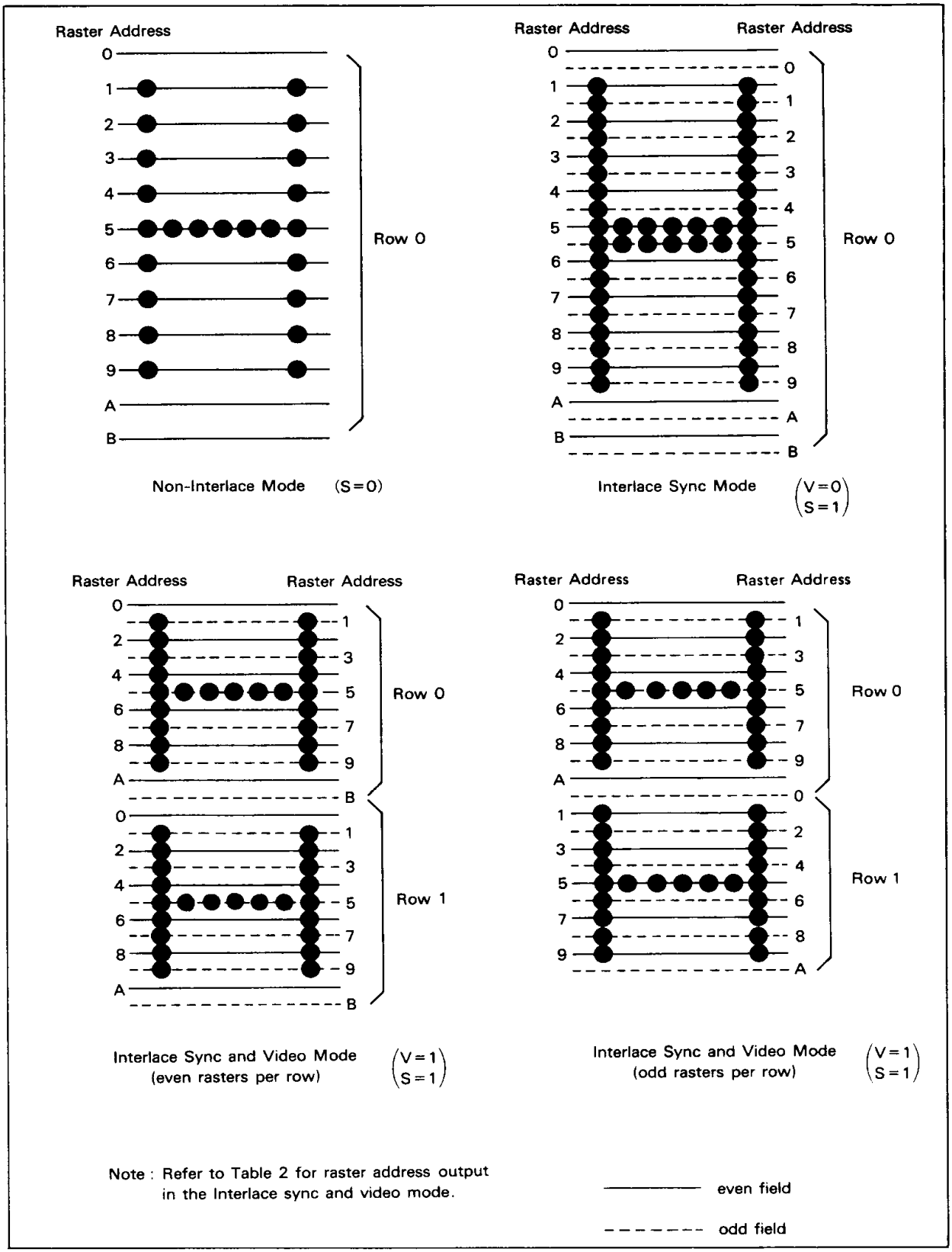


Figure 9 Raster Scanning Example

In the Interlace sync mode, the rasters in the odd field are placed downward by 1/2 raster line space from those in the even field because of the difference in HSYNC/VSYNC phases between two alternating fields.

In the Interlace sync and video mode, the placement of the rasters is the same as in the Interlace sync mode. However, the alternating even and odd resters are displayed in the alternating even and odd fields. Note that the raster address is supplied in the different way according to the total number of rasters in a row, even or odd, as shown in Table 4. Figure 9 illustrates the raster scanning example in each mode.

SMOOTH SCROLLING

Smooth scrolling in the vertical direction can be accomplished by changing the start raster address in a character row. Whether scrolling in each split-screen is available or not can be selected. Selected split-screens scroll in the same way up to four split-screens simultaneously.

Smooth scrolling is performed by the bits SS_1-SS_4 of the control 2 register (R31), and the smooth scrolling register (R29). It can be used in the Non-Interlace mode and the Interlace sync mode, but not in the Interlace sync and video mode.

Tabel 4 Start Raster Address for Each Row (In Interlace sync and video mode)

No. of Rasters per Row		Field	
		Even Field	Odd Field
Even		Even address	Odd address
Odd	Even Char. Row*	Even address	Odd address
	Odd Char. Row*	Odd address	Even address

* The start row address is assumed to be 0 (even).

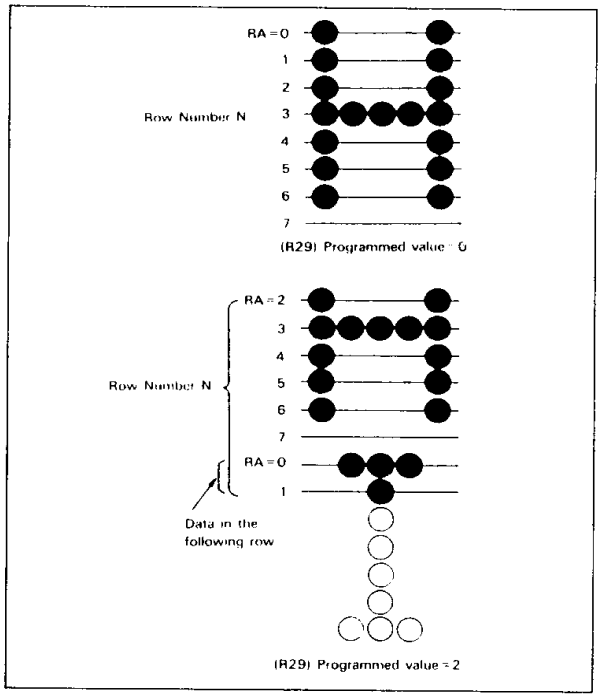


Figure 10 Smooth Scrolling

MEMORY WIDTH SETTING

The offset value is the difference between the display screen width and the display memory width in the horizontal direction. It can be specified in units of characters. (See Figure. 11)

Scrolling in any direction can be accomplished in units of characters, by setting the display memory width (horizontal direction) and the offset value, and by changing the start memory addresses. This is performed by the memory width offset register (R33) and the MW bit of the control 3 register (R32).

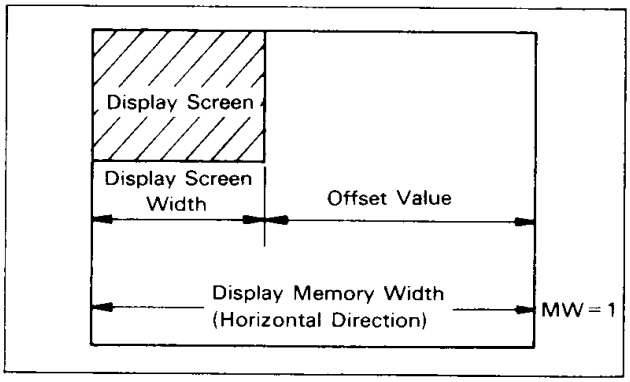


Figure 11 Memory Width

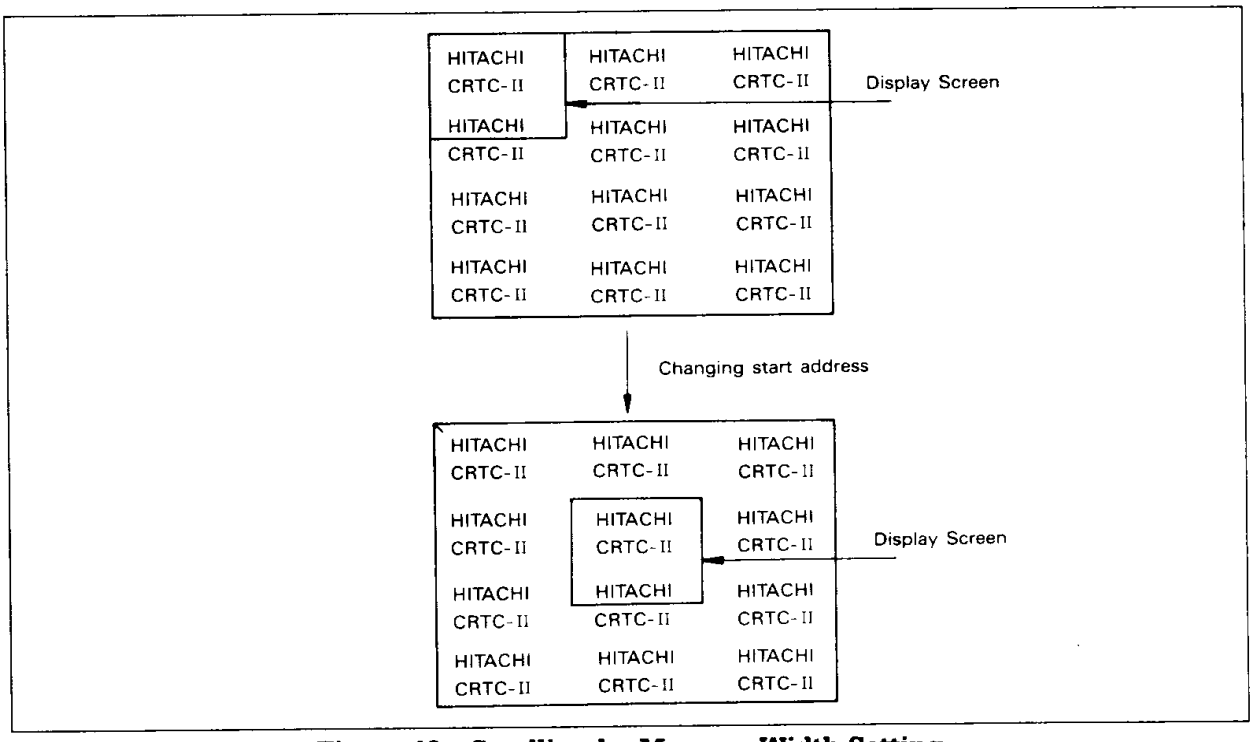
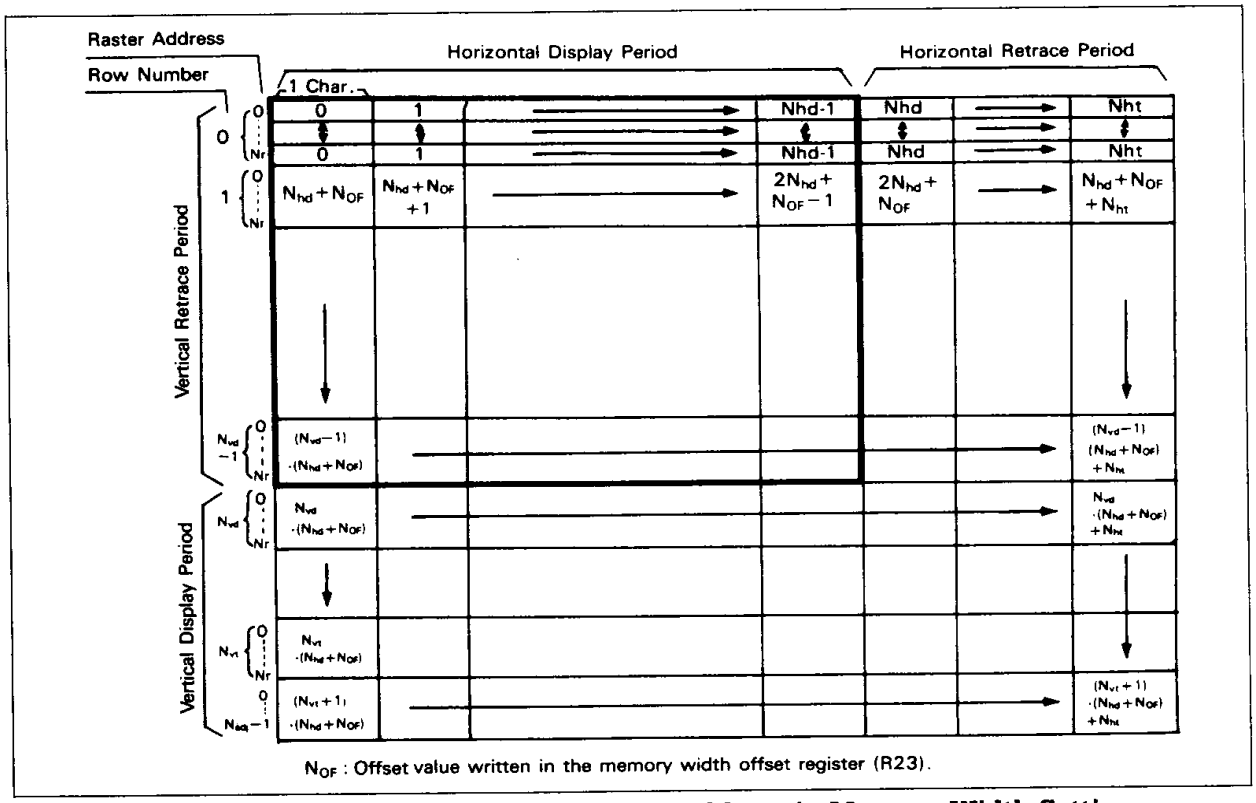


Figure 12 Scrolling by Memory Width Setting



NOF : Offset value written in the memory width offset register (R23).

Figure 13 Memory Address and Raster Address in Memory Width Setting

RASTER INTERPOLATION

Raster interpolation function increments the raster address every two rasters, doubling the vertical scan cycle; thus the display image is doubled in the vertical direction.

Raster interpolation function is controlled by the RI bit of the control 2 register (R31). This function can be used in the non-interlace mode and the interlace sync mode, but not in the interlace sync and video mode. Figure 14 is a display example using raster interpolation function.

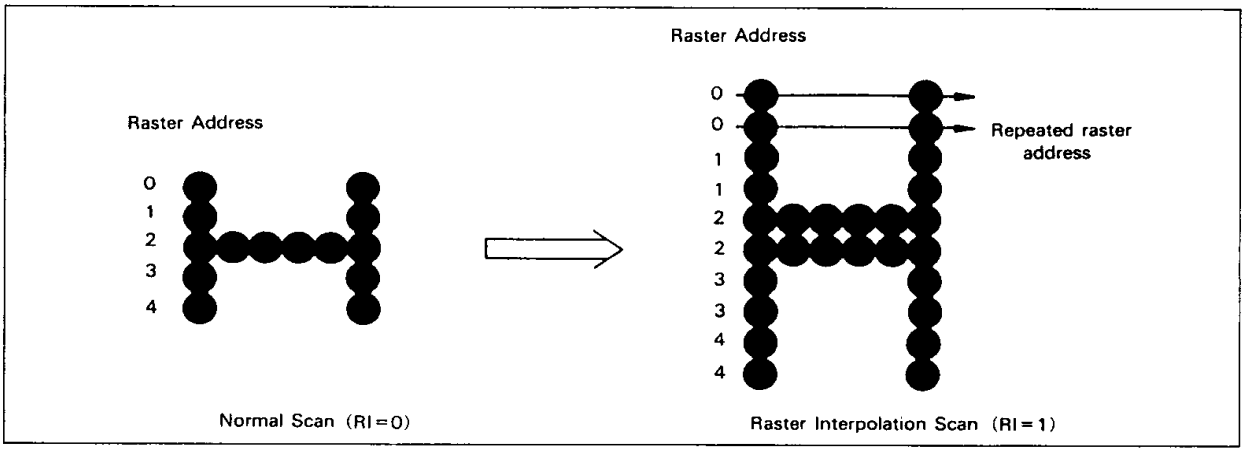


Figure 14 Raster Interpolation

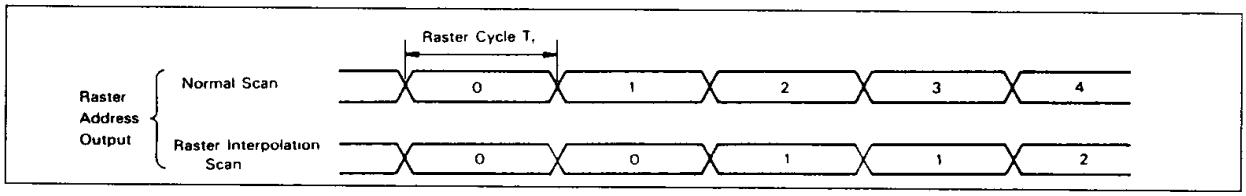


Figure 15 Raster Address Output and Raster Interpolation

EXTERNAL SYNCHRONIZATION

There are master/slave mode and TV sync mode in external synchronization.

The external synchronization is controlled by the bits VE, VS, and TV of the control 1 register (R30).

Master/slave mode is used to synchronize slave CRTC-IIs with a master CRTC-II by the VSYNC of a master CRTC-II. When superimposing a master screen with slave screen on the same CRT, clocks of a master and slave CRTC-IIs can operate in different frequency under conditions as follows.

(1) Phase of a master CRTC-II clock matches with a slave CRTC-II clock at rising edge of VSYNC.
(2) Both master and slave CRTC-IIs have the same horizontal/vertical scan cycle.

Figure 16 illustrates the system configuration. In the Interlace sync mode and the Interlace sync and video mode, the control 1 register must be set as to provide a VSYNC output in odd fields of a master CRTC-II.

TV sync mode is used to synchronize the CRTC-II with the HSYNC and VSYNC signals of a TV's video signal.

In the TV sync mode, the HSYNC/EXHSYNC pin inputs the EXHSYNC signal and the VSYNC/EXVSYNC pin inputs the EXVSYNC signal. The length of horizontal back porch is specified by the bits 0-3 of the sync width register (R3).

Figure 17 illustrates the system configuration.

In TV sync mode, when performing raster interpolation of slave CRTC-IIs, Interlace sync mode or Interlace sync and video mode must not be set in a master CRTC-II; this causes the screen moves up and down by one raster.

In the Interlace sync and video mode, the TV sync mode cannot be used.

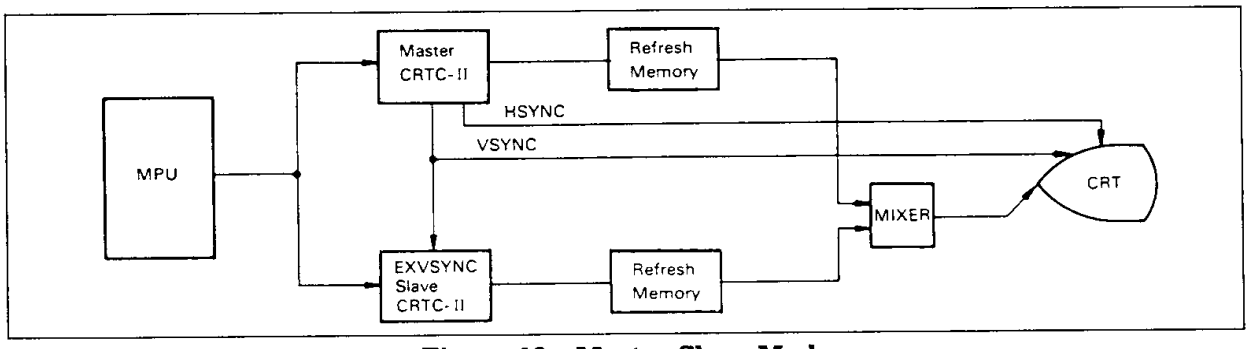


Figure 16 Master-Slave Mode

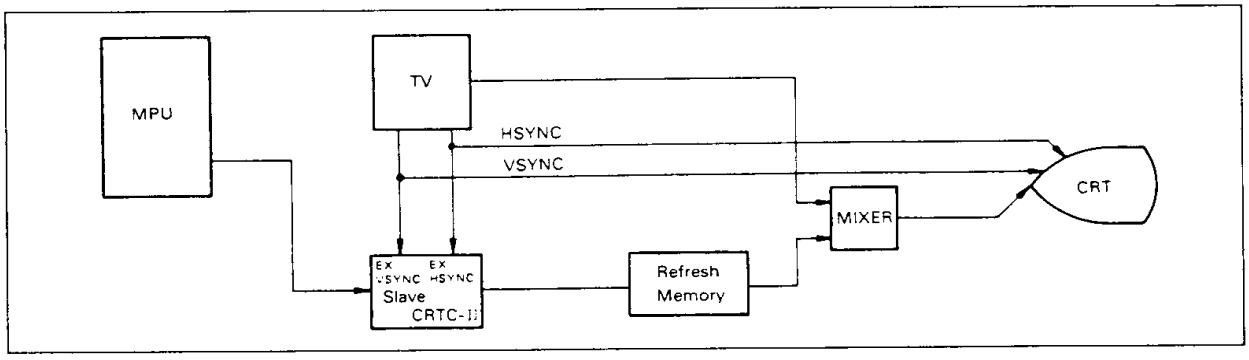


Figure 17 TV Sync Mode

Table 5 External Synchronization

				Function			
VE	**VS**	**TV**	**Mode**	**EXHSYNC /HSYNC**	**EXVSYNC /VSYNC**	**DISPTMG**	**States**
0	0	0	Master /slave mode	OUTPUT	OUTPUT	Active	Set as master CRTC-II in master-slave mode. "000" is to be set when CRTC-II is in nomal states (HD6845 compatible mode) or master mode.
0	1	0				"Low"	Set as master CRTC-II in master slave mode. Display is inhibited by setting DISPTMG "0". VSYNC signal is supplied only in odd field scan except the non-interlace mode.
1	0	0		OUTPUT	INPUT	Active	Set as slave CRTC-II in master slave mode. EXHSYNC is not used for the synchronization.
1	1	0				"Low"	Set as slave CRTC-II in master slave mode. EXVSYNC is used for the synchronization.
0	0	1	TV sync mode	INPUT	OUTPUT	Active	Program inhibited
0	1	1				"Low"	Program inhibited
1	0	1		INPUT	INPUT	Active	Set as slave CRTC-II in TV sync mode. EXHSYNC, EXVSYNC inputs are used as sync signal.
1	1	1				"Low"	Set as slave CRTC-II in TV sync mode. Display is inhibited by setting DISPTMG "0". EXHSYNC, EXVSYNC inputs are used as sync signal.

Note : Slave CRTC-IIs are always Non-Interlace mode in TV sync mode.

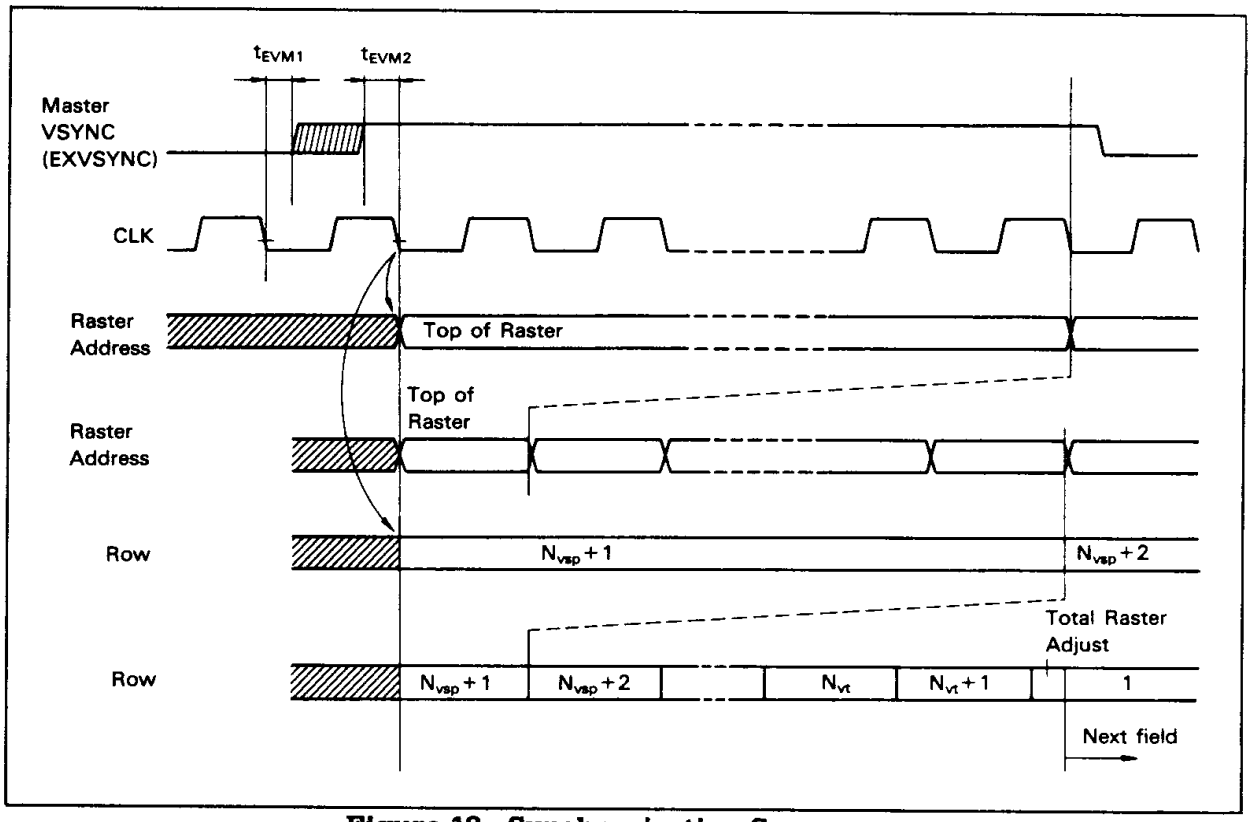


Figure 18 Synchronization Sequence

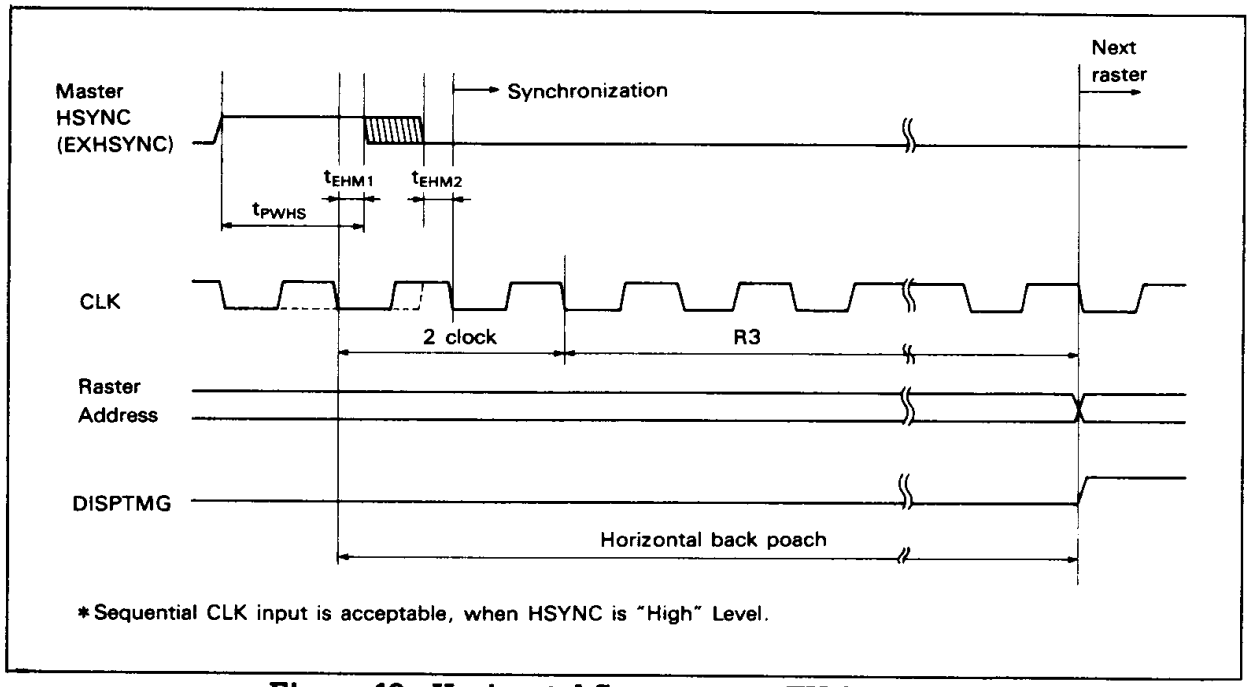


Figure 19 Hosizontal Sequence on TV Sync Mode

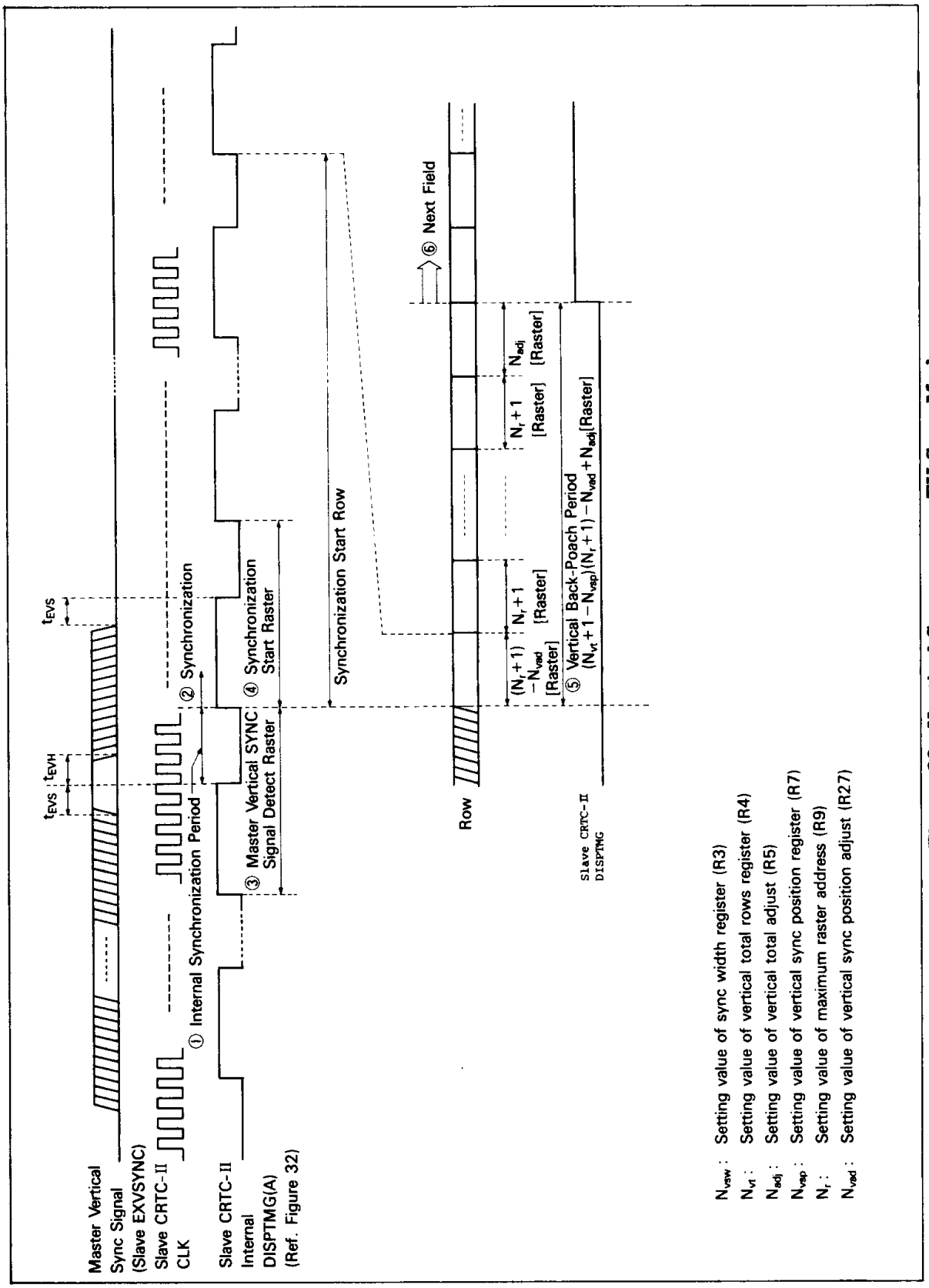


Figure 20 Vertical Sequence on TV Sync Mode

2

INTERRUPT REQUEST

An interrupt request signal to the MPU is output in the timing shown in Figure 21. Interrupt request is generated by the vertical retrace period, or the light pen input.

Reading the status register (R31) clears interrupt request signal. Thus, if the MPU does not read the status register (R31) when an interrupt request is generated, an interrupt request signal is output during all the horizontal and vertical retrace periods.

In the MPRAM mode, an interrupt request signal is not output.

An interrupt request is controlled by the bits IB and IL of the control 1 register (R30).

Table 6 Interrupt Control

IB	IL	Source of Interrupt Request
0	0	None
0	1	Light pen strobe
1	0	Vertical retrace
1	1	Light pen strobe and/or vertical retrace

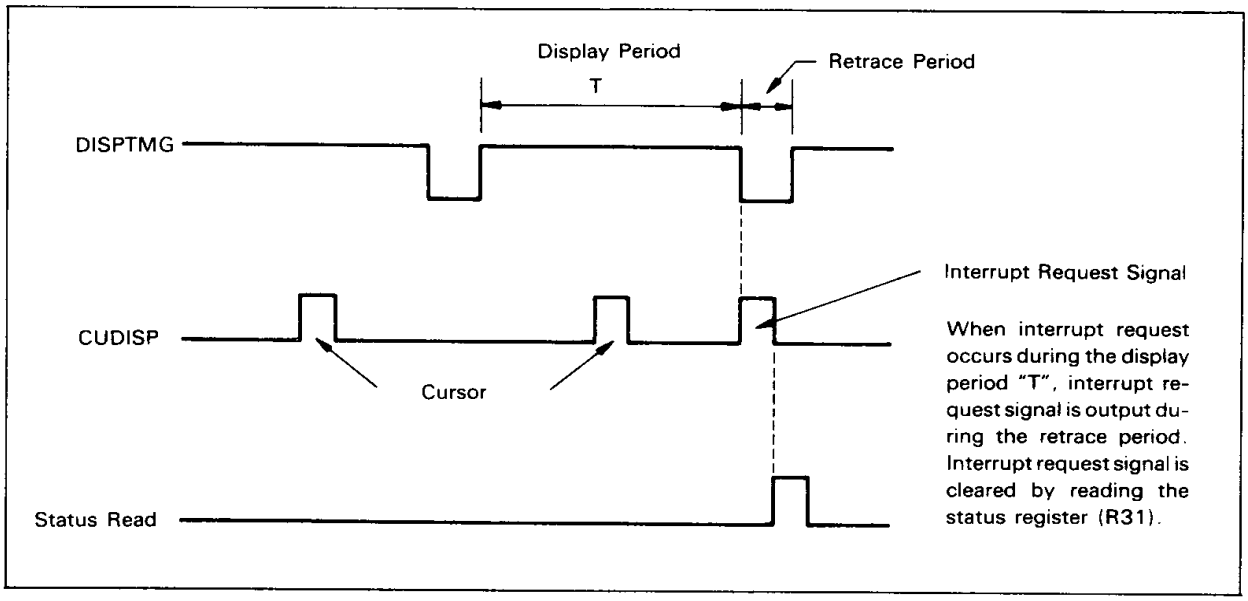


Figure 21 Interrupt Timing

THREE-STATE CONTROL OF MA/RA

Memory address (MA) and raster address (RA) outputs can be three-stated, using the TSC input pin. Three-state control is enabled by setting the TC bit of the control 3 register (R32).

When three-state control is used, a multiplexer (MPX) to select address lines from the MPU and the CRTC-II for refresh memory is not required, as shown in Figure 22.

MPRAM MODE

When the MPRAM mode is selected (DR=1), the HD6445 generates a programmable timing signal from the access inhibit pin. This signal, shown in Figure 23 as access inhibit period, provides the timing for the MPU to access to multi-port memory.

In the MPRAM mode, an interrupt request signal is not output, and the cursor 2 is not displayed.

This timing signal is controlled by the DR bit of the control 3 register (R32), and the cursor 2 width register (R39).

2

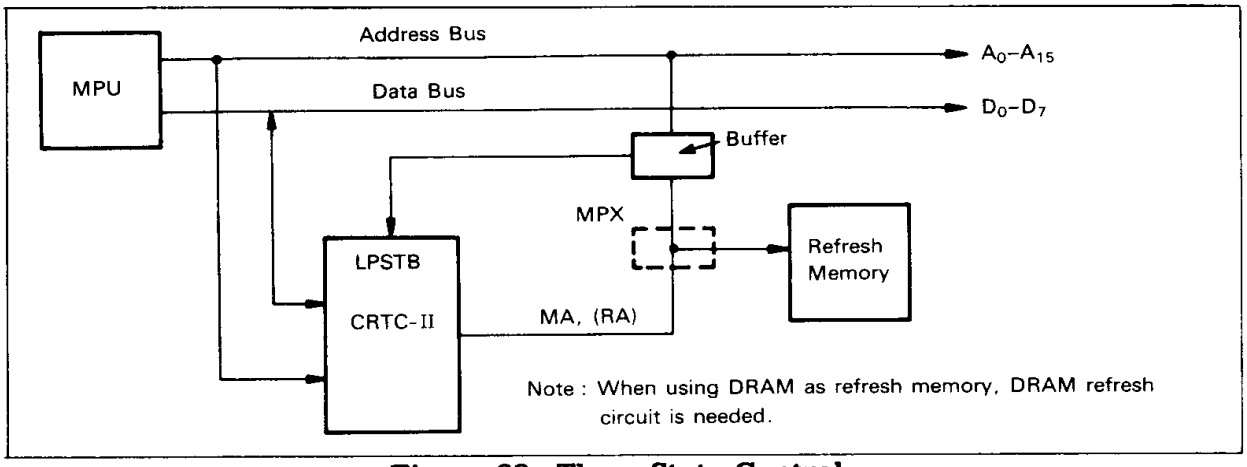


Figure 22 Three-State Control

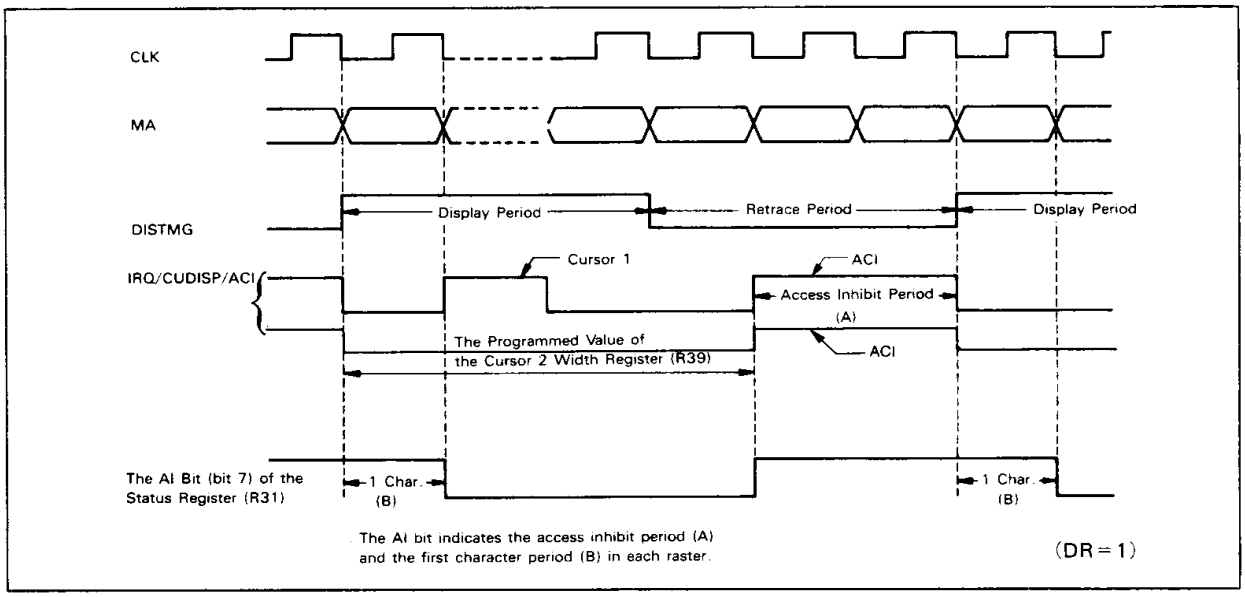


Figure 23 MPRAM Mode Output Timing

SKEW

D_1	D_0	DISPTMG
0	0	No skew
0	1	One character skew
1	0	Two character skew
1	1	Not available ("Low" fixing)

C_1	C_0	CUDISP
0	0	No skew
0	1	One character skew
1	0	Two character skew
1	1	Not available ("Low" fixing)

LIGHT PEN

The R16 and R17 registers latches the light pen detection address. R28 register latches the light pen detection raster address and the detection period. The DP bit is set to 1 when the LPSTB is detected during the display period; cleared 0 during the retrace period.

VERTICAL SYNC POSITION ADJUST

The R27 register performs a fine adjustment to the vertical sync signal output in units of rasters. The VSYNC signal is supplied after the delay of Nvad rasters. R27 register is enabled when 1 is set into the SY bit of the control 1 register (R30).

STATUS

E	Status
0	During odd field display
1	During even field display

SB	Status
0	Not during vertical retrace
1	During vertical retrace

SL	Status
0	Light pen strobe not detected
1	Light pen strobe detected

AI	Status
0	Refresh memory access allowed
1	Refresh memory access inhibited

INTERNAL REGISTER ASSIGNMENT

		Register Address	Reg.		Program			Data Bit							
CS	RS	5 4 3 2 1 0	No.	Register Name	Unit	Symbol	R/W	7	6	5	4	3	2	1	0
1	×	× × × × × ×	–	–	–	–	–								
0	0	× × × × × ×	AR	ADDRESS REGISTER	–	–	W								
0	1	0 0 0 0 0 0	R0	HORIZONTAL TORAL CHARACTERS	character	Nht	W								
0	1	0 0 0 0 0 1	R1	HORIZONTAL DISPLAYED CHARACTERS	character	Nhd	W								
0	1	0 0 0 0 1 0	R2	HORIZONTAL SYNC POSITION	character	Nhsp	W								
0	1	0 0 0 0 1 1	R3	SYNC WIDTH	*	Nvsw, Nhsw	W	Wv_3	Wv_2	Wv_1	Wv_0	Wh_3	Wh_2	Wh_1	Wh_0
0	1	0 0 0 1 0 0	R4	VERTICAL TORAL ROWS	row	Nvt	W								
0	1	0 0 0 1 0 1	R5	VERTICAL TORAL ADJUST	raster	Nadj	W								
0	1	0 0 0 1 1 0	R6	VERTICAL DISPLAYED ROWS	row	Nvd	W								
0	1	0 0 0 1 1 1	R7	VERTICAL SYNC POSITION	row	Nvsp	W								
0	1	0 0 1 0 0 0	R8	INTERLACE MODE AND SKEW	–	–	W	C_1	C_0	D_1	D_0			V	S
0	1	0 0 1 0 0 1	R9	MAX RASTER ADDRESS	raster	Nr	W								
0	1	0 0 1 0 1 0	R10	CURSOR 1 START	raster	Ncs_1	W		B_1	P_1					
0	1	0 0 1 0 1 1	R11	CURSOR 1 END	raster	Nce_1	W								
0	1	0 0 1 1 0 0	R12	SCREEN 1 START ADDRESS (H)	memory address	–	R/W								

Note 1) *: Vertical: raster/Horizontal: character.
2) ▨ : "0" is to be set, since these bits may be used in the future.

CS	RS	Register Address 5 4 3 2 1 0	Reg. No.	Register Name	Program Unit	Symbol	R/W	Data Bit 7	6	5	4	3	2	1	0
0	1	0 0 1 1 0 1	R13	SCREEN 1 START ADDRESS (L)	memory address	–	R/W								
0	1	0 0 1 1 1 0	R14	CURSOR 1 ADDRESS (H)	memory address	–	R/W								
0	1	0 0 1 1 1 1	R15	CURSOR 1 ADDRESS (L)	memory address	–	R/W								
0	1	0 1 0 0 0 0	R16	LIGHT PEN (H)	–	–	R								
0	1	0 1 0 0 0 1	R17	LIGHT PEN (L)	–	–	R								
0	1	0 1 0 0 1 0	R18	SCREEN 2 START POSITION	row	–	R/W								
0	1	0 1 0 0 1 1	R19	SCREEN 2 START ADDRESS (H)	memory address	–	R/W								
0	1	0 1 0 1 0 0	R20	SCREEN 2 START ADDRESS (L)	memoey address	–	R/W								
0	1	0 1 0 1 0 1	R21	SCREEN 3 START POSTION	row	–	R/W								
0	1	0 1 0 1 1 0	R22	SCREEN 3 START ADDRESS (H)	memory address	–	R/W								
0	1	0 1 0 1 1 1	R23	SCREEN 3 START ADDRESS (L)	memory address	–	R/W								
0	1	0 1 1 0 0 0	R24	SCREEN 4 START POSITION	row	–	R/W								
0	1	0 1 1 0 0 1	R25	SCREEN 4 START ADDRESS (H)	memory address	–	R/W								
0	1	0 1 1 0 1 0	R26	SCREEN 4 START ADDRESS (L)	memory address	–	R/W								
0	1	0 1 1 0 1 1	R27	VERTICAL SYNC POSITION ADJUST	raster	Nvad	W								
0	1	0 1 1 1 0 0	R28	LIGHT PEN RASTER	–	–	R	DP							
0	1	0 1 1 1 0 1	R29	SMOOTH SCROLLING	raster	Nss	R/W								
0	1	0 1 1 1 1 0	R30	CONTROL 1	–	–	W	VE	VS	IB	IL	SY	TV	SP_1	SP_0
0	1	0 1 1 1 1 1	R31	CONTROL 2	–	–	W	SS_4	SS_3	SS_2	SS_1	RI			
				STATUS	–	–	R	AI					E	SB	SL
0	1	1 0 0 0 0 0	R32	CONTROL 3	–	–	W	CM	C_2	CW_1	CW_2	MW	TC	DR	
0	1	1 0 0 0 0 1	R33	MEMORY WIDTH OFFSET	character	Nof	R/W								
0	1	1 0 0 0 1 0	R34	CURSOR 2 START	raster	Ncs_2	W			B_2	P_2				
0	1	1 0 0 0 1 1	R35	CURSOR 2 END	raster	Nce_2	W								
0	1	1 0 0 1 0 0	R36	CURSOR 2 ADDRESS (H)	memory address	–	R/W								
0	1	1 0 0 1 0 1	R37	CURSOR 2 ADDRESS (L)	memory address	–	R/W								
0	1	1 0 0 1 1 0	R38	CURSOR 1 WIDTH	character	Ncw_1	R/W								
0	1	1 0 0 1 1 1	R39	CURSOR 2 WIDTH	character	Ncw_2	R/W								

Note 1) *: Vertical: raster/Horizontal: character.
2) ▨ : "0" is to be set, since these bits may be used in the future.

RESET

The $\overline{RES}$ functions as a reset input signal only while the LPSTB is "L". "Reset" is definable in two stages.

(1) "During a reset state" indicates the period that the $\overline{RES}$ remains "L".

(2) "After a reset state" indicates the state after the $\overline{RES}$ transition from "L" to "H".

The pin status during a reset state is in Table 7.

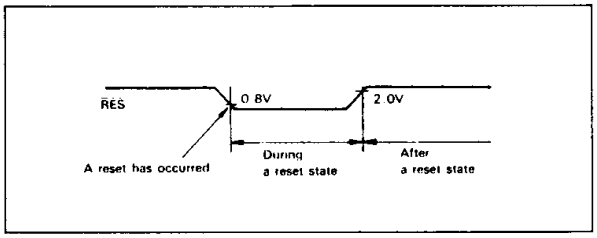


Figure 24 Reset Definition

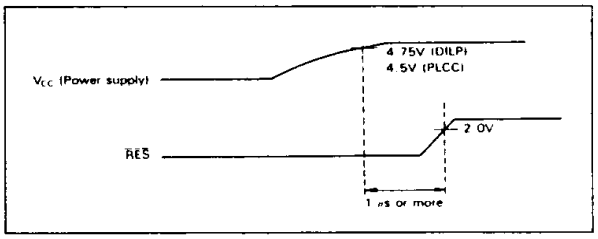


Figure 25 Reset at Power-on

Table 7 Pin Status during a Reset State

Pin No. DP-40	Pin No. CP-44	Symbol	Pin Name	Input/ Output	Pin Status
1	1, 2	V_{SS} ($V_{SS}1$, $V_{SS}2$)**	V_{SS}	–	–
2	3	$\overline{RES}$	RESET	Input	–
3	4	LPSTB	LIGHT PEN STROBE	Input	"L" level signal requested to be supplied
		$\overline{TSC}$	THREE STATE CONTROL	Input	
4-17	5-11 13-19	MA0-MA13	MEMORY ADDRESS 0-13	Output	Goes "L" immediately after reset
18	20	DISPTMG	DISPLAY TIMING	Output	Goes "L" immediately after reset
19	21	CUDISP	CURSOR DISPLAY	Output	Goes "L" immediately after reset
		ACI	ACCESS INHIBIT	Output	
		$\overline{IRQ}$	INTERRUPT REQUEST	Output	
20	22, 23	V_{CC} ($V_{CC}1$, $V_{CC}2$)**	V_{CC}	–	–
21	24	CLK	CHARACTER CLOCK	Input	Not affected
22	25	R/$\overline{W}$ ($\overline{WR}$)*	READ/WRITE (WRITE)*	Input	Not affected
23	26	E ($\overline{RD}$)*	ENABLE (READ)*	Input	Not affected
24	27	RS	REGISTER SELECT	Input	Not affected
25	28	$\overline{CS}$	CHIP SELECT	Input	Not affected
33-26	37-35 33-29	D0-D7	DATA BUS 0-7	Input/ Output	Not affected
38-34	42-38	RA0-RA4	RASTER ADDRESS 0-4	Output	Goes "L" immediately after reset
39	43	HSYNC	HORIZONTAL SYNC	Output	Outputs HSYNC signal until external sunch mode is set into the control 1 register (R29) after reset
		EXHSYNC	EXTERNAL HORIZONTAL SYNC	Input	
40	44	VSYNC	VERTICAL SYNC	Output	Outputs VSYNC signal until external sync mode is set into the control 1 register (R29) after reset
		EXVSYNC	EXTERNAL VERTICAL SYNC	Input	

Note : * marked pins are of the HD6445
** marked pins are of the CP-44

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}*	−0.3 to +7.0	V
Input Voltage		V_{in}*	−0.3 to V_{CC} +0.3	V
Operating Temperature		T_{opr}	−20 to +75	°C
Storage Temperature		T_{stg}	−55 to +150	°C
Allowable Output Current	Data Bus	$\|I_O\|$**	5	mA
	Others		3	mA
Total Allowable Output Current		$\|\Sigma I_O\|$***	60	mA

* This value is in reference to V_{SS} = 0V.
** The allowable output current is the maximum current that may be drawn from, of flow out to, one output pin or one input/output common pin.
*** The total allowable output current is the toral sum of currents that may be drawn from, or flow out to, output pins or input/output common pin.
Note: Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be under recommended operating conditions.
Exceeding any of these conditions may adversely affect its reliability.

RECOMMENDED OPERATING CONDITIONS

Item		Symbol	Min	Typ	Max	Unit
Power Supply Voltage	DP-40	V_{CC}*	4.75	5.0	5.25	V
	CP-44		4.5		5.5	
Input Low Level Voltage		V_{IL}*	−0.3	—	0.8	V
Input High Level Voltage		V_{IH}*	2.0	—	V_{CC}	V
Operating Temperature		T_{opr}	−20	25	75	°C

* This value is in reference to V_{SS} = 0V.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{CC}=5.0V ±5 % (DILP), 5.0 ±10 % (PLCC), V_{SS}=0V, T_a=−20 to +75°C (Normal) −40 to +85°C (J), unless otherwise noted)

Item		Symbol	Min	Typ*	Max	Unit	Test Conditions
Input High Level Voltage		V_{IH}	2.0	—	V_{CC}	V	
Input Low Level Voltage		V_{IL}	−0.3	—	0.8	V	
Input Leak Current	Input except D_0-D_7	I_{in}	−2.5	—	2.5	μA	V_{in}=0 to 5.25 V
Three-State (Off State) Input Current	D_0-D_7 Memory Address Raster Address	I_{TSI}	−10	—	10	μA	V_{in}=0.4 to 2.4 V V_{CC}=5.25 V
Output High Level Voltage	D_0-D_7	V_{OH}	2.4	—	—	V	I_{OH}=-205μA
	Others						I_{OH}=-100μA
Output Low Level Voltage		V_{OL}	—	—	0.4	V	I_{OL}=1.6mA
Input Capacity	D_0-D_7 EXVSYNC EXHSYNC	C_{in}	—	—	12.5	pF	V_{in}=0 V T_a=25°C f=1.0 MHz
	Others		—	—	10	pF	
Output Capacity		C_{out}	—	—	10	pF	V_{in}=0 V T_a=25°C f=1.0 MHz
Power Dissipation	No Load	P_D	—	50	100	mW	f_{CLK}=4.5 MHz f_E=2.0 MHz V_{CC}=max V_{IH}=V_{CC}-1.0 V V_{IL}=0.8 V
	Test Load			100	200		

* T_a=2.5°C, V_{CC}=5.0 V

AC CHARACTERISTICS

(V_{CC}=5.0V ±5 % (DILP), 5V ±10 % (PLCC), V_{SS}=0V, T_a= −20 to +75°C (Normal), −40 to +85°C (J), unless otherwise noted.)

1. Timing of CRT control signal

Item	Symbol	Min	Typ	Max	Unit	Reference Figure
Clock Cycle Time	tcycC	220	–	–	ns	Fig. 26
Clock High Pulse Width	PW_{CH}	100	–	–	ns	
Clock Low Pulse Width	PW_{CL}	100	–	–	ns	
Rise and Fall Time for Clock Input	tcr, tcf	–	–	20	ns	
Memory Address Delay Time	t_{MAD}	–	–	80	ns	
Raster Address Delay Time	t_{RAD}	–	–	80	ns	
DISPTMG Delay Time	t_{DTD}	–	–	120	ns	
CUDISP Delay Time	t_{CDD}	–	–	120	ns	
Horizontal Sync Delay Time	t_{HSD}	–	–	100	ns	
Vertical Sync Delay Time	t_{VSD}	15*	–	120	ns	
Light Pen Strobe Pulse Width	PW_{LPH}	60	–	–	ns	
Light Pen Strobe Uncertain Time of Acceptance	t_{LPD1}	–	–	70	ns	Fig. 28
	t_{LPD2}	–	–	0	ns	Fig. 29
Memory Address Three-State Off Time	t_{MAZ}	–	–	50	ns	Fig. 27
Raster Address Three-State Off Time	t_{RAZ}	–	–	50	ns	

Note*: Application after mark 7C1

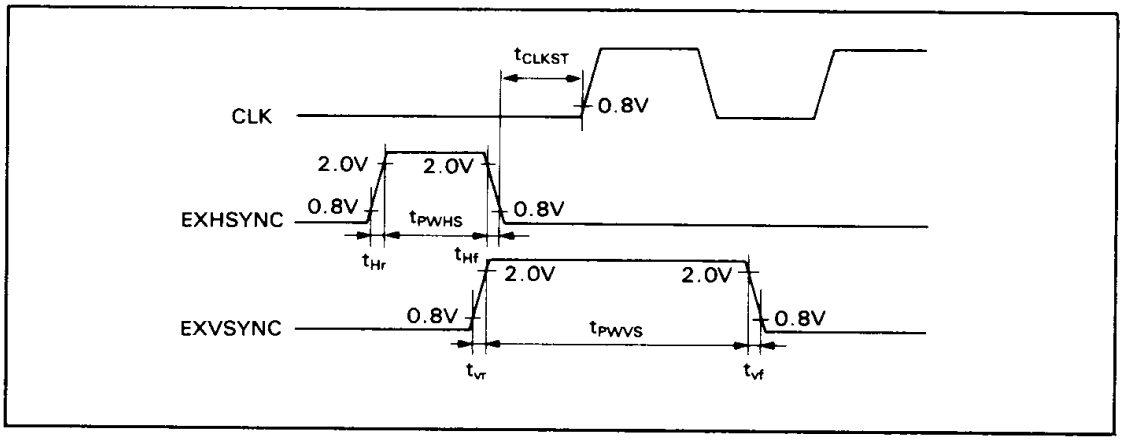
2. External sync timing

Item	Symbol	Min	Typ	Max	Unit	Reference Figure
External Vertical Sync Pulse Width*	t_{PWVS}	$2 \cdot t_{cyc}C$	–	–	ns	Fig. 32
External Vertical Sync Rise and Fall Time	t_{vr}	–	–	20	ns	
	t_{vf}	–	–	20	ns	
Master Slave Mode. EXVSYNC Uncertain Time of Acceptance	t_{EVM1}	10	–	–	ns	Fig.30
	t_{EVM2}	60	–	–	ns	
External Horizontal Sync Pulse Width	t_{PWHS}	$2 \cdot t_{cyc}C$	–	–	ns	Fig.31
External Horizontal Sync Rise and Fall Time	t_{Hr}	–	–	20	ns	Fig.32
	t_{Hf}	–	–	20	ns	
TV sync mode. EXHSYNC Uncertain Time of Acceptance	t_{EHT1}	30	–	–	ns	
	t_{EHT2}	50	–	–	ns	
TV Sync mode. EXVSYNC set-up Time	t_{EVS}	50	–	–	ns	
TV Sync mode. EXVSYNC Hold Time	t_{EVH}	50	–	–	ns	

Note * : Normal application add input over 1H (One raster period)
The above specification is applied after mark 7C1.
The following specification is applied before it.
The above specification is upward-compatible with the following specification.

External sync timing

Item	Symbol	Min	Typ	Max	Unit
Clock Halt Time	t_{CLKST}	100	–	–	ns
External Horizontal Sync Pulse Width	t_{PWHS}	1000	–	–	ns
External Horizontal Sync Rise and Fall Time	t_{Hr}	–	–	20	ns
	t_{Hf}	–	–	20	ns
External Vertical Sync Pulse Width	t_{PWVS}	1660	–	–	ns
External Vertical Sync Rise and Fall Time	t_{Vr}	–	–	20	ns
	t_{Vf}	–	–	20	ns



3. MP Bus Timing

(1) HD6345 MPU bus timing

Item	Symbol	6345 Min	6345 Max	63A45 Min	63A45 Max	63B45 Min	63B45 Max	Unit	Reference Figure
Enable Cycle Time	$tcyc_E$	1000	–	666	–	500	–	ns	Fig. 33
Enable High Pulse Width	PW_{EH}	450	–	280	–	220	–	ns	Fig. 34
Enable Low Pulse Width	PW_{EL}	400	–	280	–	210	–	ns	
Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	20	–	20	–	20	ns	
Address Setup Time	t_{AS}	80	–	80	–	40	–	ns	
Data Setup Time	t_{DSW}	195	–	80	–	60	–	ns	
Data Delay Time	t_{DDR}	–	200	–	140	–	120	ns	
Data Hold Time	t_H	10	–	10	–	10	–	ns	
Address Hold Time	t_{AH}	10	–	10	–	10	–	ns	
Data Access Time	t_{ACC}	–	280	–	220	–	160	ns	
Input Signal Rise and Fall Time ($\overline{RES}$, LPSTB, RS, $\overline{CS}$, R/$\overline{W}$)	tr, tf	–	100	–	100	–	100	ns	

(2) HD6445 MPU bus timing

Item	Symbol	Min	Typ	Max	Unit	Reference Figure
Read Address Setup Time	t_{AR}	0	–	–	ns	Fig. 35
Read Low Level Time	t_{RR}	160	–	–	ns	Fig. 36
Read Address Hold Time	t_{RA}	0	–	–	ns	
Write Address Setup Time	t_{AW}	0	–	–	ns	
Write Low Level Time	t_{WW}	190	–	–	ns	
Write Address Hold Time	t_{WA}	0	–	–	ns	
Data Delay Time	t_{RD}	–	–	120	ns	
Data Hold Time (Read)	t_{DF}	10	–	–	ns	
Data Setup Time	t_{DW}	60	–	–	ns	
Data Hold Time (Write)	t_{WD}	0	–	–	ns	
Access Inhibit Time	t_{DIS}	210	–	–	ns	
Input Signal Rise Time, Fall Time ($\overline{RES}$, LPSTB, RS, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$)	t_r t_f	–	–	100	ns	

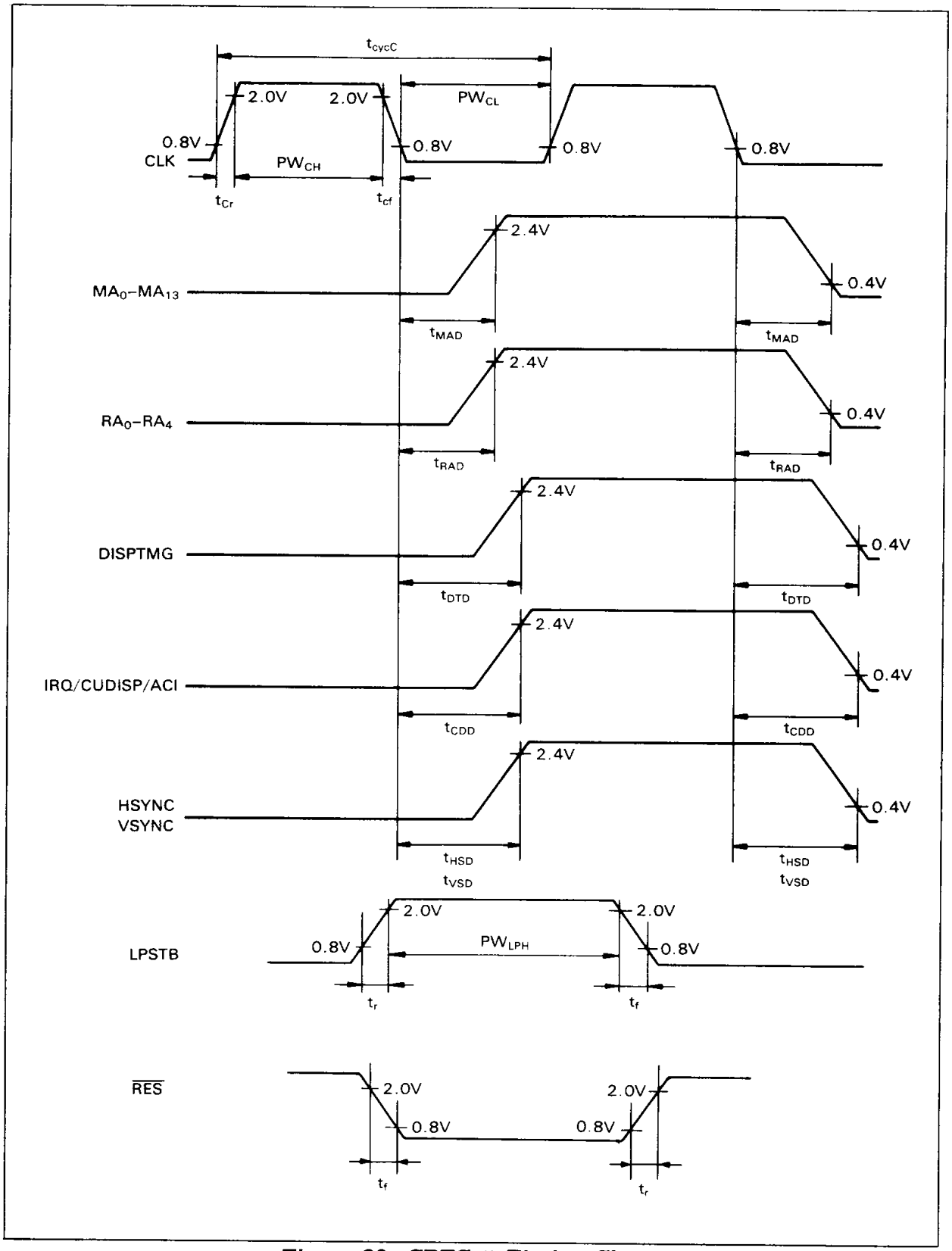
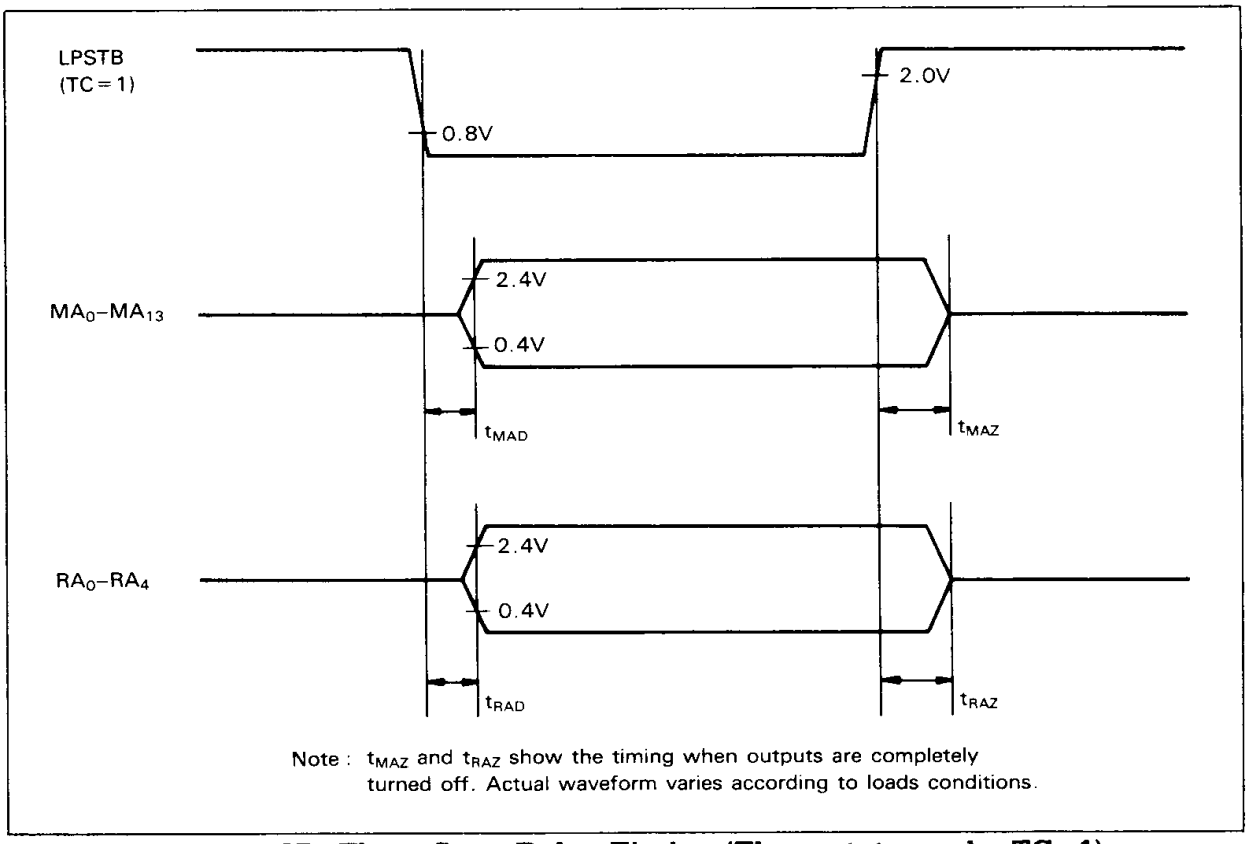


Figure 26 CRTC-II Timing Chart



Note : t_{MAZ} and t_{RAZ} show the timing when outputs are completely turned off. Actual waveform varies according to loads conditions.

Figure 27 Three-State Delay Timing (Three-state mode: TC=1)

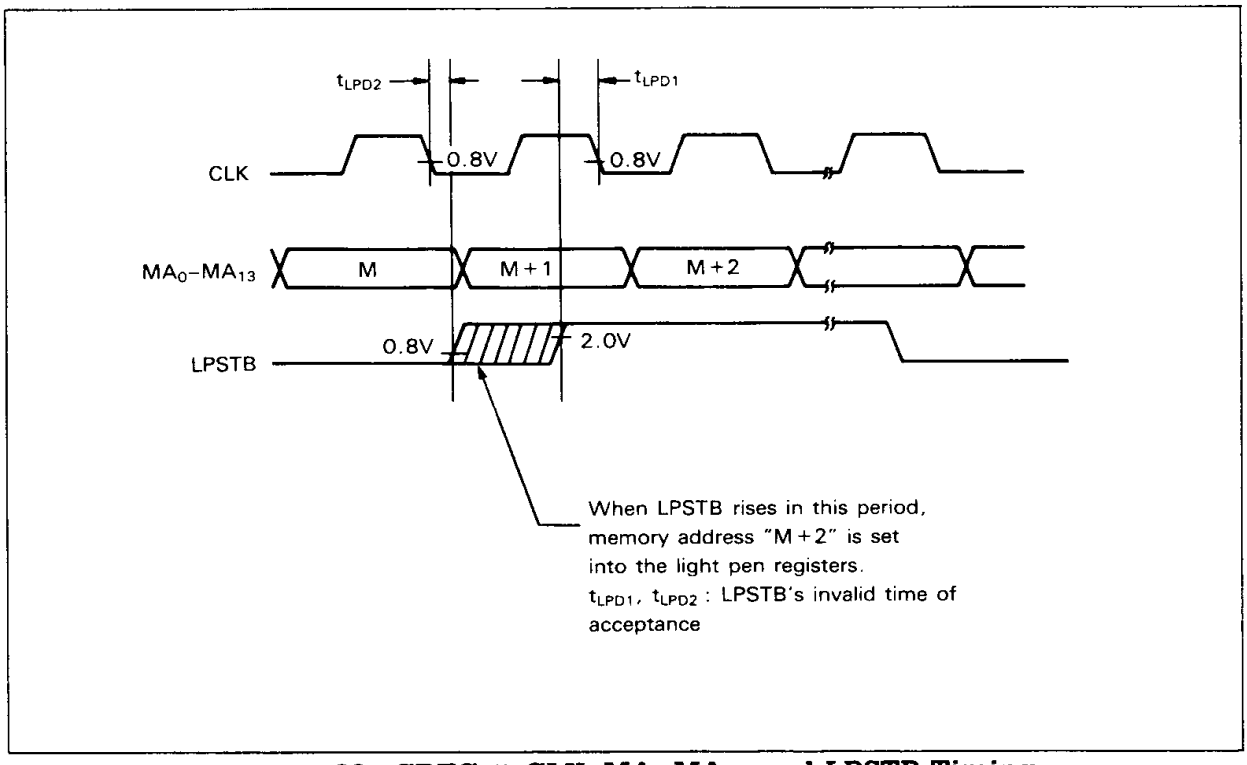


Figure 28 CRTC-II CLK, MA_0-MA_{13}, and LPSTB Timing

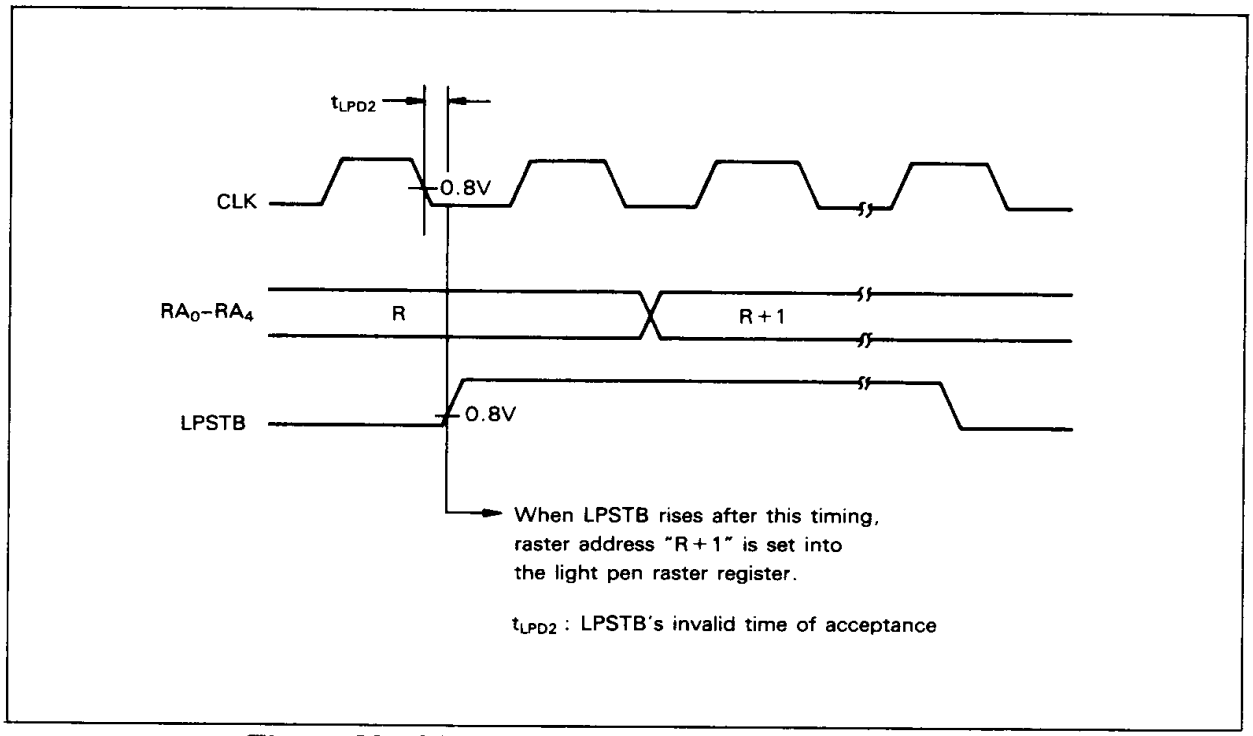


Figure 29 CRTC-II CLK, RA_0-RA_4 and LPSTB Timing

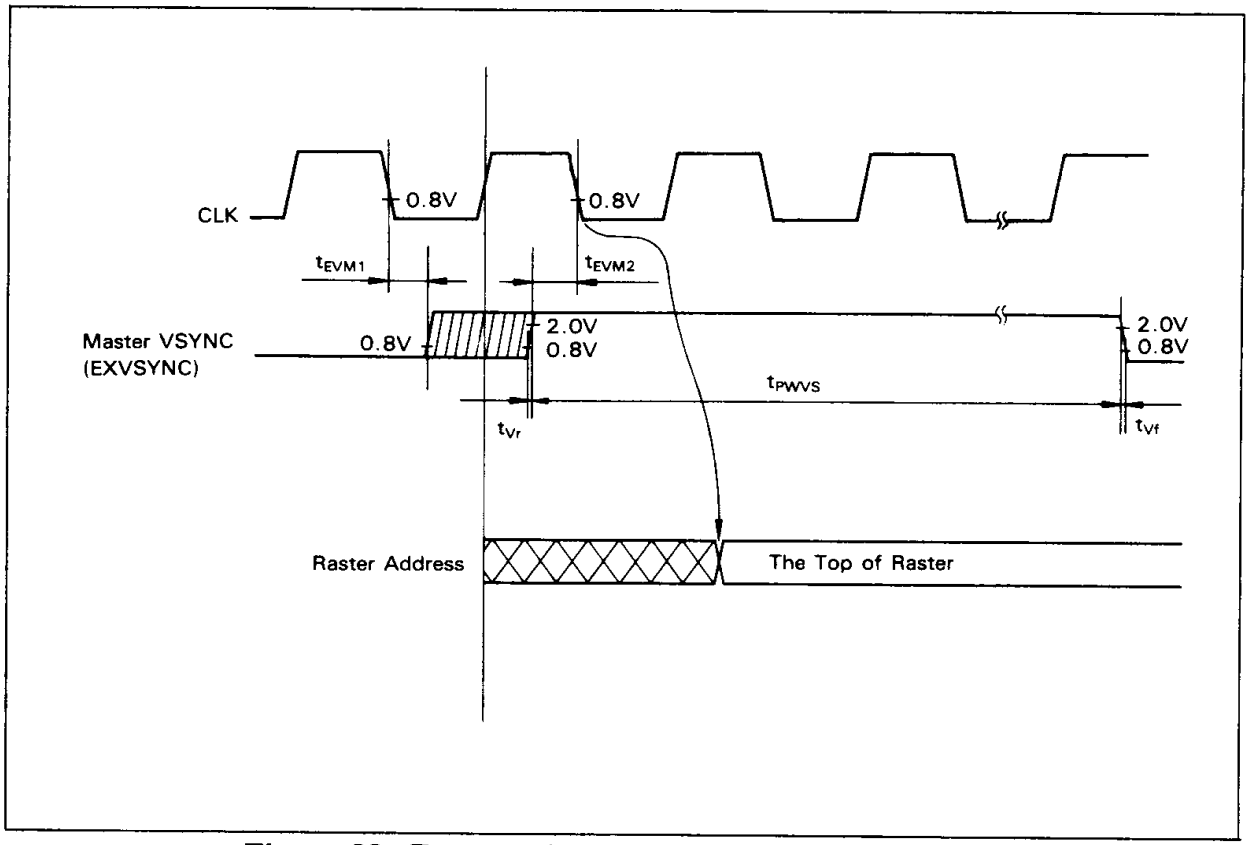


Figure 30 External Sync Timing (Master/Slave Mode)

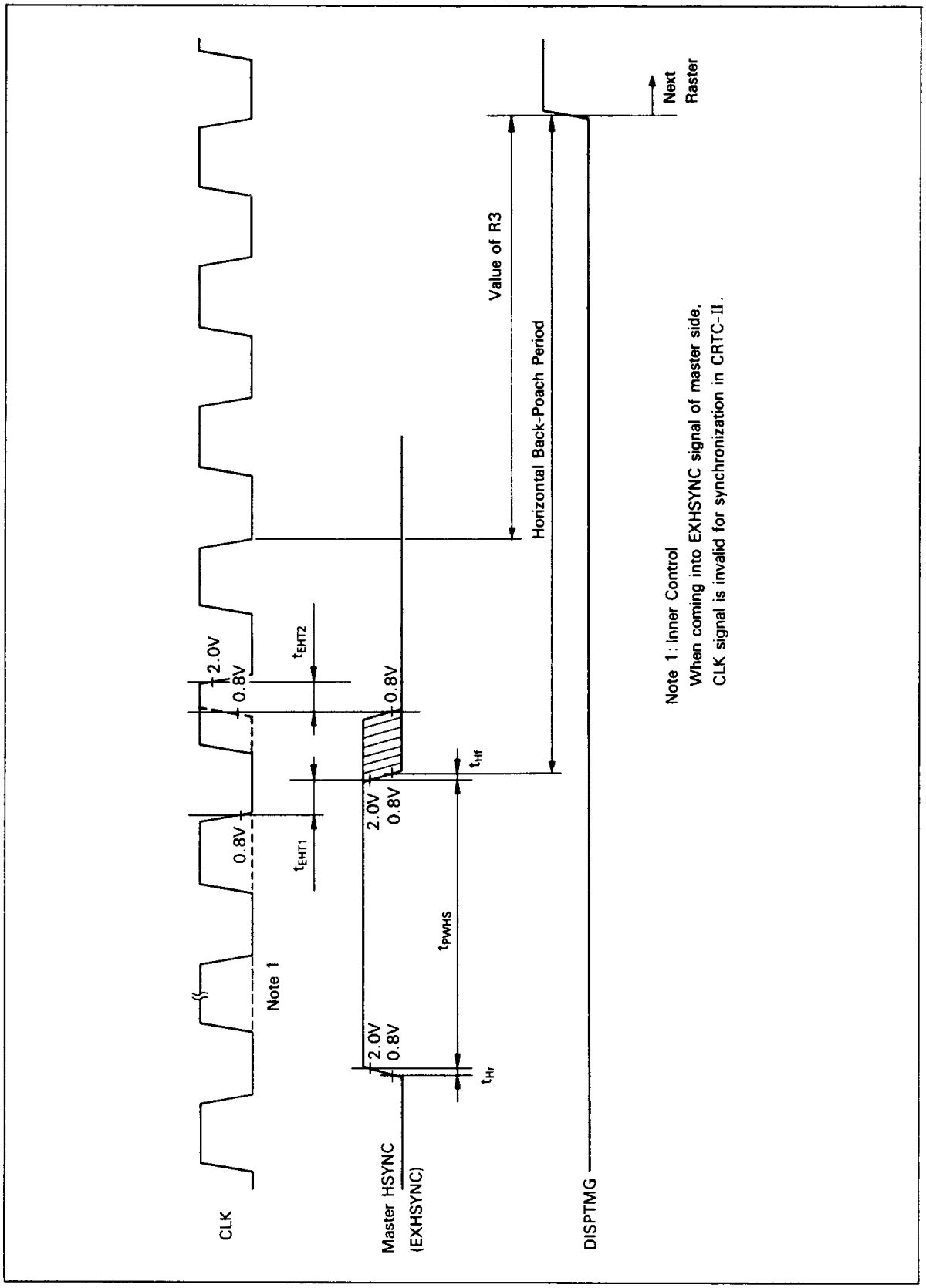


Figure 31 External Sync Timing (TV Sync Mode: EXHSYNC)

2

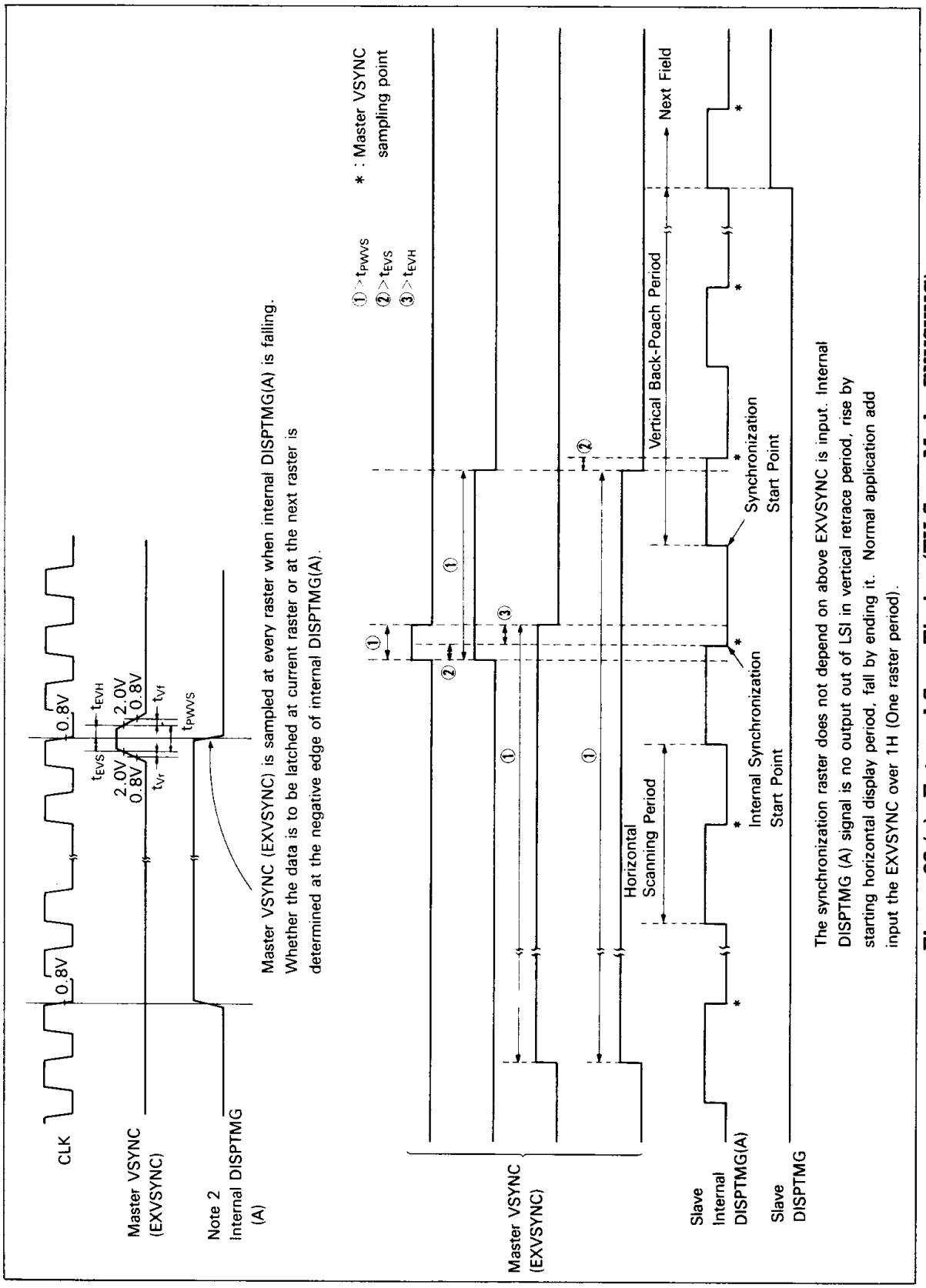


Figure 32-(a) External Sync Timing (TV Sync Mode: EXVSYNC)

Note : Internal DISPTMG
Internal DISPTMG (A) : The internal DISPTMG (A) show the display signal of the horizontal direction in circuit.
Internal DISPTMG (B) : The internal DISPTMG (B) show the display signal of the vertical direction in circuit.

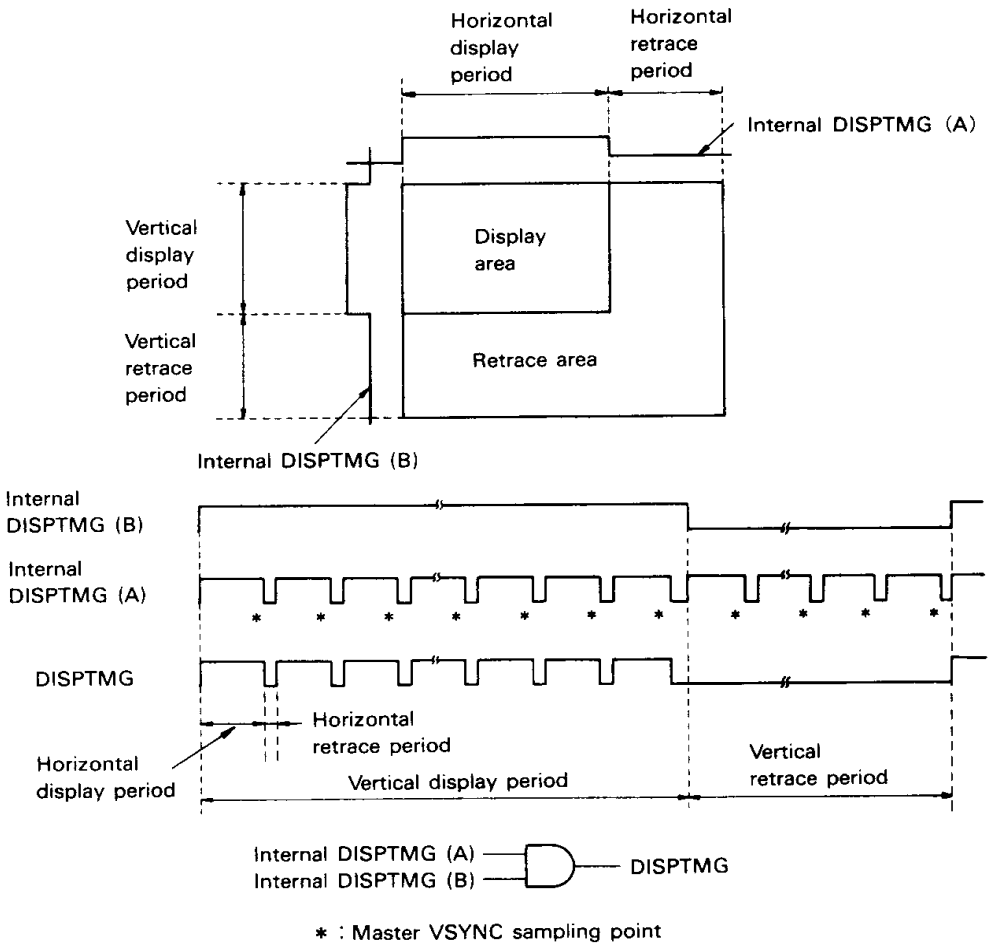


Figure 32-(b) External Sync Timing (TV Sync Mode: EXVSYNC)

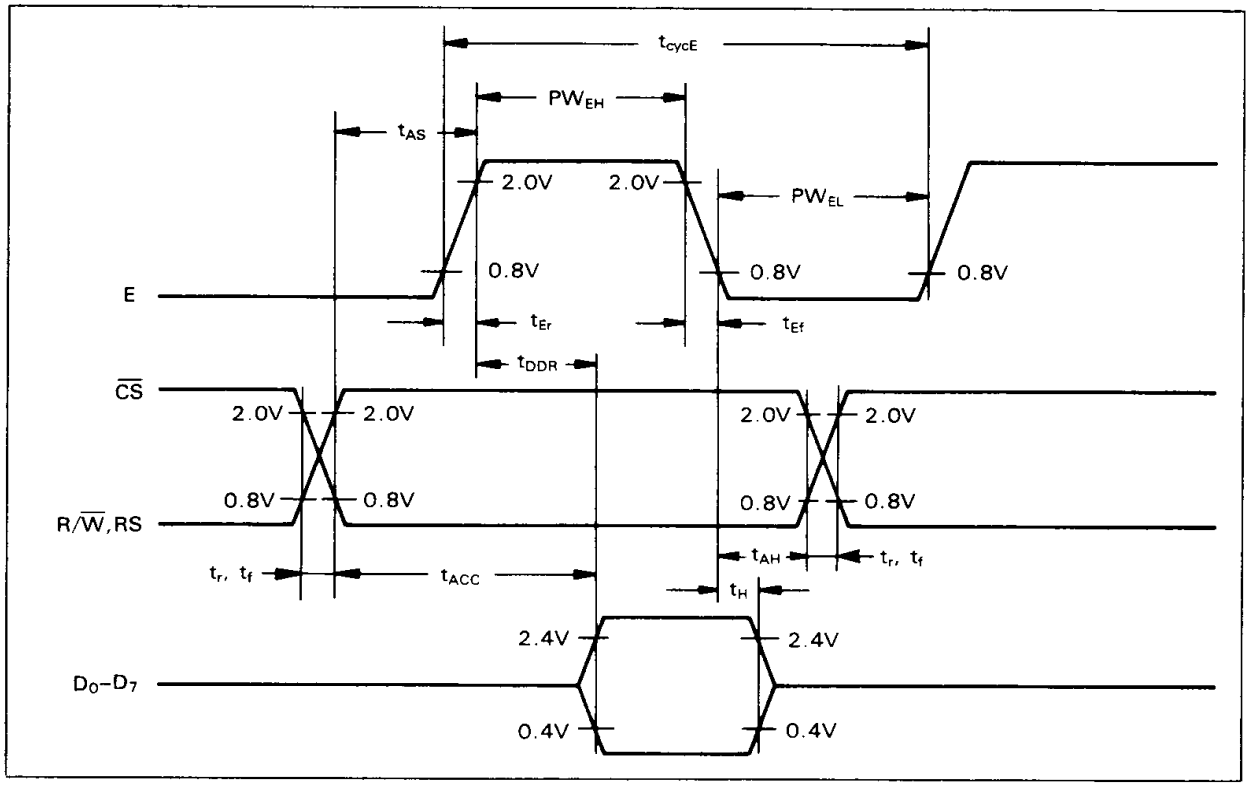


Figure 33 Read Sequence (HD6345)

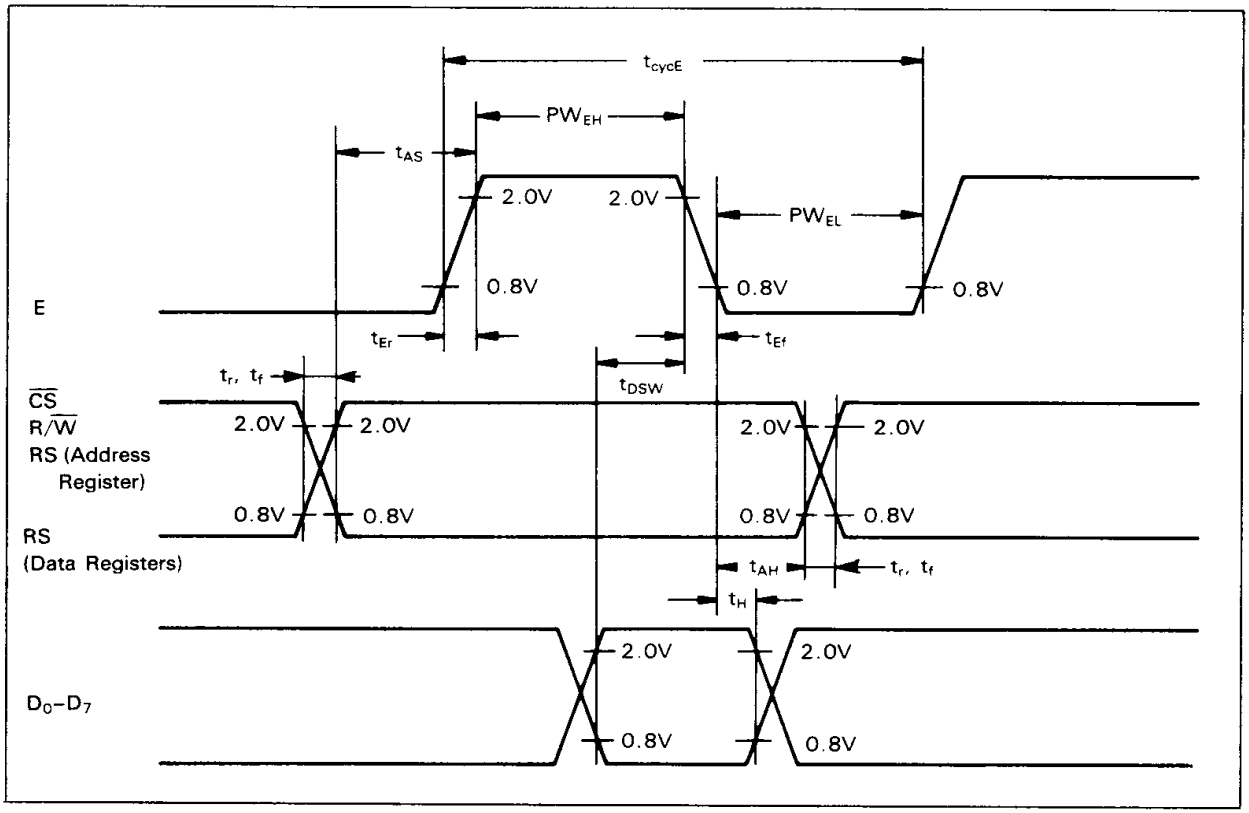


Figure 34 Write Sequence (HD6345)

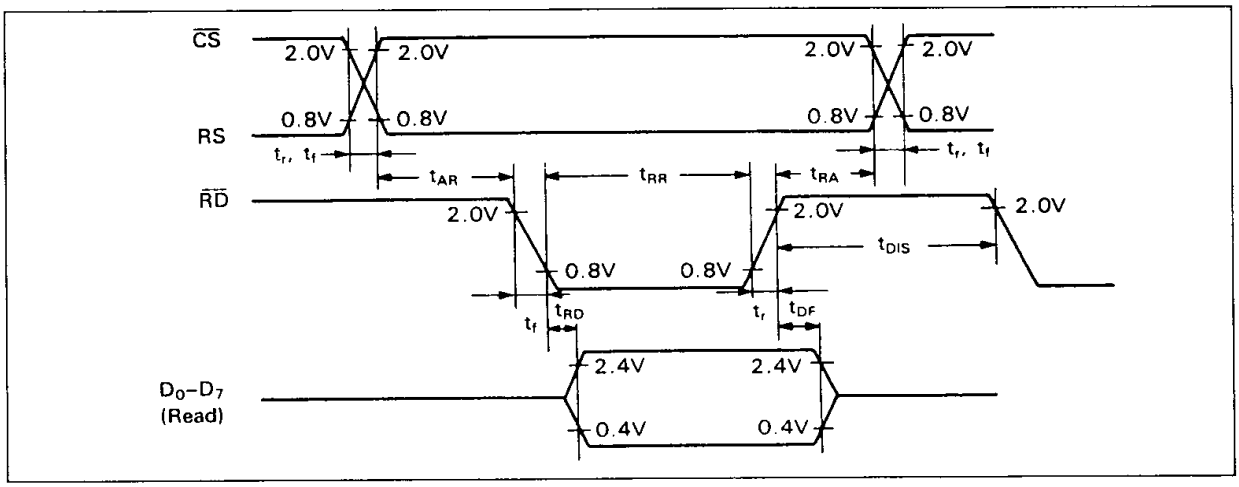


Figure 35 Read Sequence (HD6445)

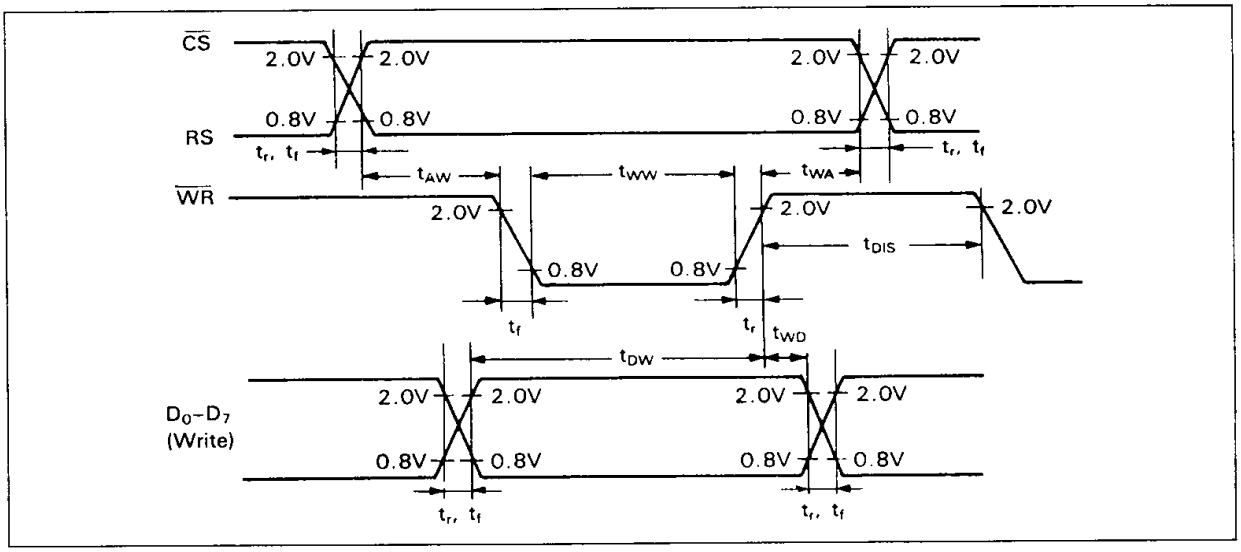


Figure 36 Write Sequence (HD6445)

TEST LOAD

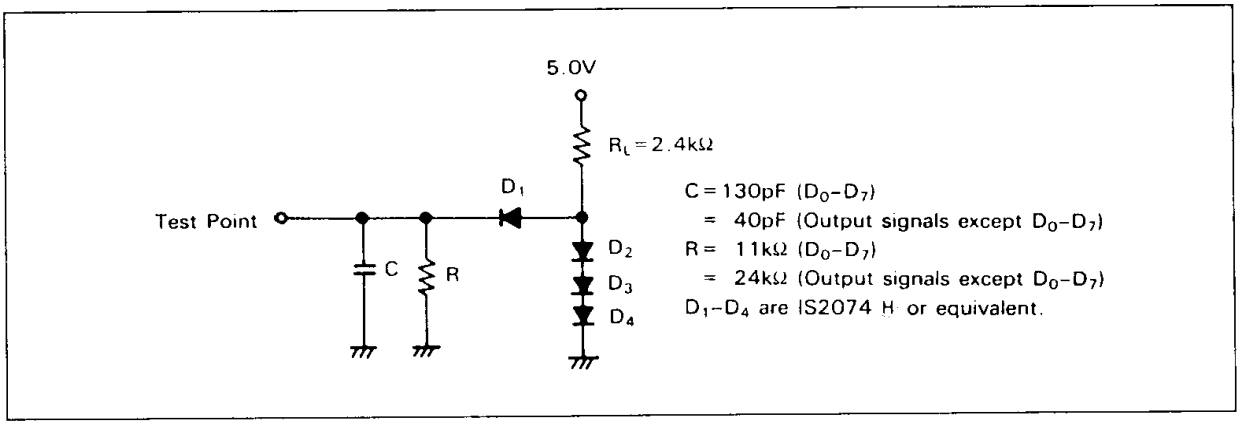


Figure 37 Test Load

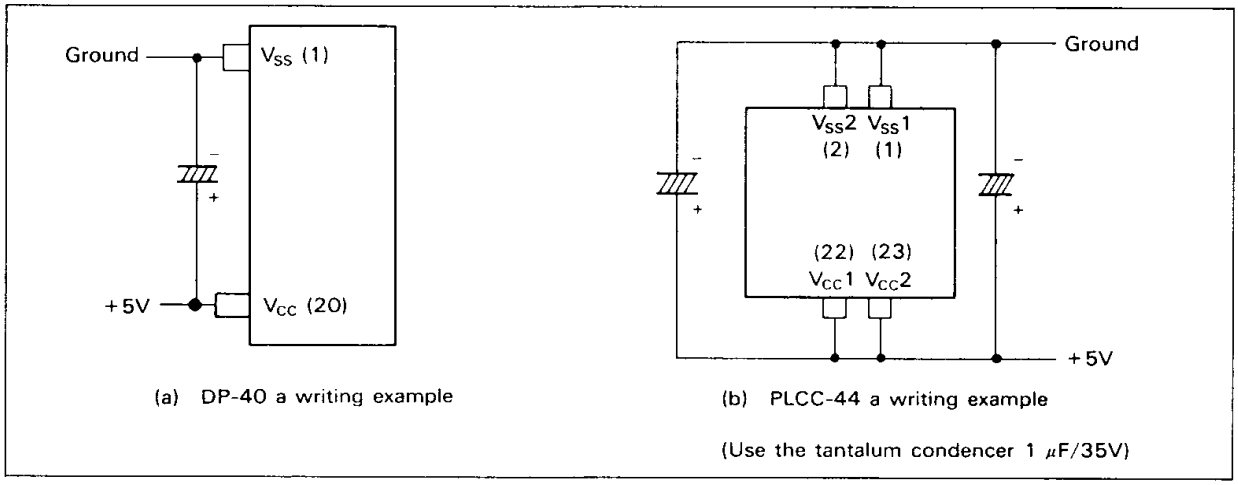


Figure 38 Note on Power Line Example

J SPECIFICATION

There is J specification in PLCC-44 of CRTC - II (HD6345/HD6445). J specification operating temperature is wider than normal specification operating temperature.

(1) Absolute maximum ratings

Item	Symbol	Rating	Unit
Operating temperature	T_{opr}	−40 to +85	°C

(2) Recommended operating conditions

		HD6345 CPJ			HD6445 CPJ			
Item	**Symbol**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
Input high level voltage	V_{IH}*	CLK 2.2	–	V_{CC}	CLK $\overline{WR}$ $\overline{RD}$ 2.2	–	V_{CC}	V
		Other 2.0	–	V_{CC}	Other 2.0	–	V_{CC}	V
Operating temperature	T_{opr}	−40	25	85	−40	25	85	°C

* This value is in reference to V_{SS} = 0 V.

(3) Electrical characteristics

		HD6345 CPJ			HD6445 CPJ			
Item	**Symbol**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
Input high level voltage	V_{IH}	CLK 2.2	–	V_{CC}	CLK $\overline{WR}$ $\overline{RD}$ 2.2	–	V_{CC}	V
		Other 2.0	–	V_{CC}	Other 2.0	–	V_{CC}	V

(4) Other item is the same normal specification items (Absolute Maximum Ratings, Recommended Operating Conditions, Electrical Characteristics).

CHARACTERISTICS DIFFERENCES BETWEEN HD6345 AND HD6845S

NO.	Item	Symbol	HD6345 Min	HD6345 Typ	HD6345 Max	HD6845S Min	HD6845S Typ	HD6845S Max	Unit
1	Power Dissipation	P_D	–	50	–	–	600	1000	mW
2	Clock Cycle Time	$tcyc_C$	220	–	–	270	–	–	ns
3	Clock High Pulse Width	PW_{CH}	100	–	–	130	–	–	ns
4	Clock Low Pulse Width	PW_{CL}	100	–	–	130	–	–	ns
5	Memory Address Delay Time	t_{MAD}	–	–	80	–	–	160	ns
6	Raster Address Delay Time	t_{RAD}	–	–	80	–	–	160	ns
7	Display Timing Delay Time	t_{DTD}	–	–	120	–	–	250	ns
8	Horizontal Sync Delay Time	t_{HSD}	–	–	100	–	–	200	ns
9	Vertical Sync Delay Time	t_{VSD}	–	–	120	–	–	250	ns
10	Cursor Display Delay Time	t_{CDD}	–	–	120	–	–	250	ns
11	Enable Cycle Time	$tcyc_E$	500	–	–	1000	–	–	ns
12	Enable High Pulse Width	PW_{EH}	220	–	–	450	–	–	ns
13	Enable Low Pulse Width	PW_{EL}	210	–	–	400	–	–	ns
14	Enable Rise and Fall Time	t_{Er}, t_{Ef}	–	–	20	–	–	–	ns
15	Address Set Up Time	t_{AS}	40	–	–	140	–	–	ns
16	Data Set Up Time	t_{DSW}	60	–	–	195	–	–	ns
17	Data Delay Time	t_{DDR}	–	–	120	–	–	320	ns
18	Data Access Time	t_{ACC}	–	–	160	–	–	460	ns
19	Input Signal Rise and Fall Time	t_r, t_f	–	–	100	–	–	–	ns

CHARACTERISTICS DIFFERENCES BETWEEN HD6445 AND HD6845S

NO.	Item	Symbol	HD6445 Min	HD6445 Typ	HD6445 Max	HD6845S Min	HD6845S Typ	HD6845S Max	Unit
1	Power Dissipation	P_D	–	50	–	–	600	1000	mW
2	Clock Cycle Time	$tcyc_C$	220	–	–	270	–	–	ns
3	Clock High Pulse Width	PW_{CH}	100	–	–	130	–	–	ns
4	Clock Low Pulse Width	PW_{CL}	100	–	–	130	–	–	ns
5	Memory Address Delay Time	t_{MAD}	–	–	80	–	–	160	ns
6	Raster Address Delay Time	t_{RAD}	–	–	80	–	–	160	ns
7	Display Timing Delay Time	t_{DTD}	–	–	120	–	–	250	ns
8	Horizontal Sync Delay Time	t_{HSD}	–	–	100	–	–	200	ns
9	Vertical Sync Delay Time	t_{VSD}	–	–	120	–	–	250	ns
10	Cursor Display Delay Time	t_{CDD}	–	–	120	–	–	250	ns

Refer to user's manual (No. ADE-602-006A), application note (No. ADE-502-004) for detail of this product.